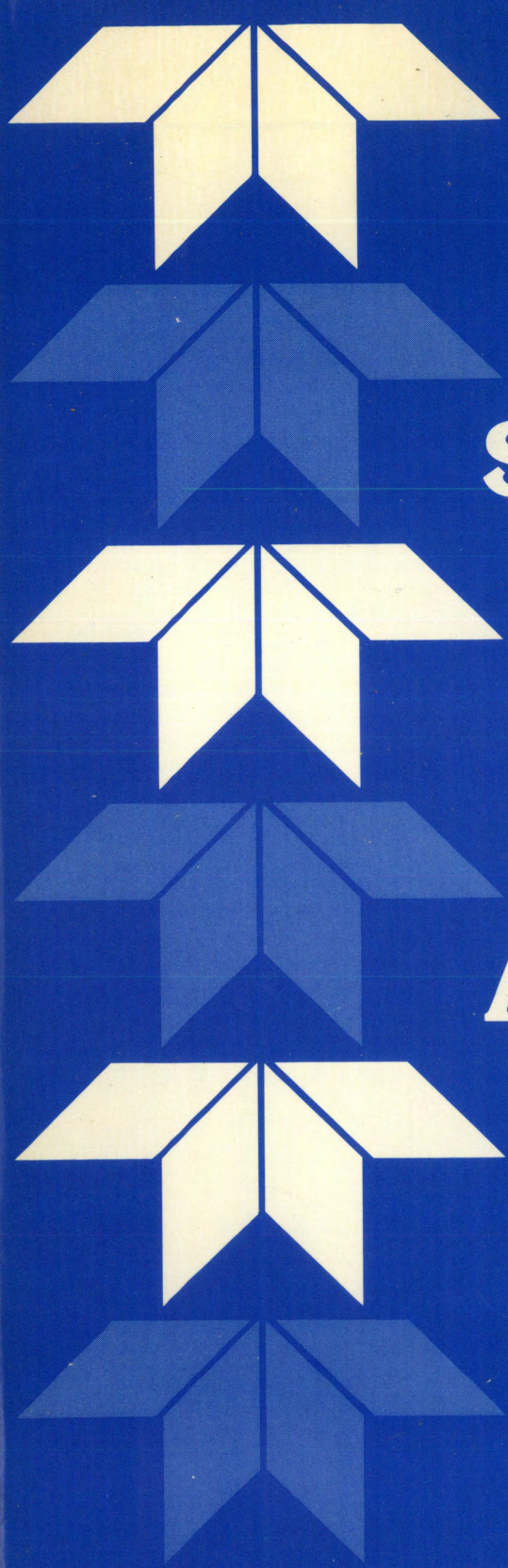
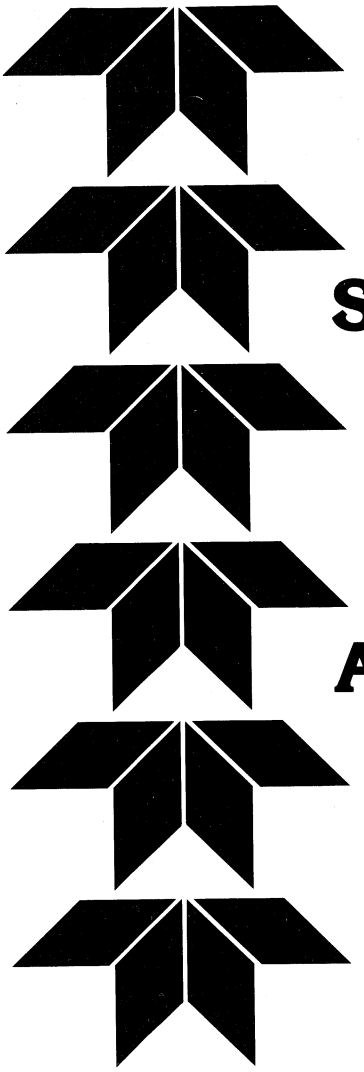


Teledyne Semiconductor

1984 Data Acquisition Design Handbook

TELEDYNE SEMICONDUCTOR



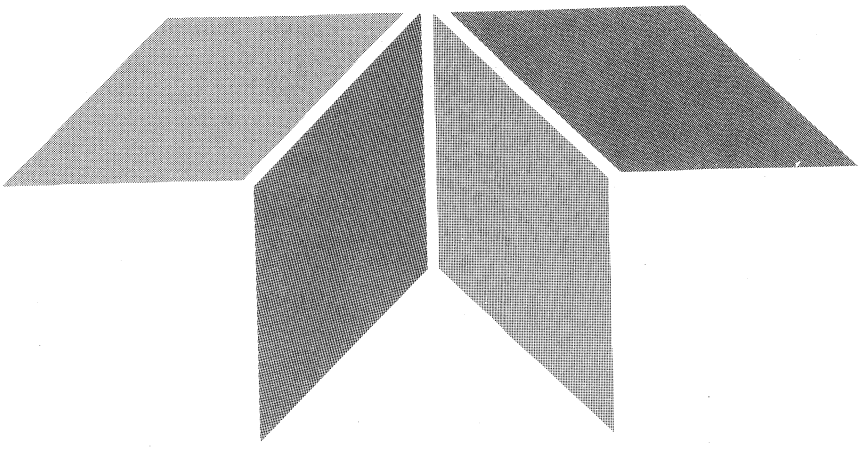
Teledyne Semiconductor

1984

Data Acquisition Design Handbook

1300 Terra Bella Avenue, Mountain View, California, USA 94043 • (415) 968-9241 TWX: (910) 379-6494

Printed in USA/October 1983



SECTION 1

Table of Contents

Section 1
Table of Contents 1-1

1984 Data and Design Manual

Section 1
Table of Contents 1-1

Section 2
Ordering Information/Package Drawings 2-1

Section 3
Quality Assurance Program 3-1

Section 4
Alphanumeric Product List 4-1

Section 5
Cross Reference Guide 5-1

Section 6
Advance Product Information 6-1

TSC426/427/428	High Speed Dual Power MOSFET Driver	6-3
TSC500	Precision Analog Processor	6-5
TSC805	Auto-Ranging Instrumentation A/D Converter	6-7
TSC826	LCD Bar Graph Display A/D Converter	6-9
TSC841	4 1/2 Digit A/D Converter	6-11

Section 7
Display A/D Converters 7-1

TSC7106A/7107A	(LCD Drive) 3 1/2 Digit A/D Converter	7-3
TSC7106/TSC7107	(LED Drive) 3 1/2 Digit Converter	7-21
TSC7116A/7117A	(LCD Drive) 3 1/2 Digit A/D Converter	7-33
TSC7116/7117	(LED Drive) 3 1/2 Digit A/D Converter	7-45
TSC7126A	3 1/2 Digit A/D Converter	7-57
TSC7126	3 1/2 Digit A/D Converter	7-69
TSC7135	4 1/2 Digit Precision A/D Converter	7-81
TSC8750	3 1/2 Digit ADC w/Parallel BCD Output	7-93
TSC14433A	Precision 3 1/2 Digit ADC	7-101
TSC14433B	Low Cost 3 1/2 Digit ADC	7-107
TSC14433	3 1/2 Digit ADC	7-113

Section 8
Binary A/D Converters 8-1

TSC7109	12-Bit Plus Sign Integrating A/D Converter	8-3
TSC800	15-Bit Plus Sign Integrating A/D Converter	8-23
TSC8700 (8-Bit)	Binary Output ADC	8-39
TSC8701 (10-Bit)	Binary Output ADC	8-39
TSC8702 (12-Bit)	Binary Output ADC	8-39
TSC8703 (8-Bit)	Three State Binary Output ADC	8-51
TSC8704 (10-Bit)	Three State Binary Output ADC	8-51
TSC8705 (12-Bit)	Three State Binary Output ADC	8-51

Section 9
Voltage to Frequency/Frequency to Voltage Converters 9-1

TSC9400	(0.05% Linearity)	9-3
TSC9401	(0.01% Linearity)	9-3
TSC9402	(0.25% Linearity)	9-3

Table of Contents

Section 10
Display Drivers 10-1

TSC700A	High Current Four Digit LED Driver	10-3
TSC701AM	High Current Bus Compatible Four Digit LED Driver	10-11
TSC7211A	Four Digit LCD Driver	10-19
TSC7212A	Four Digit LED Driver	10-19
TSC7211AM	Bus Compatible Four Digit LCD Driver	10-31
TSC7212AM	Bus Compatible Four Digit LED Driver	10-31

Section 11
Interface IC's 11-1

TSC450	Dual Power MOSFET Driver	11-3
TSC7660	DC to DC Voltage Converter	11-7
TSC9403	Serial Input/16-Bit Parallel Output Peripheral Driver	11-17
TSC9404	Serial Input/16-Bit Parallel Output Peripheral Driver	11-17

Section 12
References 12-1

TSC9491	1.22 V Bandgap Reference	12-3
TSC9495	+5 V Bandgap Voltage Reference/Temperature Transducer	12-5
TSC9496	+10 V Bandgap Voltage Reference	12-9

Section 13
Operational Amplifiers 13-1

TSC7650	Precision Chopper - Stabilized Operational Amplifier	13-3

Section 14
Digital Logic 14-1

	Purpose of Bipolar Interface Logic	14-3
	Most Popular 300 Series Devices	14-4
	Electrical Summary Data	14-6
	Input Current Requirements	14-8
	Output Sink Current vs. Output Voltage	14-9
	Pin-Out Guide	14-10
TSC301	Power NAND Gates Dual 5-Input	14-15
TSC302	Power NAND Gates Quad 2-Input	14-15
TSC303	Power NAND Gates Quad 2-Input	14-15
TSC304	Power NAND Gates Triple 4, 3, 4-Input	14-15
TSC306	NOR Gate Quad 2, 2, 3, 3-Input	14-19
TSC307	NOR Gate Quad 2, 2, 3, 3-Input	14-19
TSC311	Flip Flops Master/Slave RST	14-21
TSC312	Flip Flops Dual J-K Edge Triggered	14-21
TSC313	Flip Flops Dual J-K Master/Slave	14-21
TSC321	NAND Gates Quad 2-Input	14-27
TSC322	NAND Gates Dual 5-Input	14-27
TSC323	NAND Gates Quad 2-Input	14-27
TSC324	NAND Gates Quad 2-Input	14-27
TSC325	NAND Gates 2, 2, 3, 3-Input	14-31
TSC326	NAND Gates 2, 2, 3, 3-Input	14-31
TSC331	Gate Expander Dual 5-input	14-35
TSC332	Hex Inverter Gates 4-Inverter, 2-NAND	14-37
TSC333	Hex Inverter Gates 4-Inverter, 2-NAND	14-37
TSC334	Hex Inverter Gates Strobed Hex NAND	14-37
TSC335	Hex Inverter Gates Strobed Hex NAND	14-37
TSC341	Multifunction Gates Dual 2-Wide, 2-Input and/or Invert	14-41
TSC342	Dual Monostable Multivibrator	14-45
TSC343	Digital Comparator 4-Bit	14-49
TSC347	Dual Retriggerable Monostable Multivibrator	14-53

Section 14
Digital Logic (cont.)

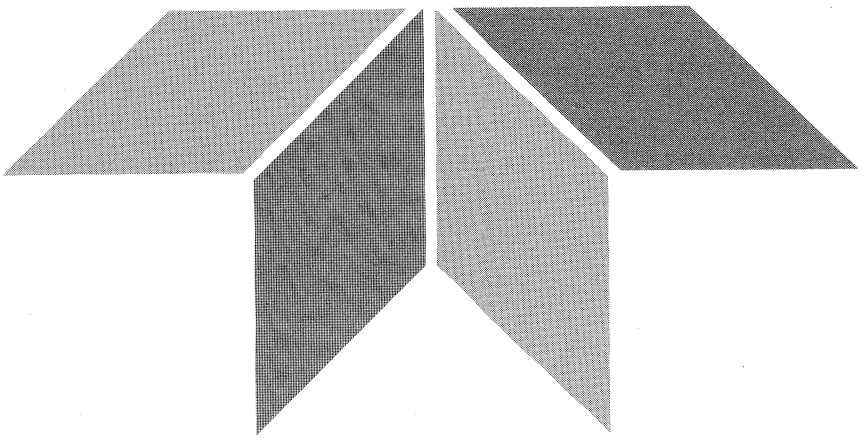
TSC349 Dual Retriggerable Pulse Stretcher 14-57
TSC350 Multiplexers 8-Bit 14-61
TSC351 Multiplexers Dual 4-Bit 14-61
TSC355 Timer 14-65
TSC361 Dual 11-16 V to 5 V Interface Voltage Translator 14-69
TSC362 5 V to 11-16 V Interface Dual Transistor 14-71
TSC363 5 V to 11-16 V Interface Quad 2-Input NAND 14-71
TSC367 Schmitt Trigger Quad Active Pullup 14-75
TSC368 Schmitt Trigger Quad Open Collector 14-75
TSC370 Flip Flop Quad D 14-81
TSC371 Counters Decade 14-83
TSC372 Counters Hexadecimal 14-83
TSC373 Up-Down Counter Decade 14-87
TSC374 Up-Down Counter Hexadecimal 14-87
TSC375 Shift Register 4-Bit 14-91
TSC380 BCD-to-Decade Decoder/Drivers Lamp Driver 14-95
TSC381 BCD-to-Decade Decoder/Drivers Logic Driver 14-95
TSC382 BCD-to-Decade Decoder/Drivers Gas Tube Driver 14-99
TSC383 Decoder/Driver BCD-to-7 Segment 14-103
TSC390 Dual Interface Buffers 4-Input Expandable AND 14-107
TSC391 Dual Interface Buffers 2-Input AND 14-107
TSC392 Dual Interface Buffers 2-Input NAND 14-107
TSC393 Dual Interface Buffers 2-Input OR 14-107
TSC394 Dual Interface Buffers 2-Input NOR 14-107
TSC395 Dual Interface Buffers 4-Input Expandable NAND 14-107
TSC396 Line Driver Receiver Dual Differential 14-111

Section 15
Application Notes 15-1

Application Note 1 Using High Noise Immunity Logic 15-3
Application Note 2 Design Techniques with HiNIL Schmitt Trigger 367 Quad 15-11
Application Note 3 Designing Programmable Controllers with HiNIL 15-15
Application Note 4 HiNIL 375 Universal Shift Register 15-19
Application Note 5 High Noise Immunity Logic — Powerful, Versatile and Growing 15-29
Application Note 6 The HiNIL 347 Dual Retriggerable One-Shot Theory and Applications 15-35
Application Note 7 Using Bipolar Logic to Improve Performance in CMOS and Microprocessor Systems 15-41
Application Note 8 Interfacing the 8700 A/D with the 8080 μP System 15-45
Application Note 9 Applications of the 8700 Series A/D Converters 15-51
Application Note 10 Applications of the 9400 V/F, F/V Converters 15-67
Application Note 11 7106/7107 Digital Meter Applications 15-77
Application Note 12 A Single IC Digital Thermocouple Thermometer Using the 7106 15-85
Application Note 16 TSC7135 Microprocessor Interface 15-87
Application Note 17 Simplify A/D Converter Interface w/Software 15-91
Application Note 18 TSC7211AM/TSC7212AM Display Driver Microprocessor Interface 15-95
Application Note 19 BCD A/D Converter Interface to Dot Matrix LEDs 15-99
Application Note 20 Two Digit Serial Input LED Display Driver Using TSC9404 15-101
Application Brief 1 Combining HiNIL and CMOS — an Optimum Design Technique 15-103
Application Brief 2 Protecting Logic Inputs 15-107
Application Brief 3 The 355 Timer Solves Noise Problems 15-109
Application Brief 4 Keeping the Bugs Out of Microprocessor Systems with High Noise Immunity Logic 15-111
Application Brief 5 HiNIL Interface Summary 15-113
Application Brief 6 Typical Applications for Bipolar Interface Logic 15-115

Section 16
Glossary of Terms and Abbreviations 16-1

Section 17
Distributors and Representatives 17-1



SECTION 2

Ordering Information
Package Information

Section 2
Ordering Information/Package Drawings 2-1

The Device Identification Codes for Device Numbers of TSC8700, TSC9400 and TSC14433 Family are as Follows:

PACKAGED DEVICES — TSC XXXXX X X X X

1. TELEDYNE SEMICONDUCTOR DEVICE
2. DEVICE NUMBER
3. ELECTRICAL GRADE (if applicable)
4. R – REVERSE LEAD CONFIGURATION (if applicable)
5. OPERATING TEMPERATURE RANGE
   - C – Commercial Temperature Range (0–70°C)
   - E – Extended Temperature Range (–40 to +85°C)
   - B – Military Temperature Range (–55 to +125°C)
6. PACKAGE TYPE
   - J – Plastic Package
   - N – Ceramic Package
   - L – CerDIP
   - Y – Dice
   - E – Metal Can (TO–99)
   - M – Metal Can (TO–18)

EXAMPLE: TSC8701CL Operates Over the Commercial Temperature Range and is a CerDIP Package

PRODUCT STATUS

Three Classes of Data Sheets are Shown in this Data Book. These are Identified by the Presence or Absence of a "Banner" on the First Page.

DATA SHEET INDENTIFICATION	PRODUCT STATUS	COMMENTS
No Identification	Production	Data Sheet Finalized Delivery Subject to Product Demand.
Preliminary	Initial Production	Data Sheet Electrical Limits Established. Limited Production Quantities Available. Samples Available.
Advance Product Information	Design	Data Sheet Gives Design Goal, Electrical Specifications and Major Product Features. Contact Teledyne Marketing for Samples and Information.

Note: Teledyne Semiconductor Reserves the Right to Make Changes at Any Time Without Notice in Order to Improve Performance and Supply.

Ordering Information

All Other CMOS ICs (Except 87XX/94XX/14433 Products)

The Device Identification Codes for All Other CMOS Products and All Products in 60-Pin Flat Packages are as Follows:

PACKAGED DEVICES — TSC XXXXXX X X X X / XXX

1. TELEDYNE SEMICONDUCTOR DEVICE

2. DEVICE NUMBER

3. ELECTRICAL PERFORMANCE GRADE OPTION (if applicable)
   - R – Reversed Pin Layout

4. OPERATING TEMPERATURE RANGE
   - M – Military Temperature Range (–55°C to +125°C)
   - I* – Industrial Temperature Range (–25°C to +85°C)
   - C – Commercial Temperature Range (0°C to +70°C)
   - * – May Be –40°C to +85°C. Refer to Specific Device Specification

5. PACKAGE TYPE
   - J – CerDIP Dual-In-Line (non side brazed)
   - P – Plastic Dual-In-Line
   - T – TO–99 Type (round metal can)
   - B – Plastic Flat Package (formed leads)
   - S – Plastic Flat Package (unformed (straight) leads)

6. NUMBER OF PACKAGE PINS

A – 8	N – 18	Y – 8 (pin 4 connected to case)
D – 14	G – 24	Q – 60
E – 16	I – 28	S – 68
F – 22	L – 40	

7. PROCESSING OPTION
   - 883 – MIL-STD-883B, Class B Processing
   - BI – 100% Burn-In at 125°C for 160 Hours

PACKAGED DEVICES

TSC XXX X X

1. TELEDYNE SEMICONDUCTOR DEVICE

2. DEVICE NUMBER

3. ELECTRICAL GRADE AND TEMPERATURE RANGE
   - A — Industrial Temperature Range, 15 V, (−30 to +70°C)
   - B — Military Temperature Range, 12 V, (−55 to +125°C)
   - C — Industrial Temperature Range, 12 V, (−30 to +85°C)
   - M — Military Temperature Range, 15 V, (−55 to +125°C)

4. PACKAGE TYPE
   - G — Metal Can (TO−8)
   - H — Flatpack
   - J — Plastic Package
   - L — Ceramic Package (CerDIP)
   - Y — Dice

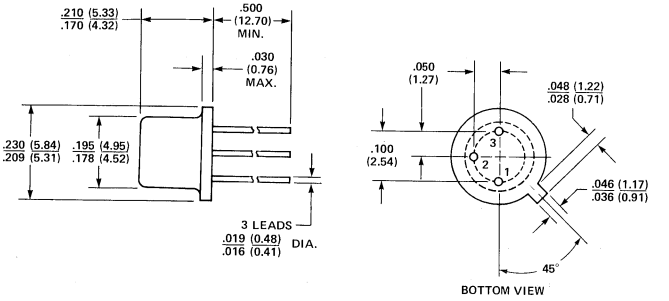
EXAMPLE: 303AL Operates Over an Industrial Temperature Range at 15 V and is a CerDIP Package

Product List — Digital Logic

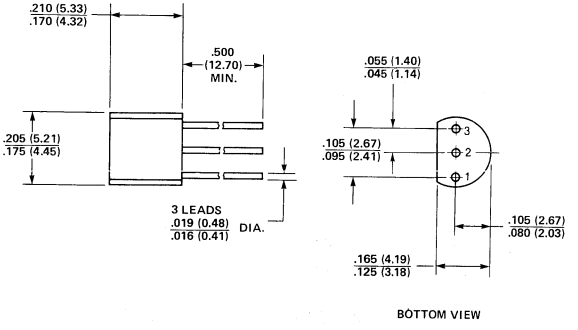
301 Power NAND Gates Dual 5-Input
302 Power NAND Gates Quad 2-Input
303 Power NAND Gates Quad 2-Input
304 Power NAND Gates Triple 4, 3, 4-Input
306 NOR Gate Quad 2, 2, 3, 3-Input
307 NOR Gate Quad 2, 2, 3, 3-Input
311 Flip Flops Master/Slave RST
312 Flip Flops Dual J-K Edge Triggered
313 Flip Flops Dual J-K Master/Slave
321 NAND Gates Quad 2-Input
322 NAND Gates Dual 5-Input
323 NAND Gates Quad 2-Input
324 NAND Gates Quad 2-Input
325 NAND Gates 2, 2, 3, 3-Input
326 NAND Gates 2, 2, 3, 3-Input
331 Gate Expander Dual 5-Input
332 Hex Inverter Gates 4-Inverter, 2-NAND
333 Hex Inverter Gates 4-Inverter, 2-NAND
334 Hex Inverter Gates Strobed Hex NAND
335 Hex Inverter Gates Strobed Hex NAND
341 Multifunction Gates Dual 2-Wide, 2-Input and/or Invert
342 Dual Monostable Multivibrator
343 Digital Comparator 4-Bit
344 Multifunction Gates Dual Expandable AND-NOR
347 Dual Retriggerable Monostable Multivibrator
349 Dual Retriggerable Pulse Stretcher
350 Multiplexers 8-Bit
351 Multiplexers Dual 4-Bit
355 Timer
361 Dual 11-16V to 5V Interface Voltage Translator
362 5V to 11-16V Interface Dual Translator
363 5V to 11-16V Interface Quad 2-Input NAND
367 Schmitt Trigger Quad(Active Pullup)
368 Schmitt Trigger Quad(Open Collector)
370 Flip Flop Quad D
371 Counters Decade
372 Counters Hexadecimal
373 Up-Down Counters Decade
374 Up-Down Counters Hexadecimal
375 Shift Register 4-Bit
380 BCD-to-Decade Decoder/Drivers Lamp Driver
381 BCD-to-Decade Decoder/Drivers Logic Driver
382 BCD-to-Decade Decoder/Drivers Gas Tube Driver
383 Decoder/Driver BCD-to-7 Segment
390 Dual Interface Buffers 4-Input Expandable AND
391 Dual Interface Buffers 2-Input AND
392 Dual Interface Buffers 2-Input NAND
393 Dual Interface Buffers 2-Input OR
394 Dual Interface Buffers 2-Input NOR
395 Dual Interface Buffers 4-Input Expandable NAND
396 Line Driver/Receiver Dual Differential

Package Information

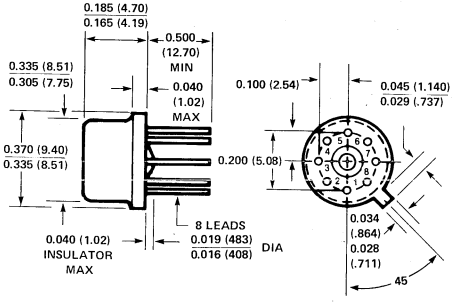
(Package #1)
TO-18 (3 Pin)



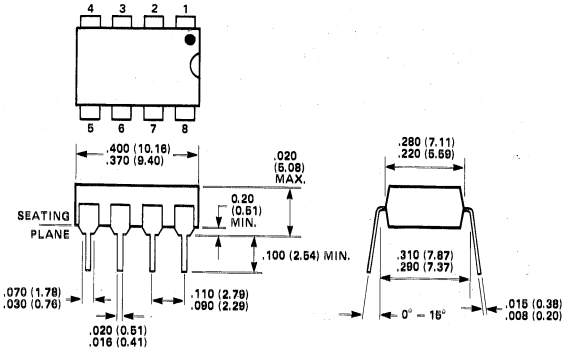
(Package #2)
TO-92 (3 Pin)



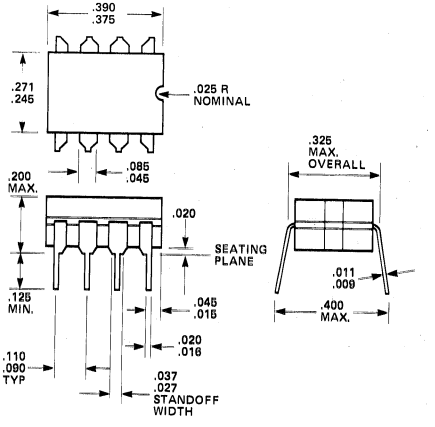
(Package #3)
TO-99 (8 Pin)



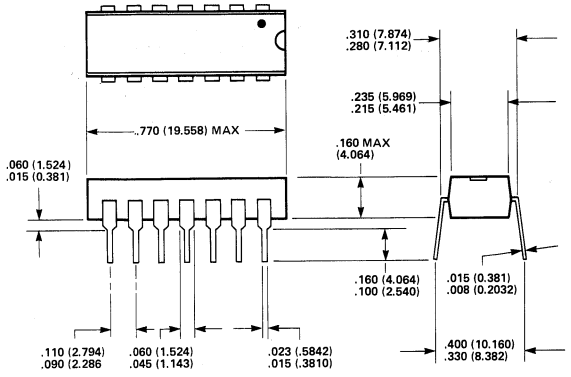
(Package #4)
8-Pin Plastic Dip (J Package)



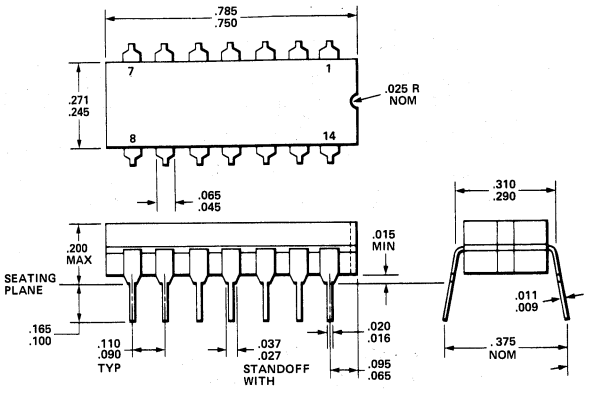
(Package #5)
8-Pin CerDIP (L Package)



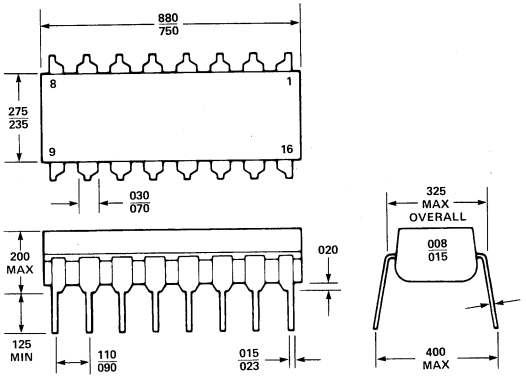
(Package #6)
14-Pin Plastic Dip (J Package)



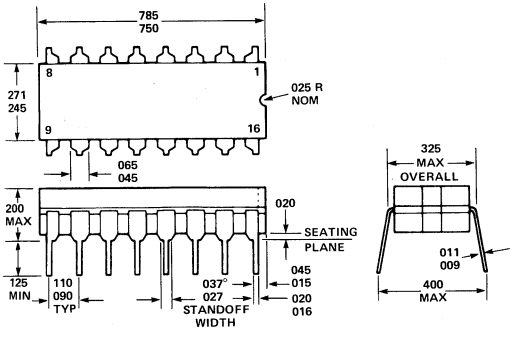
(Package #7)
14-Pin CerDIP (L Package)

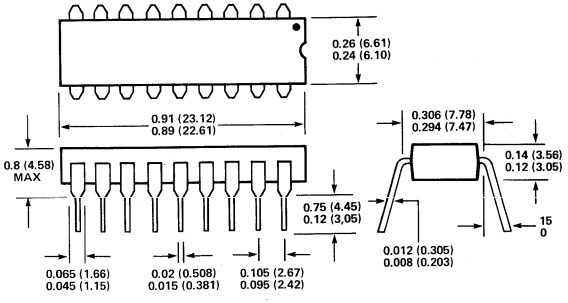


(Package #8)
16-Pin Plastic Dip (L Package)



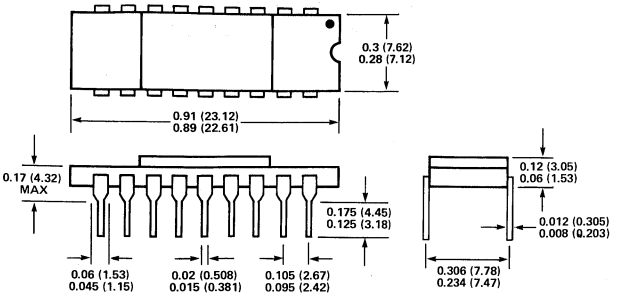
(Package #9)
16-Pin CerDIP (L Package)





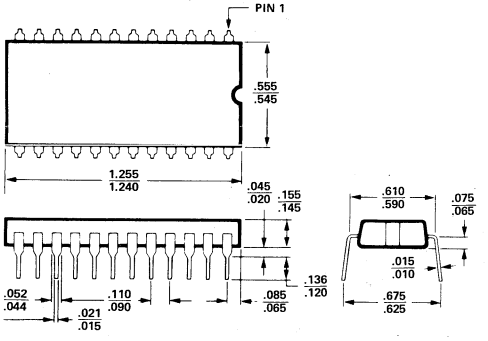
(Package #10)
18-Pin Plastic Dip (J Package)

Package Information

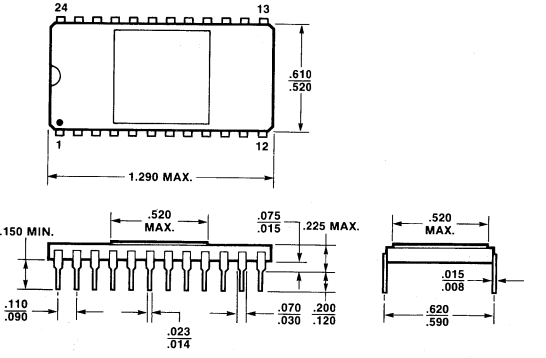


(Package #11)
18-Pin Ceramic Dip (N Package)

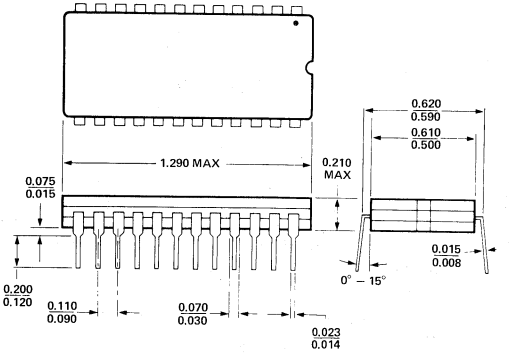
(Package #12)
24-Pin Plastic Dip (J Package)



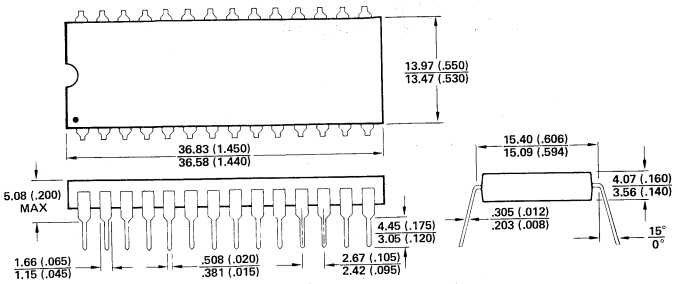
(Package #13)
24-Pin Ceramic Dip (N Package)

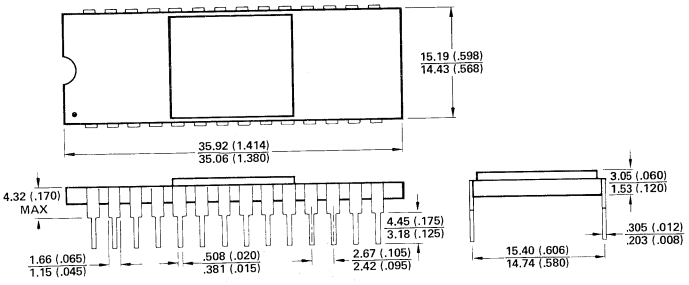


(Package #14)
24-Pin CerDIP (L Package)



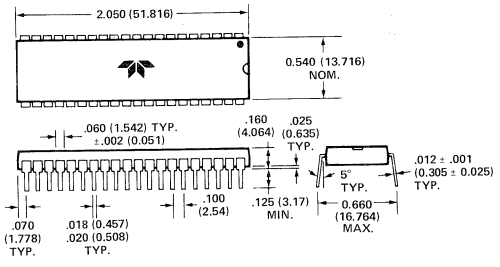
(Package #15)
28-Pin Plastic Dip (J Package)



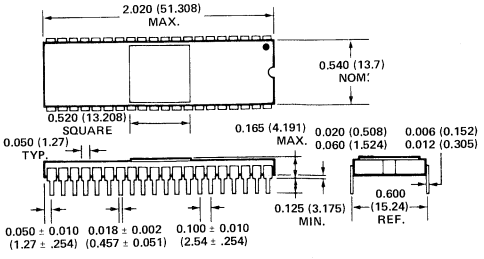


(Package #16)
28-Pin Ceramic Dip (N Package)

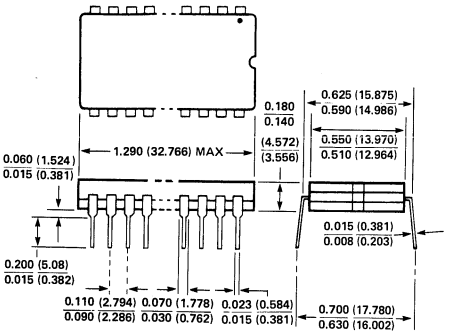
(Package #17)
40-Pin Plastic Dip (PL Package)



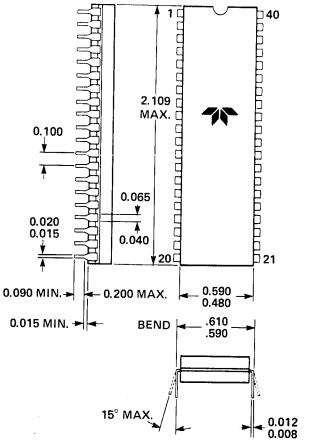
(Package #18)
40-Pin Ceramic Dip (DL Package)



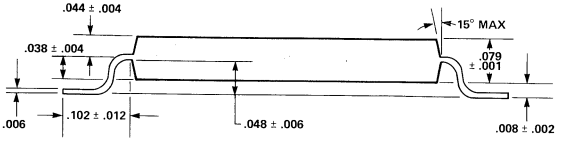
(Package #19)
28-Pin CerDIP (J Package)



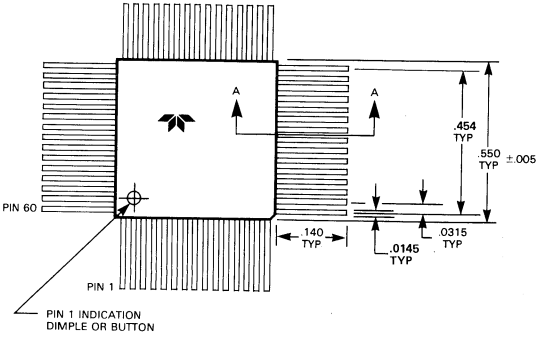
(Package #20)
40-Pin CerDIP

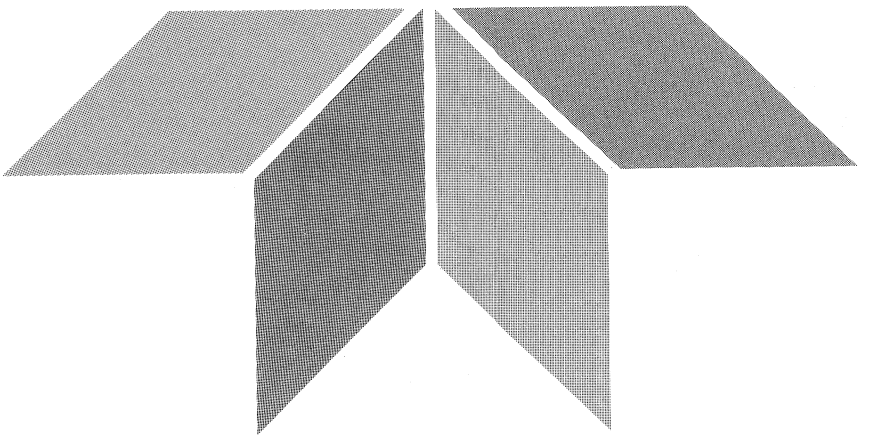


(Package #21)
60-Pin Flat Package
Formed Leads



(Package #22)
60-Pin Flat Package
Unformed Leads





SECTION 3

Quality Assurance Program

Section 3
Quality Assurance Program 3-1

Teledyne Semiconductor Product Assurance Program

Teledyne Semiconductor's Product Assurance Program is based on four major blocks:

- **Quality Control**
- **Quality Assurance**
- **Reliability**
- **Quality Circles**

Quality Control

The Quality Control function handles continuous monitoring of production, from incoming inspection of raw materials to wafer and assembly processing. This includes surveillance of documentation, calibration, and environmental processing.

The three major areas of Quality Control are:

- Incoming Inspection
- In-Process Control
- Operation Surveillance

Quality Assurance

The Quality Assurance (QA) function involves checking the ability of manufactured parts to meet specifications.

After devices are subjected to 100% testing in manufacturing, they are formed into lots and submitted to Quality Assurance acceptance testing. Three types of tests are performed on samples: Visual/Mechanical, Parametric, and Functional. The sampling is based on a plan equivalent to a 0.11 AQL. All testing is done at room and elevated temperature. Lower temperature testing is performed when required by the specification, or when a potential problem is known to exist.

Reliability

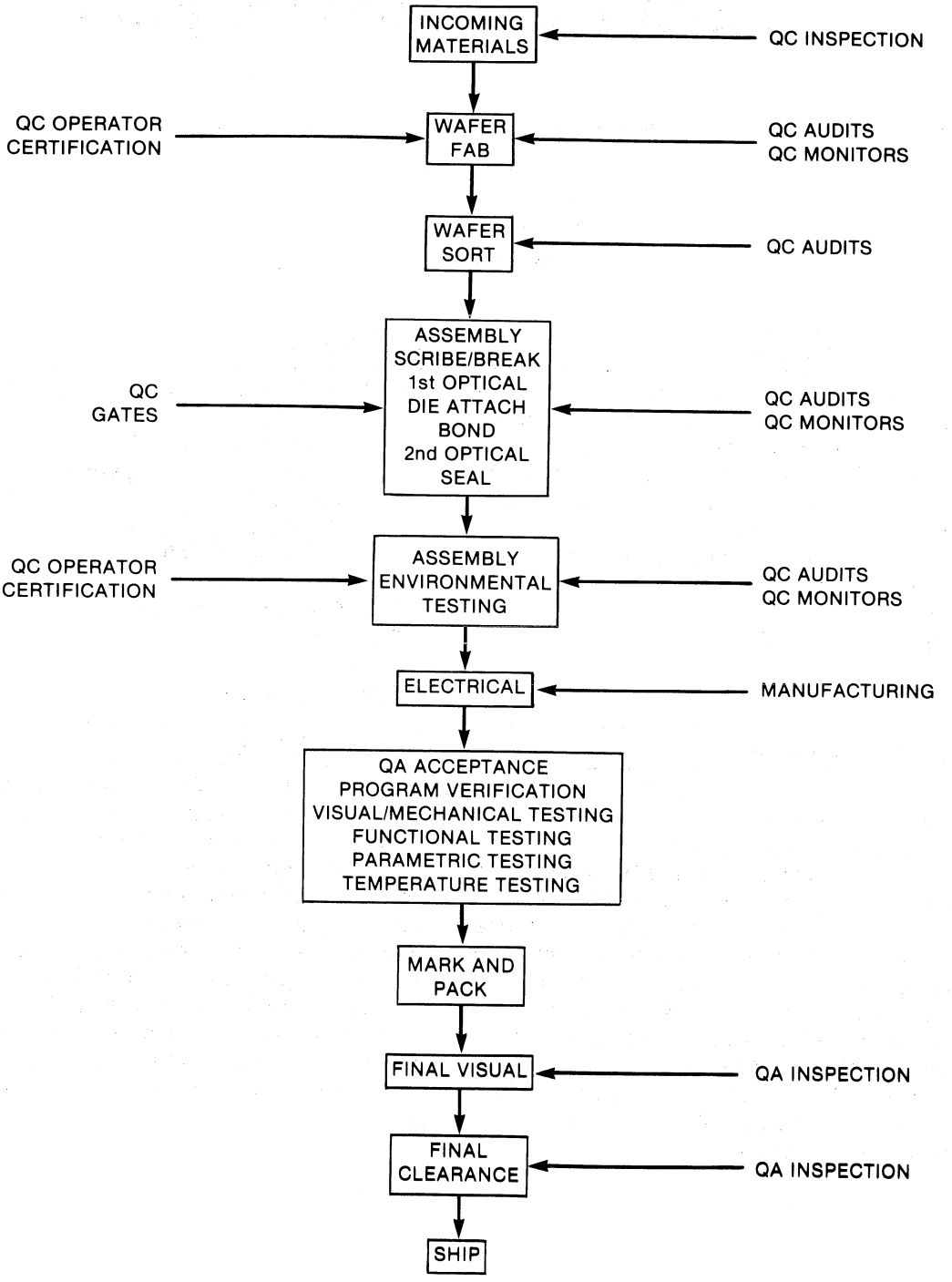
The Reliability Group is responsible for the following functions:

- New Process Qualification
- Process Change Qualification
- Process Monitoring
- New Device Qualification
- Device Change Qualification
- Device Monitoring
- New Package Qualification
- Package Change Qualification
- Package Monitoring
- Failure Analysis

Quality Control Circles

Quality Control Circles are a vital part of the quality loop at Teledyne Semiconductor. The concept allows each employee directly involved in manufacturing to have a voice in how to build a quality product. Volunteers within a group meet weekly to determine and solve problems. Some solutions to problems may be implemented on the job. Others require management support, and to this end, circle members are trained in management presentation. The goal is total employee involvement with an emphasis on building-in quality.

Product Assurance Program



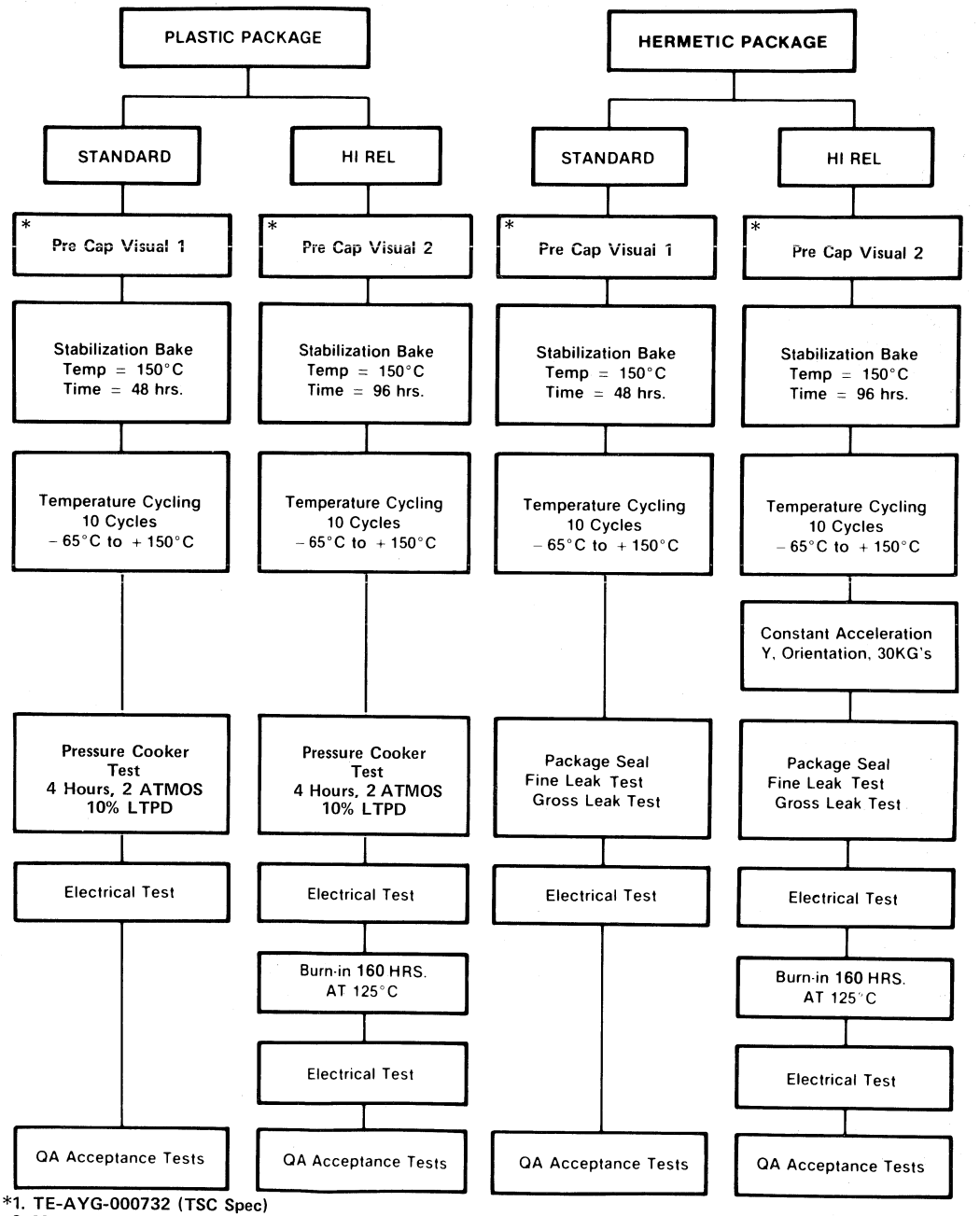
Generic Data

Generic Data is generated on a three month basis (maximum) for the following test.

MIL-STD-883B Quality Conformance Tests	Method	Test Condition	LTPD
GROUP B			
SUBGROUP 1			
Physical Dimensions	2016		2 Devices
SUBGROUP 2			
Resistance to Solvents	2015		3 Devices
Internal Visual: Mechanical	2014		1 Device
Bond Strength	2011	Test Condition C or D	15
GROUP C			
SUBGROUP 1			5
Steady State Life Test	1005	1000 hrs. at 125°C	
Electrical End Points			
SUBGROUP 2			15
Temperature Cycling	1010	Test Condition C	
Constant Acceleration	2001	Test Condition E, Y only	
Seal	1014		
Fine			
Gross			
Visual Examination			
Electrical End Points			
GROUP D			
SUBGROUP 1			15
Physical Dimensions	2016		
Internal Water-Vapor Content	1018	5,000 PPM — Cerdip only	3 Devices
SUBGROUP 2			
Lead Integrity	2004	Test Condition B2	
Seal	1014		
Fine			
Gross			
SUBGROUP 3			15
Thermal Shock	1011	Test Condition B, 15 Cycles	
Temperature Cycling	1010	Test Condition C, 100 Cycles	
Moisture Resistance	1004		
Seal	1014		
Fine			
Gross			
Visual Examination			
Electrical End Points			
SUBGROUP 4			15
Mechanical Shock	2002	Test Condition B	
Vibration Variable Frequency	2007	Test Condition A	
Constant Acceleration	2001	Test Condition E, Y only	
Seal	1014		
Fine			
Gross			
Visual Examination			
Electrical End Points			
SUBGROUP 5			15
Salt Atmosphere	1009	Test Condition A	
Seal	1014		
Fine			
Gross			
Visual Examination			

Quality Assurance
Integrated Circuit Screening

PER MIL-STD-883



*1. TE-AYG-000732 (TSC Spec)
2. MIL-STD-883, Method 2010

I.C. Handling Precautions

Transportation

Two main concerns to be minimized during transportation are mechanical vibration and shock and Electrostatic Discharge (ESD) damage. While mechanical shock can be minimized by suitable packing and handling, ESD damage requires additional measures including:

- Use containers or jigs which will not induce static electricity as the result of vibration during transportation. It is desirable to use an electrically conductive foam or aluminum foil and static eliminating bags.
- In order to prevent device breakage from clothing-induced static electricity workers should be properly grounded with ground ing straps while handling devices. A resistor of about 1 M ohm must be provided to protect from electric shock.
- When transporting the printed circuit boards on which semiconductor devices are mounted suitable preventive measures against static electricity transfer and induction must be taken. Shorting connectors should be placed on open contacts and the board transported in electrically conductive bags.

Storage

It is preferable to store semiconductor devices in the following ways to prevent deterioration in their electrical characteristics, solderability, and mechanical appearance.

- Store in an ambient temperature of 5 to 30° C, and in a relative humidity of 40 to 60%.
- Store in a clean air environment, free from dust and active gas.
- Store in a container which does not induce static electricity.
  Store without any physical load.
  If semiconductor devices are stored for a long time, store them as sent from the factory. If their lead wires are formed beforehand, they may corrode during storage.
  If the chips are unsealed, store them in a cool, dry, dark, and dustless place. Assemble them within 5 days after unpacking. Storage in nitrogen gas is desirable. They can be stored for 20 days or less in dry nitrogen gas with a dew point at -30° C or lower. Unpacked devices must not be stored for over 3 months.
  Take care not to allow condensation during storage due to rapid temperature changes.

I.C. Handling Precautions (cont.)

Testing

Avoid ESD, noise or voltage surges when testing I.C.S. The device is in its least protected state during handling, insertion and testing. Any test equipment that leaks current or is allowed to attain only a few hundred volts of ESD can destroy CMOS I.C.S. All equipment must be grounded and periodically tested for leakage.

Soldering

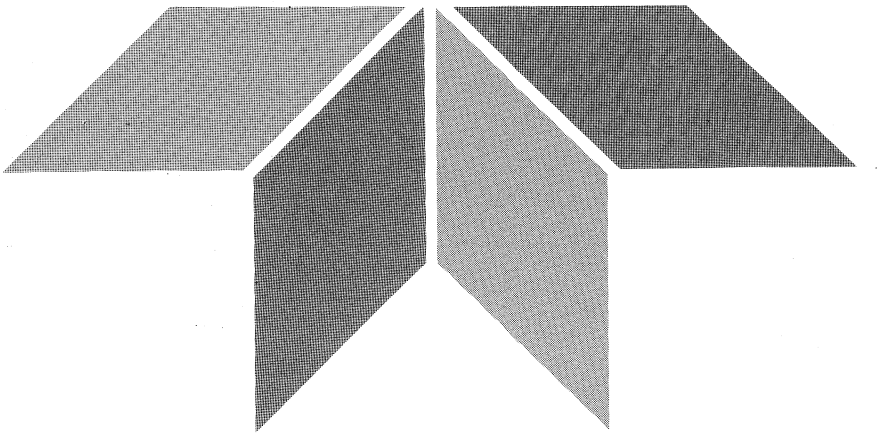
Semiconductor devices should not be left at high temperatures for a long time. Regardless of the soldering method, soldering must be done in a short time and at the lowest possible temperature. Soldering work must meet soldering heat test conditions, namely, 260° C for 10 seconds and 350° C for 3 seconds at a point 1 to 1.5 mm away from the end of the device package.

Use of a strong alkali or acid flux may corrode the leads, deteriorating device characteristics. The recommended soldering iron is the type that is operated with a secondary voltage supplied by a transformer and grounded to protect from lead current. Solder the leads at the farthest point from the device package.

Removing Residual Flux

To insure the reliability of electronic systems, residual flux must be removed from circuit boards. Detergent or ultrasonic cleaning is usually applied. If chloric detergent is used for the plastic molded devices, package corrosion may occur. Since cleaning over extended periods or at high temperatures will cause swollen chip coating due to solvent permeation, select the type of detergent and cleaning condition carefully. Do not use any trichloroethylene solvent. For ultrasonic cleaning, the following conditions are advisable:

- Frequency: 28 to 29 kHz (to avoid device resonation)
- Ultrasonic output: 15W/ℓ
- Keep the devices out of direct contact with the power generator.
- Cleaning time: Less than 30 seconds



SECTION 4

Alphanumeric Product List

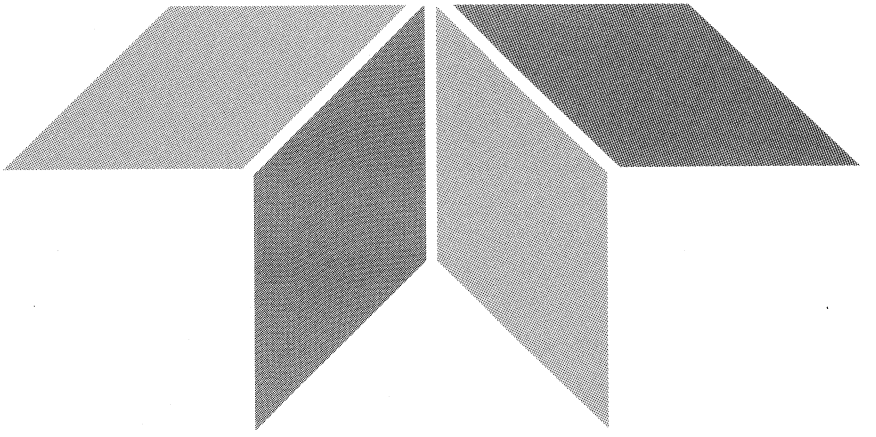
Section 4
Alphanumeric Product List 4-1

Alphanumeric Product List

TSC301	Power NAND Gates Dual 5-Input	14-15
TSC302	Power NAND Gates Quad 2-Input	14-15
TSC303	Power NAND Gates Quad 2-Input	14-15
TSC304	Power NAND Gates Triple 4, 3, 4-Input	14-15
TSC306	NOR Gate Quad 2, 2, 3, 3-Input	14-19
TSC307	NOR Gate Quad 2, 2, 3, 3-Input	14-19
TSC311	Flip Flops Master/Slave RST	14-21
TSC312	Flip Flops Dual J-K Edge Triggered	14-21
TSC313	Flip Flops Dual J-K Master/Slave	14-21
TSC321	NAND Gates Quad 2-Input	14-27
TSC322	NAND Gates Dual 5-Input	14-27
TSC323	NAND Gates Quad 2-Input	14-27
TSC324	NAND Gates Quad 2-Input	14-27
TSC325	NAND Gates 2, 2, 3, 3-Input	14-31
TSC326	NAND Gates 2, 2, 3, 3-Input	14-31
TSC331	Gate Expander Dual 5-input	14-35
TSC332	Hex Inverter Gates 4-Inverter, 2-NAND	14-37
TSC333	Hex Inverter Gates 4-Inverter, 2-NAND	14-37
TSC334	Hex Inverter Gates Strobed Hex NAND	14-37
TSC335	Hex Inverter Gates Strobed Hex NAND	14-37
TSC341	Multifunction Gates Dual 2-Wide, 2-Input and/or Invert	14-41
TSC342	Dual Monostable Multivibrator	14-45
TSC343	Digital Comparator 4-Bit	14-49
TSC347	Dual Retriggerable Monostable Multivibrator	14-53
TSC349	Dual Retriggerable Pulse Stretcher	14-57
TSC350	Multiplexers 8-Bit	14-61
TSC351	Multiplexers Dual 4-Bit	14-61
TSC355	Timer	14-65
TSC361	Dual 11-16 V to 5 V Interface Voltage Translator	14-69
TSC362	5 V to 11-16 V Interface Dual Transistor	14-71
TSC363	5 V to 11-16 V Interface Quad 2-Input NAND	14-71
TSC367	Schmitt Trigger Quad Active Pullup	14-75
TSC368	Schmitt Trigger Quad Open Collector	14-75
TSC370	Flip Flop Quad D	14-81
TSC371	Counters Decade	14-83
TSC372	Counters Hexadecimal	14-83
TSC373	Up-Down Counters Decade	14-87
TSC374	Up-Down Counters Hexadecimal	14-87
TSC375	Shift Register 4-Bit	14-91
TSC380	BCD-to-Decade Decoder/Drivers Lamp Driver	14-95
TSC381	BCD-to-Decade Decoder/Drivers Logic Driver	14-95
TSC382	BCD-to-Decade Decoder/Drivers Gas Tube Driver	14-99
TSC383	Decoder/Driver BCD-to-7 Segment	14-103
TSC390	Dual Interface Buffers 4-Input Expandable AND	14-107
TSC391	Dual Interface Buffers 2-Input AND	14-107
TSC392	Dual Interface Buffers 2-Input NAND	14-107
TSC393	Dual Interface Buffers 2-Input OR	14-107
TSC394	Dual Interface Buffers 2-Input NOR	14-107
TSC395	Dual Interface Buffers 4-Input Expandable NAND	14-107
TSC396	Line Driver Receiver Dual Differential	14-111
TSC426	High Speed Dual Power MOSFET Driver	6-3
TSC427	High Speed Dual Power MOSFET Driver	6-3
TSC428	High Speed Dual Power MOSFET Driver	6-3
TSC450	Dual Power MOSFET Driver	11-3
TSC500	Precision Analog Processor	6-5
TSC700A	High Current Four Digit LED Driver	10-3
TSC701AM	High Current Bus Compatible Four Digit LED Driver	10-11
TSC800	15-Bit Plus Sign Integrating A/D Converter	8-23
TSC805	Auto-Ranging Instrumentation A/D Converter	6-7
TSC826	LCD Bar Graph Display A/D Converter	6-9

Alphanumeric Product List

TSC841	4 1/2 Digit A/D Converter	6-11
TSC7106A/7107A	(LCD Drive) 3 1/2 Digit A/D Converter	7-3
TSC7106/TSC7107	(LED Drive) 3 1/2 Digit A/D Converter	7-21
TSC7109	12-Bit Plus Sign Integrating A/D Converter	8-3
TSC7116A/7117A	(LCD Drive) 3 1/2 Digit A/D Converter	7-33
TSC7116/7117	(LED Drive) 3 1/2 Digit A/D Converter	7-45
TSC7126A	3 1/2 Digit A/D Converter	7-57
TSC7126	3 1/2 Digit A/D Converter	7-69
TSC7135	4 1/2 Digit Precision A/D Converter	7-81
TSC7211A	Four Digit LCD Driver	10-19
TSC7212A	Four Digit LED Driver	10-19
TSC7211AM	Bus Compatible Four Digit LCD Driver	10-31
TSC7212AM	Bus Compatible Four Digit LED Driver	10-31
TSC7650	Precision Chopper - Stabilized Operational Amplifier	13-3
TSC7660	DC to DC Voltage Converter	11-7
TSC8700 (8-Bit)	Binary Output ADC	8-39
TSC8701 (10-Bit)	Binary Output ADC	8-39
TSC8702 (12-Bit)	Binary Output ADC	8-39
TSC8703 (8-Bit)	Three State Binary Output ADC	8-51
TSC8704 (10-Bit)	Three State Binary Output ADC	8-51
TSC8705 (12-Bit)	Three State Binary Output ADC	8-51
TSC8750	3 1/2 Digit ADC w/Parallel BCD Output	7-93
TSC9400	V/F Converter (0.05% Linearity)	9-3
TSC9401	V/F Converter (0.01% Linearity)	9-3
TSC9402	V/F Converter (0.25% Linearity)	9-3
TSC9403	Serial Input/16-Bit Parallel Output Peripheral Driver	11-17
TSC9404	Serial Input/16-Bit Parallel Output Peripheral Driver	11-17
TSC9491	1.22 V Bandgap Reference	12-3
TSC9495	+5 V Bandgap Voltage Reference/Temperature Transducer	12-5
TSC9496	+10 V Bandgap Voltage Reference	12-9
TSC14433A	Precision 3 1/2 Digit ADC	7-101
TSC14433B	Low Cost 3 1/2 Digit ADC	7-107
TSC14433	3 1/2 Digit ADC	7-113



SECTION 5

Cross Reference Guide

Section 5
Cross Reference Guide 5-1

3 1/2 Digit LCD Drive ADC

Teledyne Semiconductor Part No.*	Manufacturer Part No.	Manufacturer Part No.	Manufacturer Part No.
TSC7106CJL	ICL7106CJL		
TSC7106CPL	ICL7106CPL		
TSC7106IJL			
TSC7106IPL			
TSC7106RCPL	ICL7106RCPL		

* See TSC7106A for improved pin compatible device

3 1/2 Digit LED Drive ADC

Teledyne Semiconductor Part No.*	Manufacturer Part No.	Manufacturer Part No.	Manufacturer Part No.
TSC7107CJL	ICL7107CJL		
TSC7107CPL	ICL7107CPL		
TSC7107IDL			
TSC7107IJL			
TSC7107IPL			
TSC7107RCPL	ICL7107RCPL		

* See TSC7107A for improved pin compatible device

3 1/2 Digit Low Power LCD Drive ADC

Teledyne Semiconductor Part No.*	Manufacturer Part No.	Manufacturer Part No.	Manufacturer Part No.
TSC7126CJL	ICL7126CJL		
TSC7126CPL	ICL7126CPL		
TSC7126IJL			
TSC7126RCPL			

* See TSC7126A for improved pin compatible device

12-Bit Plus Sign Integrating ADC

Teledyne Semiconductor Part No.*	Manufacturer Part No.	Manufacturer Part No.	Manufacturer Part No.
TSC7109CPL	ICL7109CPL		
TSC7109IJL	ICL7109IJL		
TSC7109MJL	ICL7109MJL		

* See TSC7109B for low cost pin compatible device

3 1/2 Digit LCD Drive ADC With Display Hold

Teledyne Semiconductor Part No.*	Manufacturer Part No.	Manufacturer Part No.	Manufacturer Part No.
TSC7116CJL	ICL7116CJL		
TSC7116CPL	ICL7116CPL		
TSC7116IJL			
TSC7116IPL			

* See TSC7116A for improved pin compatible device

3 1/2 Digit LED Drive ADC With Display Hold

Teledyne Semiconductor Part No.*	Manufacturer Part No.	Manufacturer Part No.	Manufacturer Part No.
TSC7117CJL	ICL7117CJL		
TSC7117CPL	ICL7117CPL		
TSC7117IJL			
TSC7117IPL			

* See TSC7117A for improved pin compatible device

4 1/2 Digit Multiplexed BCD Data Output ADC

Teledyne Semiconductor Part No.	Manufacturer Part No.	Manufacturer Part No.	Manufacturer Part No.
TSC7135CJI	ICL7135CJI		
TSC7135CPI	ICL7135CPI		

3 1/2 Digit Multiplexed BCD Data Output ADC

Teledyne Semiconductor Part No.*	Manufacturer Part No.	Manufacturer Part No.	Manufacturer Part No.
TSC14433ACJ	MC14433P		
TSC14433ACL	MC14433L		
TSC14433ACN	MC14433L		
TSC14433CJ	MC14433P		
TSC14433CN	MC14433L		
TSC14433CL	MC14433L		

* "A" version gives improved rollover performance. See TSC14433B for low cost version.

Four Digit LCD Display Driver/Decoders

Teledyne Semiconductor Part No.	Manufacturer Part No.	Manufacturer Part No.	Manufacturer Part No.
TSC7211AIPL	ICM7211AIPL	CD22104AE	HLCD7211-2

Four Digit LED Display Driver/Decoders

Teledyne Semiconductor Part No.*	Manufacturer Part No.	Manufacturer Part No.	Manufacturer Part No.
TSC7212AIPL	ICM7212AIPL		

*See TSC700A for improved pin compatible device

Four Digit Bus Compatible LCD Display Driver/Decoders

Teledyne Semiconductor Part No.	Manufacturer Part No.	Manufacturer Part No.	Manufacturer Part No.
TSC7211AMIPL	ICM7211AMIPL	CD22105AE	HLCD7211-4

Four Digit Bus Compatible LED Display Driver/Decoders

Teledyne Semiconductor Part No.*	Manufacturer Part No.	Manufacturer Part No.	Manufacturer Part No.
TSC7212AMIPL	ICM7212AMIPL		

* See TSC701AM for improved pin compatible device

Voltage References

Teledyne Semiconductor Part No.	Manufacturer Part No.	Manufacturer Part No.	Manufacturer Part No.
TSC9491AJ	ICL8069CCZR		
TSC9491IAM	ICL8069CMSQ		
TSC9491BJ	ICL8069DCZR		
TSC9491IBM	ICL8069DMSQ		
TSC9495CJ		MP5531C	REF02CP
TSC9496CJ		MP5532C	REF01CP

Voltage-To-Frequency & Frequency-To-Voltage Converters

Teledyne Semiconductor Part No.	Manufacturer Part No.	Manufacturer Part No.	Manufacturer Part No.
TSC9400CJ	4780	VFQ-1C	
TSC9400CL		VFQ-1R	
TSC9401CJ	4781		

Precision Operational Amplifiers

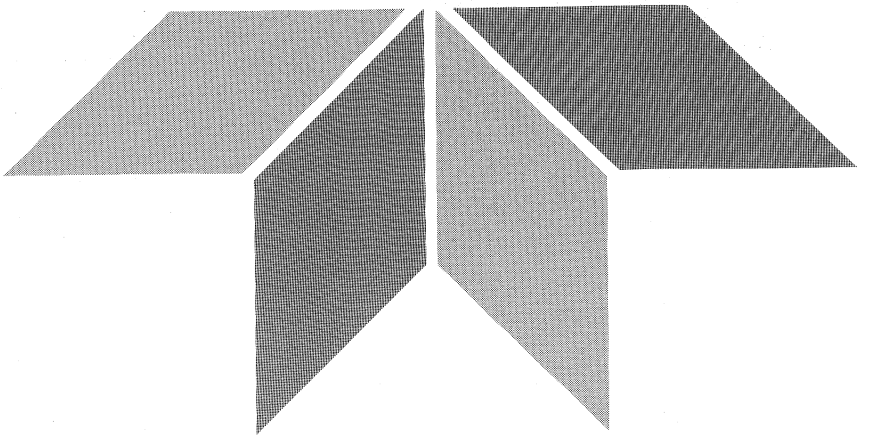
Teledyne Semiconductor Part No.	Manufacturer Part No.	Manufacturer Part No.	Manufacturer Part No.
TSC7650CPD	ICL7650CPD		
TSC7650IJD	ICL7650IJD		

DC To DC Voltage Converters

Teledyne Semiconductor Part No.	Manufacturer Part No.	Manufacturer Part No.	Manufacturer Part No.
TSC7660CPA	ICL7660CPA		

8/10/12-Bit Binary Output ADC

Teledyne Semiconductor Part No.	Manufacturer Part No.	Manufacturer Part No.	Manufacturer Part No.
TSC8700CJ	ADC-EK8B		
TSC8701CJ	ADC-EK10B		
TSC8702CN	ADC-EK12B		
TSC8750CJ	ADC-EK12DC		
TSC8750BN	ADC-EK12DM		
TSC8750CN	ADC-EK12DR		
TSC8703CJ	ADC-ET8BC		
TSC8703BL	ADC-ET8BM		
TSC8703CL	ADC-ET8BR		
TSC8704CJ	ADC-ET10BC		
TSC8704BN	ADC-ET10BM		
TSC8704CN	ADC-ET10BR		
TSC8705CJ	ADC-ET12BC		
TSC8705BN	ADC-ET12BM		
TSC8705CN	ADC-ET12BR		



SECTION 6

Advance Product Information

Section 6
Advance Product Information 6-1

TSC426/427/428	High Speed Dual Power MOSFET Driver	6-3
TSC500	Precision Analog Processor	6-5
TSC805	Auto-Ranging Instrumentation A/D Converter	6-7
TSC826	LCD Bar Graph Display A/D Converter	6-9
TSC841	4 1/2 Digit A/D Converter	6-11

Advance Product Information

TSC426/427/428
Dual Power MOSFET Driver
• 1.5 Amp Peak Drive Current
• 50 ns Rise Time

General Description

The TSC426/427/428 are dual high speed power MOSFET drivers. Each device converts CMOS/TTL input levels to a high voltage level drive signal. Switching times of 50 ns are typical with 1000 pf loads. Peak output drive current is 1.5 amp. Delay times have been matched for both inverting and non-inverting stages.

The TSC428 contains an inverting and non-inverting driver. The TSC426 is inverting and TSC427 non-inverting.

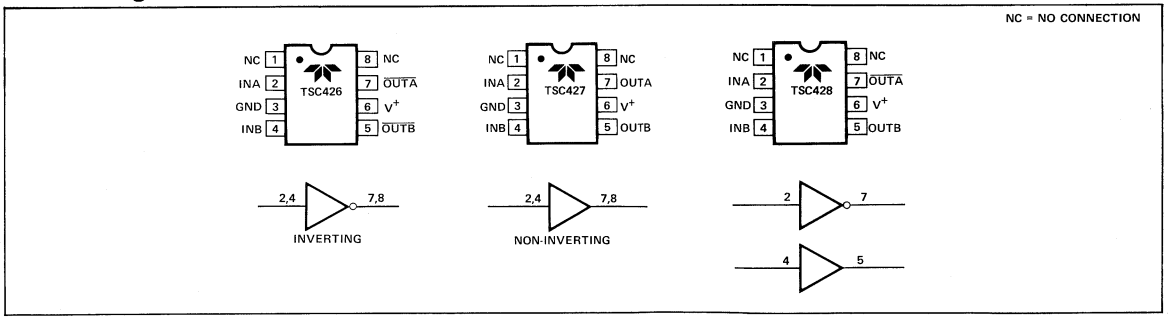
Features

- CMOS Construction for Low Current Drain ..... 6 mA
- High Output Voltage ..... V_S -0.05 V
- High Peak Current Drive ..... 1.5 A
- High Speed Switching (C_H = 1000 pF) ..... 50 ns
- Available as Inverting/Non-Inverting Driver
- Wide Supply Voltage Operation ..... 4.5 to 20 V
- TTL/CMOS Compatible Input Drive
- Pin-Out Equivalent to DS0026

Preliminary Ordering Information

Ordering Part No.	Operating Temp. Range	Package	Configuration	Peak Output Current	Rise Time (C_L = 1000 pF)
TSC426CPA	0° C to 70° C	8-Pin Plastic Dip	Inverting	1.5 A	50 ns
TSC426IJA	-25° C to 85° C	8-Pin CerDIP	Inverting	1.5 A	50 ns
TSC426MJA	-55° C to 125° C	8-Pin CerDIP	Inverting	1.5 A	50 ns
TSC427CPA	0° C to 70° C	8-Pin Plastic Dip	Non-Inverting	1.5 A	50 ns
TSC427IJA	-25° C to 85° C	8-Pin CerDIP	Non-Inverting	1.5 A	50 ns
TSC427MJA	-55° C to 125° C	8-Pin CerDIP	Non-Inverting	1.5 A	50 ns
TSC428CPA	0° C to 70° C	8-Pin Plastic Dip	Non-Inv. & Inv.	1.5 A	50 ns
TSC428IJA	-25° C to 85° C	8-Pin CerDIP	Non-Inv. & Inv.	1.5 A	50 ns
TSC428MJA	-55° C to 125° C	8-Pin CerDIP	Non-Inv. & Inv.	1.5 A	50 ns

Pin Configuration



TELEDYNE SEMICONDUCTOR

Advance Product Information

TSC500
Precision Analog Processor
• Low Power CMOS
• Precision Internal Reference
• Auto-Zero Cycle

General Description

The TSC500 is a precision integrating analog-to-digital converter building block. The converter control logic can be implemented with a microprocessor and software routine or with discrete logic.

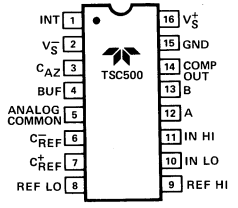
On-chip are the analog input buffer, integrator, comparator, voltage reference, analog switches and drivers, and phase control logic. A precision dual slope integrating converter with automatic zero scale offset voltage and drift correction requires only external resistors and capacitors. A zero integrator output cycle makes the converter quickly recover from an overrange input signal.

Accuracies of one part in 20,000 are easily achieved with the low power CMOS TSC500. The differential analog inputs feature a $10^{12}\Omega$ input impedance and a 10 pA leakage current. The reference voltage is also differential making ratiometric measurements possible.

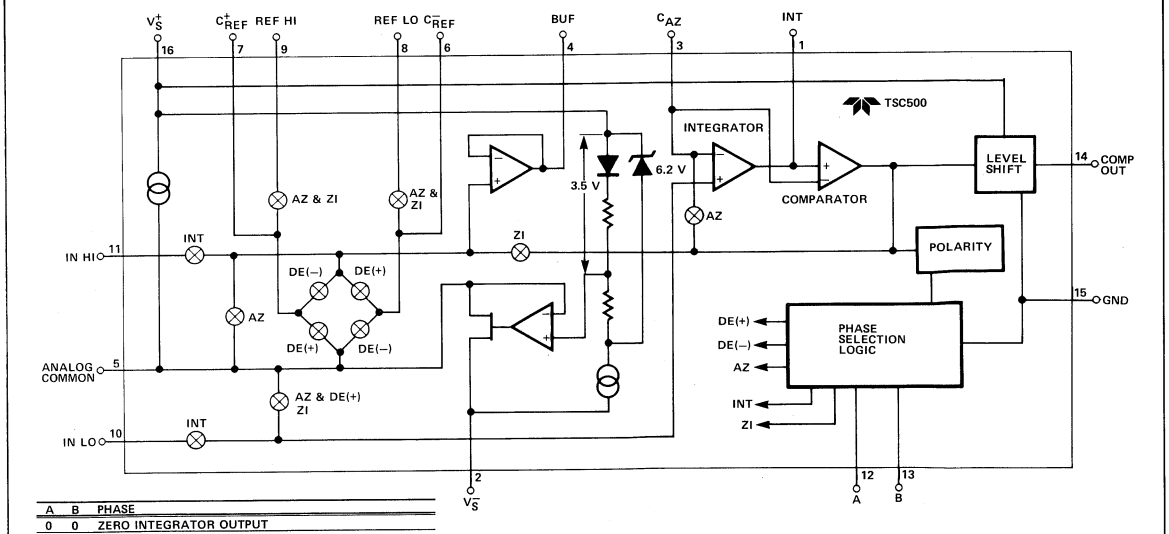
Features

- High Linearity 0.005%
- Auto-Zero Cycle Eliminates Zero Scale Error and Drift
- Differential Reference Input for Ratiometric Measurements
- Differential Analog Input
- Fast Recovery From Input Overload
- Automatic Polarity Detection
- Low Drift Internal Voltage Reference . 50 ppm/°C Max.
- Low Power CMOS Construction ..... 10 mW
- Low Input Current ..... 10 pA
- Microprocessor Control of Analog Cycles
- Wide Analog Input Voltage Range ..... ±4.5 V

Pin Configuration



Functional Diagram



A	B	PHASE
0	0	ZERO INTEGRATOR OUTPUT
0	1	AUTO-ZERO (ZERO SCALE OFFSET/DRIFT CORRECTION)
1	0	SIGNAL INTEGRATE
1	1	DEINTEGRATE (REFERENCE VOLTAGE INTEGRATE)

TELEDYNE SEMICONDUCTOR

TSC805
Auto-Ranging Instrumentation Analog-to-Digital Converter
- 3 1/2 Digit Resolution
- Tri-Plex LCD Drive
- AC & DC Measurements

Advance Product Information

General Description

The TSC805 is a 3 1/2 digit integrating analog-to-digital converter with tri-plex LCD display drive and automatic ranging. The CMOS TSC805 contains all the logic and analog switches needed to manufacture an auto-ranging instrument for ohms and voltage measurements.

The auto-ranging feature automatically selects the proper display decimal point location. Auto-ranging is available during ohms (high and low voltage) and voltage (AC & DC) measurements. Auto-ranging eliminates expensive range switches in hand-held DMM designs and makes compact meters easier and less costly to design. Auto-ranging instruments are easy to operate and are ideal for non-technical end users. The auto-range feature may be bypassed allowing decimal point selection and input attenuator selection control through a single line input.

The TSC805 includes an AC to DC converter for AC audio frequency range measurements. Only inexpensive external diodes/resistors/capacitors are required.

A complete LCD annunciator set visually describes the TSC805 meter function and measurement range during ohms, voltage and current operation. AC or DC measurements are indicated. A low battery detection circuit also sets a low battery warning display annunciator.

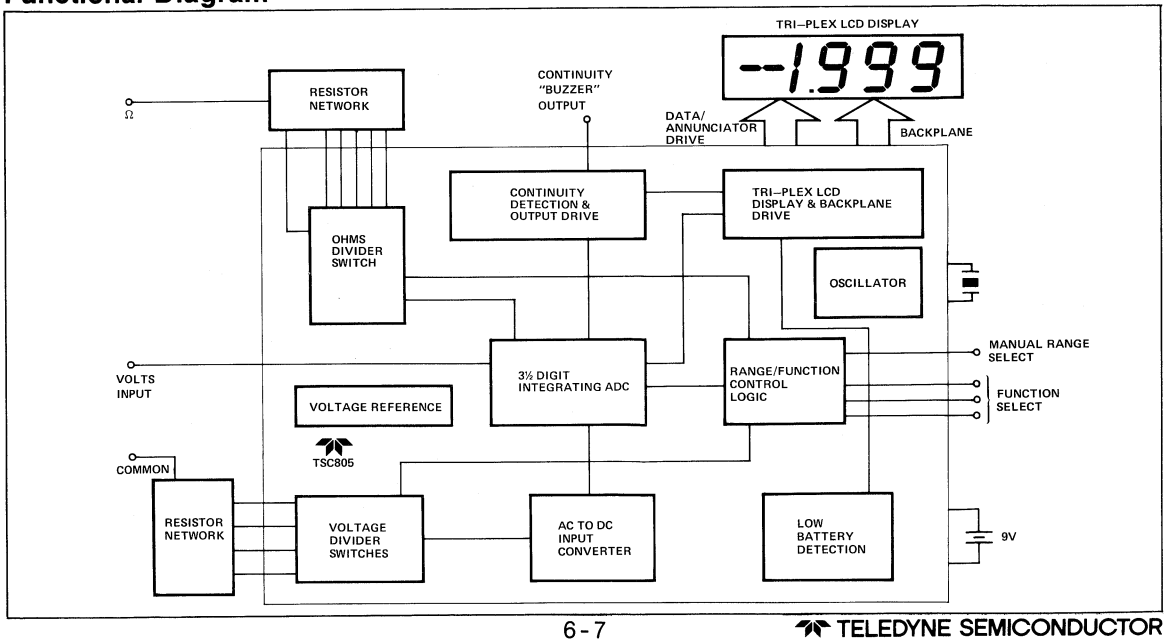
Features

- Auto-Ranging on volts (AC & DC) and Ohms Scale
- Automatic Sign, Function and Unit Display
- AC to DC Voltage Converter on Chip
- Low Voltage Ohms Range Option
- Continuity Detection & "Buzzer" Drive Output
- 3 1/2 Digit Resolution on 200 mV Full-Scale Range
- Low Noise Input Stage ..... 15 μVp-p
- Precision Internal Reference ..... 50 ppm/°C Max.
- Triplex LCD Drivers On Chip
- Low Battery Detection & LCD Annunciator
- Convenient 9 V Battery Operation
- Low Power Consumption ..... 10 mW
- Compact 60-Pin Flat Package

The "low ohms" measurement option allows in circuit resistance measurements by preventing semiconductor junctions from being forward biased. A zero ohms adjust is included to compensate for lead resistance.

A continuity buzzer output is activated with inputs less than 5% of full-scale. An overrange input also enables the buzzer and flashes the MSD display. Offering single 9 V battery operation, 10 mW power consumption, a precision internal voltage reference (50 ppm/°C max. TC) and available in a compact 60-pin flat package the TSC805 is ideal for portable instruments.

Functional Diagram



TELEDYNE SEMICONDUCTOR

Advance Product Information

TSC826
LCD Bar Graph Display Analog-to-Digital Converter
- 2.5% Resolution
- 1 mW Power Dissipation
- Direct LCD Drive

General Description

The TSC826 is a CMOS analog-to-digital converter that directly drives liquid crystal bar graph displays. LCD drivers are on-chip for forty data segment, zero, polarity, and overrange annunciators. A backplane oscillator and driver are included. All active components are on-chip for a 2.5% resolution bar graph display. Up to 16 conversions per second are possible.

An auto-zero cycle guarantees a zero display for zero volt input. No adjustment potentiometers are needed. The precision internal reference with a 35 ppm/° C temperature coefficient virtually eliminates full scale errors over temperature.

The CMOS TSC826 draws less than 100 μA from a 9 V battery guaranteeing long life in portable applications. Available in a 60-pin flat package compact portable designs with multiple bar graph indicators are possible.

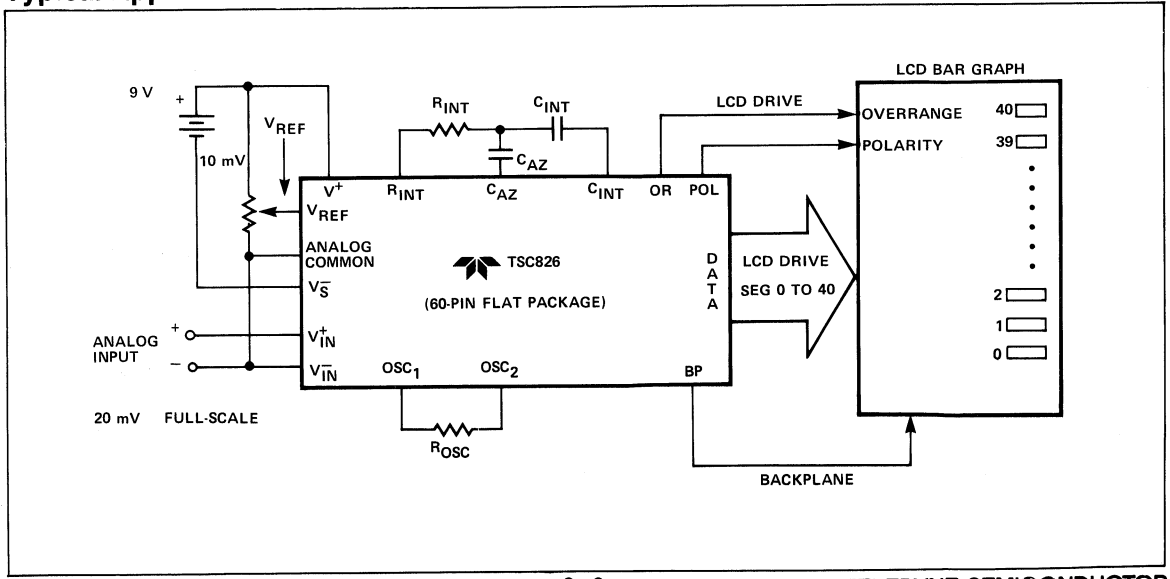
Features

- Bar Graph Data Display . . . 40 Segments plus zero
- Overrange Plus Polarity Indication
- Precision On-Chip Reference . . . 35 ppm/° C
- Auto-Zero Cycle Eliminates Zero Adjust Potentiometer
- Low Power Consumption . . . 1 mW
- Differential Analog Input
- LCD Drivers and Backplane Oscillator
- 9 V Battery Operation
- 20 mV Full-Scale Operation
- Compact Flat Package

Preliminary Ordering Information

Part No.	Package	Temperature Range
TSC826IBQ	60-Pin Plastic Flat Package (Formed Leads)	-40° C to +85° C

Typical Application



Advance Product Information

TSC841
4 1/2 Digit A/D Converter
• Tri-Plex LCD Display Drive
• 200 mV Full-Scale

General Description

The TSC841 is a 4 1/2 digit analog-to-digital converter that directly drives a tri-plex liquid crystal display. Featuring a 200 mV full-scale, the TSC841 gives 10 μV resolution with 0.005% full-scale accuracy.

The TSC841 is a dual slope integrating converter incorporating four phases: auto-zero, signal integrate, reference deintegrate and integrator zero. The auto-zero phase eliminates zero-scale error. A zero reading is guaranteed with a zero volt input. The integrator zero phase speeds recovery from overrange input signals by removing excess charge stored on the auto-zero capacitor.

The TSC841 minimizes the effective input noise by using digital averaging. Six conversions are averaged to generate the displayed output. Each of the six conversions take 67 msec making a display/measurement cycle 400 msec long (2.5 conv/sec). Input noise is reduced to 3 μVp-p.

A multiplexed LCD display drive format allows the TSC841 to be packaged in both 40-pin dip and 60-pin flat packages. Besides providing drive for four seven segment digits, the half digit, minus sign, and low battery warning indicator eight user selected annunciators are available. These are selected by two, 2-bit input codes and can be used to drive decimal points or function annunciators (volts, amperes, ohms, AC, frequency, etc.).

The TSC841 also includes a digital continuity output that is enabled whenever the digital display <100. Overrange, underrange and busy digital output signals can be used to design an auto-ranging 4 1/2 digit ADC. An internal low battery detection/annunciator drive signal warns the user when a new battery is needed.

An internal reference removes the need for an external active component. A complete 4 1/2 digit, 10 μV resolution measurement system can be constructed with six external R/C components, a 9 V battery, a crystal and an inexpensive tri-plex LCD display.

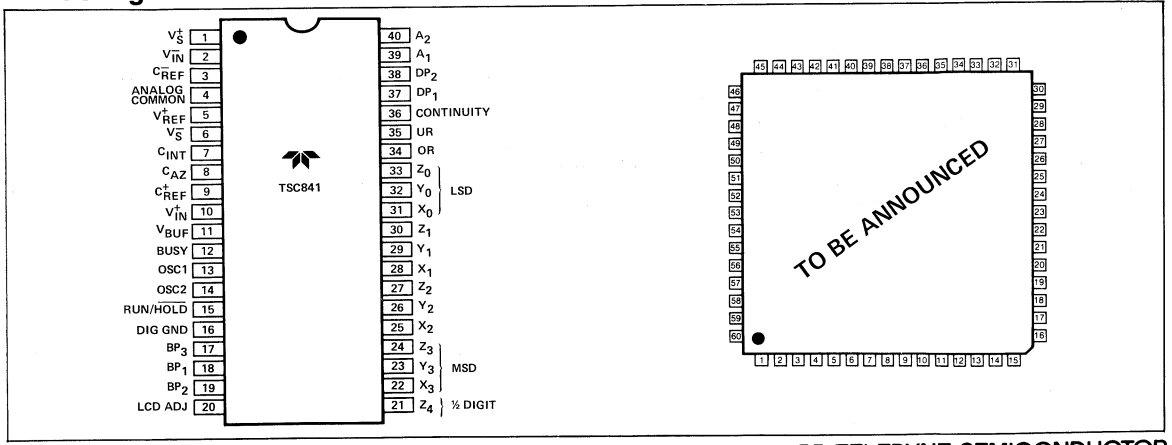
Features

- 4 1/2 Digit (50 ppm) Resolution
- 200 mV and 2 V Full-Scale Range
- 10 μV Resolution
- Ten Times More Accurate Than 3 1/2 Digit Devices
- Precision Internal Reference ..... 15 ppm/°C
- Low Input Noise ..... 3 μV_{P-P}
- Full 4 1/2 Digit Triplex LCD Drive
  - — Four Seven Segment Digits
  - — Half Digit Plus Polarity
  - — Four Decimal Points
  - — Low Battery Warning
  - — Four User Defined & Selected Annunciators
- Overrange/Underrange Signals for Auto-Ranging
- Differential Analog Input
- 9 V Battery Operation
- High Impedance CMOS Inputs ..... $10^{12}\Omega$
- Low Input Leakage Current ..... 5 pA
- High Speed Continuity Detection for Audio "Buzzer" Drive ..... <50 msec
- Low Battery Detection & Annunciator
- Guaranteed Zero Reading With Zero Input

Ordering Information

Part No.	Package	Temp. Range
TSC841CPL	40-Pin Plastic Dip	COM
TSC841CJL	40-Pin CerDIP	COM
TSC841CBQ	60-Pin Plastic Flat Package: Formed Leads	COM
TSC841SBQ	60-Pin Plastic Flat Package: Unformed Leads	COM

Pin Configuration



Absolute Maximum Ratings

Supply Voltage (V^+ to V^-) ..... 15 V
Analog Input Voltage (either input) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Power Dissipation
CerDIP Package (J) ..... 1000 mW
Plastic Package (P) ..... 800 mW
Epoxy Flat Package (B, S) ..... 800 mW

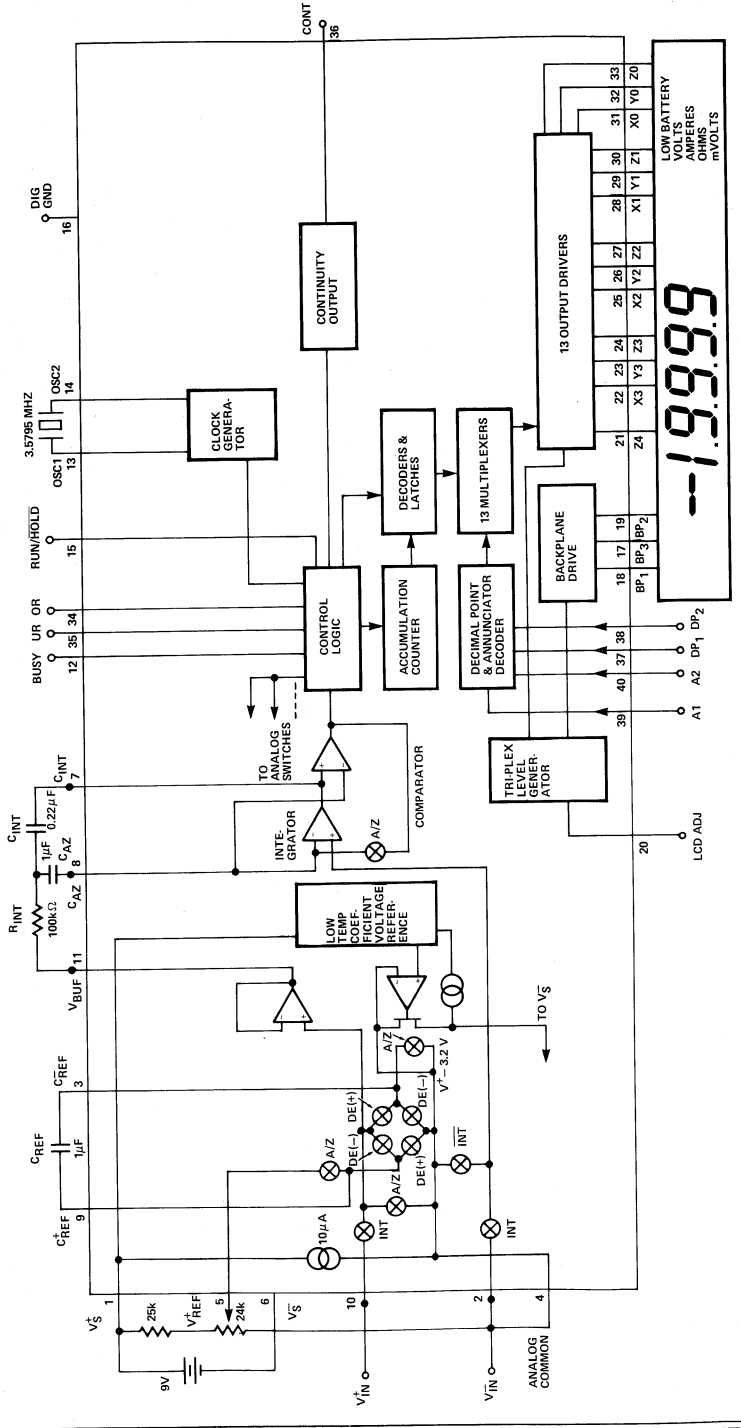
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300 °C

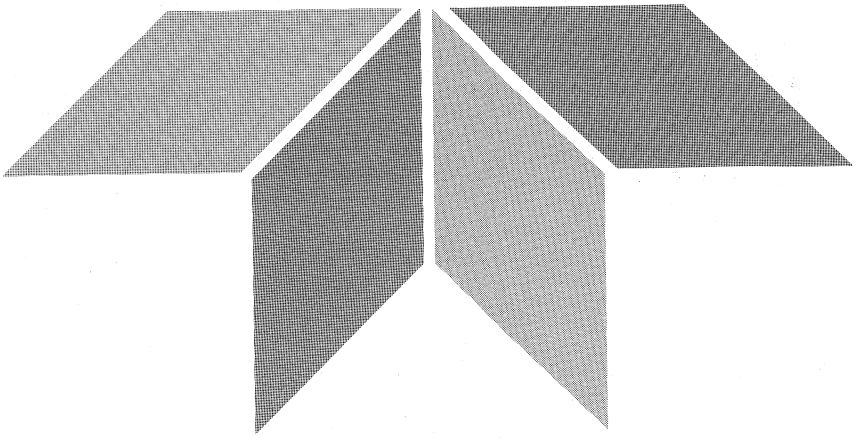
Electrical Characteristics: V_S = 9 V, f_{XTAL} = 3.5785 MHz and T_A = 25° C unless otherwise noted. V_{IN} = 200 mV.

TYPE	NO.	SYMBOL	PARAMETER	TSC841 MIN	TSC841 TYP	TSC841 MAX	UNIT
INPUT	1	—	Zero Input Reading	-00000	±00000	+00000	Digital Reading
	2	—	Zero Reading Drift	—	0.2	1	μV/° C
	3	NL	Linearity Error	—	±0.2	—	Counts
	4	—	Rollover Error	-1	±0.2	+1	Counts
	5	E_N	Noise	—	3	—	μV_{P-P}
	6	I_L	Input Leakage Current	—	5	—	pA
	7	CMRR	Common-Mode Rejection Ratio	—	50	—	μV/V
	8	—	Scale Factor Temperature Coefficient	—	1	5	ppm/° C
ANALOG COMMON	9	V_{CTC}	Analog Common Temperature Coefficient	—	15	—	ppm/° C
	10	V_C	Analog Common Temperature (Below V^+)	—	3.20	—	V
DRIVE	11	V_{SD}	LCD Segment Drive Voltage	—	5	—	V_{P-P}
	12	V_{BD}	LCD Backplane Drive Voltage	—	5	—	V_{P-P}
SUPPLY	13	I_S	Power Supply Current	—	5	—	mA

4 1/2 Digit A/D Converter

- Tri-Plex LCD Display Drive
- 200 mV Full-Scale





SECTION 7

Display Analog-to-Digital Converters

Section 7
Display A/D Converters 7-1

TSC7106A/7107A	(LCD Drive) 3 1/2 Digit A/D Converter	7-3
TSC7106/TSC7107	(LED Drive) 3 1/2 Digit Converter	7-21
TSC7116A/7117A	(LCD Drive) 3 1/2 Digit A/D Converter	7-33
TSC7116/7117	(LED Drive) 3 1/2 Digit A/D Converter	7-45
TSC7126A	3 1/2 Digit A/D Converter	7-57
TSC7126	3 1/2 Digit A/D Converter	7-69
TSC7135	4 1/2 Digit Precision A/D Converter	7-81
TSC8750	3 1/2 Digit ADC w/Parallel BCD Output	7-93
TSC14433A	Precision 3 1/2 Digit ADC	7-101
TSC14433B	Low Cost 3 1/2 Digit ADC	7-107
TSC14433	3 1/2 Digit ADC	7-113

TELEDYNE SEMICONDUCTOR

TSC7106A (LCD Drive)
TSC7107A (LED Drive)
3 1/2 Digit A/D Converter
• Low Drift Internal Reference
• Automatic Zero Correction

General Description

The TSC7106A and TSC7107A 3 1/2 digit direct display drive analog-to-digital converters allow existing 7106/7107 based systems to be upgraded. Each device offers a precision internal voltage reference featuring a 20 ppm/° C typical, 50 ppm° C maximum temperature drift coefficient. This represents a 4 to 7 times improvement over similar 3 1/2 digit converters. Existing 7106 or 7107 based systems may be upgraded without changing external passive component values. The need for a costly, space consuming external reference is removed. The TSC7107A drives common anode light emitting diode (LED) displays directly with an 8 mA drive current per segment. A low cost, high resolution indicating meter requires only a display, four resistors, and four capacitors. The TSC7106A low power drain and 9 V battery operation make it suitable for portable applications.

The TSC7106A/TSC7107A reduces linearity error to less than 1 count. Rollover error — the difference in readings for equal magnitude but opposite polarity input signals — is below ± 1 count. High impedance differential inputs offer 1 pA leakage current and a 10^{12} Ω input impedance. The differential reference input allows ratiometric measurements for ohms or bridge transducer measurements. The 15 μVp-p noise performance guarantees a "rock solid" reading. The auto-zero cycle guarantees a zero display reading with a zero volt input.

The TSC7106A/TSC7107A dual slope conversion technique automatically rejects interference signals if the converters integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400 Hz line frequency signals are present.

The TSC7106A/TSC7107A are available in a small 60-pin flat package for compact designs. DIP devices are offered in an industrial temperature range and with burn-in lasting for 160 hours at +125° C.

Where long battery life is needed see the TSC7126 or the TSC7126A data sheets.

Features

- Internal Reference with Low Temperature Drift ..... 20 ppm/° C Typical, 50 ppm/° C Maximum
- Drives LCD or LED Displays Directly
- Guaranteed Zero Reading with Zero Input
- Low Noise for Stable Display
- Auto-Zero Cycle Eliminates Need for Zero Adjustment
- True Polarity Indication for Precision Null Applications
- Convenient 9 V Battery Operation (TSC7106A)
- High Impedance CMOS Differential Inputs ..... 10^{12} Ω
- Differential Reference Inputs Simplify Ratiometric Measurements
- Low Power Operation ..... 10 mW
- Available in 60-Pin Plastic Flat Package

7

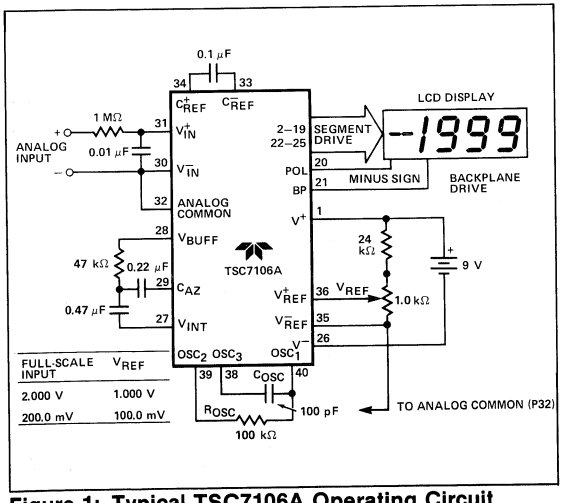
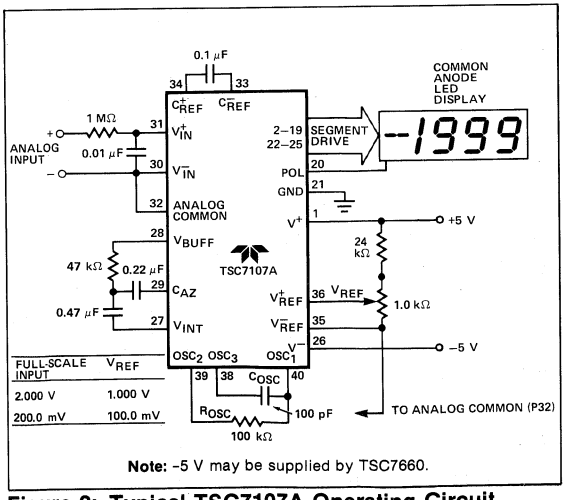


Figure 1: Typical TSC7106A Operating Circuit



Note: -5 V may be supplied by TSC7660.

Figure 2: Typical TSC7107A Operating Circuit

Absolute Maximum Ratings

TSC7106A

Supply Voltage (V^+ to V^-) ..... 15 V
Analog Input Voltage (either input) (Note 1) .... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... Test to V^+
Power Dissipation (Note 2)
  CerDIP Package ..... 1000 mW
  Plastic Package ..... 800 mW
Operating Temperature
  "C" Devices ..... 0°C to +70°C
  "I" Devices ..... -25°C to +85°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may effect device reliability.

TSC7107A

Supply Voltage
  V^+ ..... +6 V
  V^- ..... -9 V
Analog Input Voltage (either input) (Note 1) .... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... GND to V^+
Power Dissipation (Note 2)
  CerDIP Package ..... 1000 mW
  Plastic Package ..... 800 mW
Operating Temperature
  "C" Devices ..... 0°C to +70°C
  "I" Devices ..... -25°C to +85°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Electrical Characteristics (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	V_{IN} = 0.0 V Full-Scale = 200.0 mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in Reading for Equal Positive and Negative Reading Near Full-Scale)	$-V_{IN} = +V_{IN} \simeq$ 200.0 mV	-1	±0.2	+1	Counts
Linearity (Max. Deviation From Best Straight Line Fit)	Full-Scale = 200 mV or Full-Scale = 2.000 V	-1	±0.2	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1 V, V_{IN} = 0 V. Full-Scale = 200.0 mV	—	50	—	μV/V
Noise (Pk - Pk Value Not Exceeded 95% of Time)	V_{IN} = 0 V Full-Scale = 200.0 mV	—	15	—	μV
Leakage Current @ Input	V_{IN} = 0 V	—	1	10	pA
Zero Reading Drift	V_{IN} = 0 V "C" Device = 0°C to 70°C V_{IN} = 0 V "I" Device = -25°C to +85°C	— —	0.2 1.0	1 2	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0 mV, "C" Device = 0°C to 70°C (Ext. Ref = 0 ppm/°C) V_{IN} = 199.0 mV "I" Device: -25°C to +85°C	— —	1 —	5 20	ppm/°C ppm/°C
Supply Current (Does Not Include LED Current for TSC7107A)	V_{IN} = 0	—	0.8	1.8	mA
Analog Common Voltage (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply	2.7	3.05	3.35	V
Temp. Coeff. of Analog Common (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply 0°C ≤ T_A ≤ 70°C "C," Commercial Temp. Range Devices	—	20	50	ppm/°C
Temp. Coeff. of Analog Common (with Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply -25°C ≤ T_A ≤ 85°C "I," Industrial Temp. Range Devices	—	—	75	ppm/°C
TSC7106A ONLY Pk - Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V

Electrical Characteristics (Note 3)

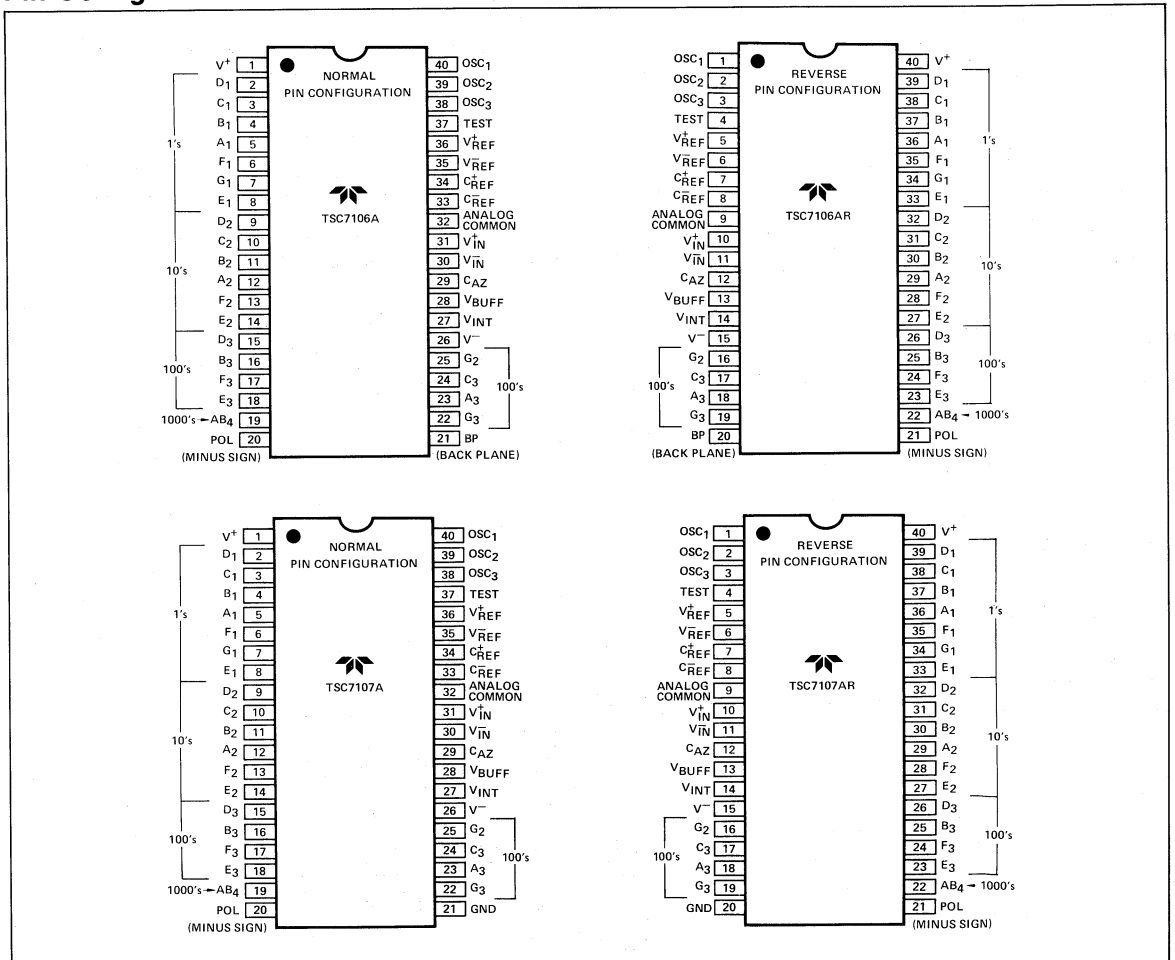
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
TSC7106A ONLY Pk - Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V
TSC7107A ONLY Segment Sinking Current (Except Pin 19)	V^+ = 5.0 V Segment Voltage = 3 V	5	8.0	—	mA
TSC7107A ONLY Segment Sinking Current (Pin 19 Only)	V^+ = 5.0 V Segment Voltage = 3 V	10	16	—	mA

NOTES:

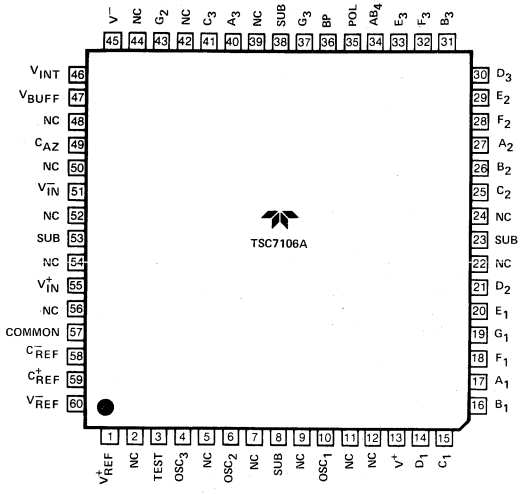
1. Input voltages may exceed the supply voltages provided the input current is limited to ± 100 μA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Unless other wise noted, specifications apply to both the TSC7106A and TSC7107A at T_A = 25° C, f_{CLOCK} = 48 kHz. TSC7106A is tested in the circuit of Figure 1. TSC7107A is tested in the circuit of Figure 2.
4. Refer to "Differential Input" discussion.
5. Backplane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average dc component is less than 50 mV.

7

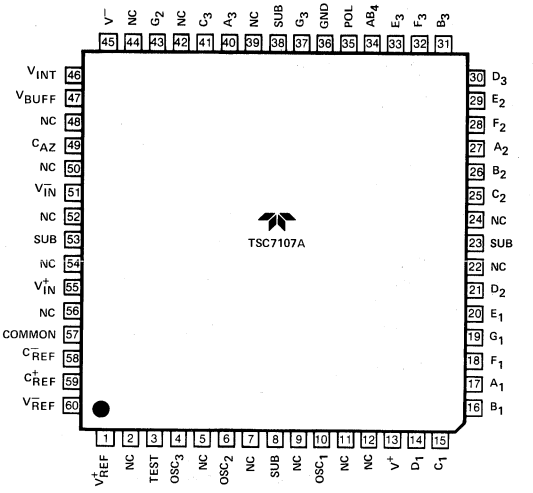
Pin Configuration



Pin Configuration (Cont.)



Notes:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V^+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.



Notes:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V^+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

Ordering Information

Part No.	Package	Pin Layout	Temp. Range	Display Drive
TSC7106ACPL	40-Pin Plastic Dip	Normal	0°C to +70°C	LCD
TSC7106ARCPL	40-Pin Plastic Dip	Reverse	0°C to +70°C	LCD
TSC7106AIJL	40-Pin CerDIP	Normal	-25°C to +85°C	LCD
TSC7106ACBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LCD
TSC7106ACSQ	60-Pin Plastic Flat Package	Unformed Leads	0°C to +70°C	LCD
TSC7107ACPL	40-Pin Plastic Dip	Normal	0°C to +70°C	LED
TSC7107ARCPL	40-Pin CerDIP	Normal	0°C to +70°C	LED
TSC7107AIJL	40-Pin CerDIP	Normal	-25°C to +85°C	LED
TSC7107ACBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LED
TSC7107ACSQ	60-Pin Plastic Flat Package	Unformed Leads	0°C to +70°C	LED
Devices with Burn-In (160 Hours at +125°C)				
TSC7106ACPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C	LCD
TSC7107ACPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C	LED
TSC7107AIJL/BI	40-Pin CerDIP	Normal	-25°C to +85°C	LED

Pin Description

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
1	(40)	13	V^+	Positive supply voltage.
2	(39)	14	D_1	Activates the D section of the units display.
3	(38)	15	C_1	Activates the C section of the units display.
4	(37)	16	B_1	Activates the B section of the units display.
5	(36)	17	A_1	Activates the A section of the units display.
6	(35)	18	F_1	Activates the F section of the units display.
7	(34)	19	G_1	Activates the G section of the units display.
8	(33)	20	E_1	Activates the E section of the units display.
9	(32)	21	D_2	Activates the D section of the units display.

Pin Description (Cont.)

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
10	(31)	25	C_2	Activates the C section of the tens display.
11	(30)	26	B_2	Activates the B section of the tens display.
12	(29)	27	A_2	Activates the A section of the tens display.
13	(28)	28	F_2	Activates the F section of the tens display.
14	(27)	29	E_2	Activates the E section of the tens display.
15	(26)	30	D_3	Activates the D section of the hundreds display.
16	(25)	31	B_3	Activates the B section of the hundreds display.
17	(24)	32	F_3	Activates the F section of the hundreds display.
18	(23)	33	E_3	Activates the E section of the hundreds display.
19	(22)	34	AB_4	Activates both halves of the 1 in the thousands display.
20	(21)	35	POL	Activates the negative polarity display.
21	(20)	36	BP GND	TSC7106A: LCD Backplane drive output. TSC7107A: Digital Ground.
22	(19)	37	G_3	Activates the G section of the hundreds display.
23	(18)	40	A_3	Activates the A section of the hundreds display.
24	(17)	41	C_3	Activates the C section of the hundreds display.
25	(16)	43	G_2	Activates the G section of the tens display.
26	(15)	45	V^-	Negative power supply voltage.
27	(14)	46	V_{INT}	Integrator output. Connection point for integration capacitor. See INTEGRATING CAPACITOR section for additional details.
28	(13)	47	V_{BUFF}	Integration resistor connection. Use a 47 kΩ for a 200 mV full-scale range and a 470 kΩ for 2 V full-scale range.
29	(12)	49	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.47 μF capacitor for a 200 mV full-scale, and a 0.047 μF capacitor for a 2 volt full-scale. See paragraph on AUTO-ZERO CAPACITOR for more details.
30	(11)	51	V_{IN}^-	The analog low input is connected to this pin.
31	(10)	55	V_{IN}^+	The analog high input signal is connected to this pin.
32	(9)	57	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on ANALOG COMMON for more details. It also acts as a reference voltage source.
33	(8)	58	C_{REF}^-	See pin 34.
34	(7)	59	C_{REF}^+	A 0.1 μF capacitor is used in most applications. If a large common-mode voltage exists (for example the V_{IN}^- pin is not at analog common), and a 200 mV scale is used, a 1.0 μF is recommended and will hold the rollover error to 0.5 count.
35	(6)	60	V_{REF}^-	See pin 36.
36	(5)	1	V_{REF}^+	The analog input required to generate a full-scale output (1,999 counts). Place 100 mV between pins 35 and 36 for 199.9 mV full-scale. Place 1.00 volts between pins 35 and 36 for 2 volts full-scale. See paragraph on REFERENCE VOLTAGE.
37	(4)	3	Test	Lamp test. When pulled high (to V^+) all segments will be turned on and the display should read -1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38	(3)	4	OSC_3	See pin 40.
39	(2)	6	OSC_2	See pin 40.
40	(1)	10	OSC_1	Pins 40, 39, 38 make up the oscillator section. For a 48 kHz clock (3 readings per section) connect pin 40 to the junction of a 100 kΩ resistor and a 100 pF capacitor. The 100 kΩ resistor is tied to pin 39 and the 100 pF capacitor is tied to pin 38.

General Theory of Operation

Dual Slope Conversion Principles

The TSC7106A and TSC7107A are dual slope, integrating analog-to-digital converters. An understanding of the dual slope conversion technique will aid in following the detailed operation theory.

The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period (T_{SI}). Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (T_{RI}). (Figure 3A).

In a simple dual slope converter a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

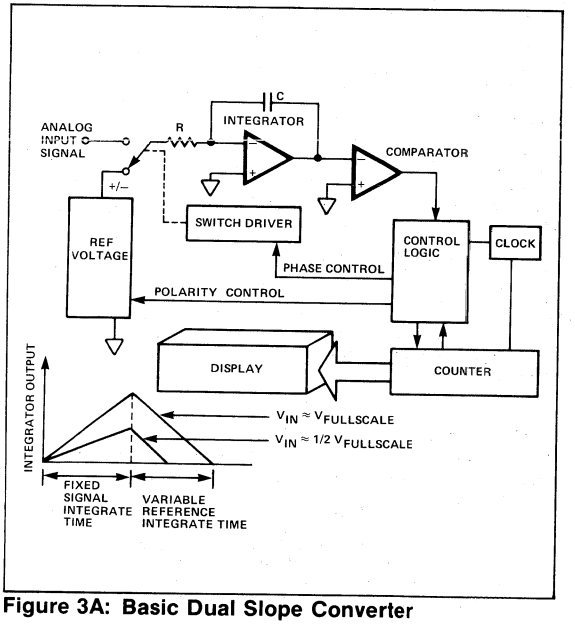


Figure 3A: Basic Dual Slope Converter

A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{RC}\int_0^{T_{SI}} V_{IN}(t)dt = \frac{V_R T_{RI}}{RC}$$

where:

V_R = Reference Voltage
T_{SI} = signal Integration Time (Fixed)
T_{RI} = Reference Voltage Integration Time (Variable)

For a constant V_{IN}:

$$V_{IN} = V_R \frac{T_{RI}}{T_{SI}}$$

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfering signals with frequency components at multiples of the averaging period will be attenuated. Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50/60 Hz power line period. (Figure 3B)

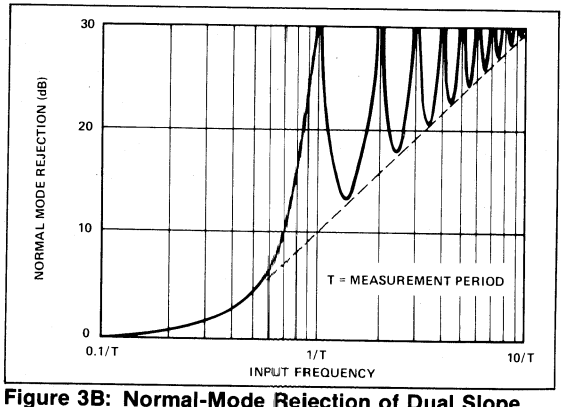


Figure 3B: Normal-Mode Rejection of Dual Slope Converter

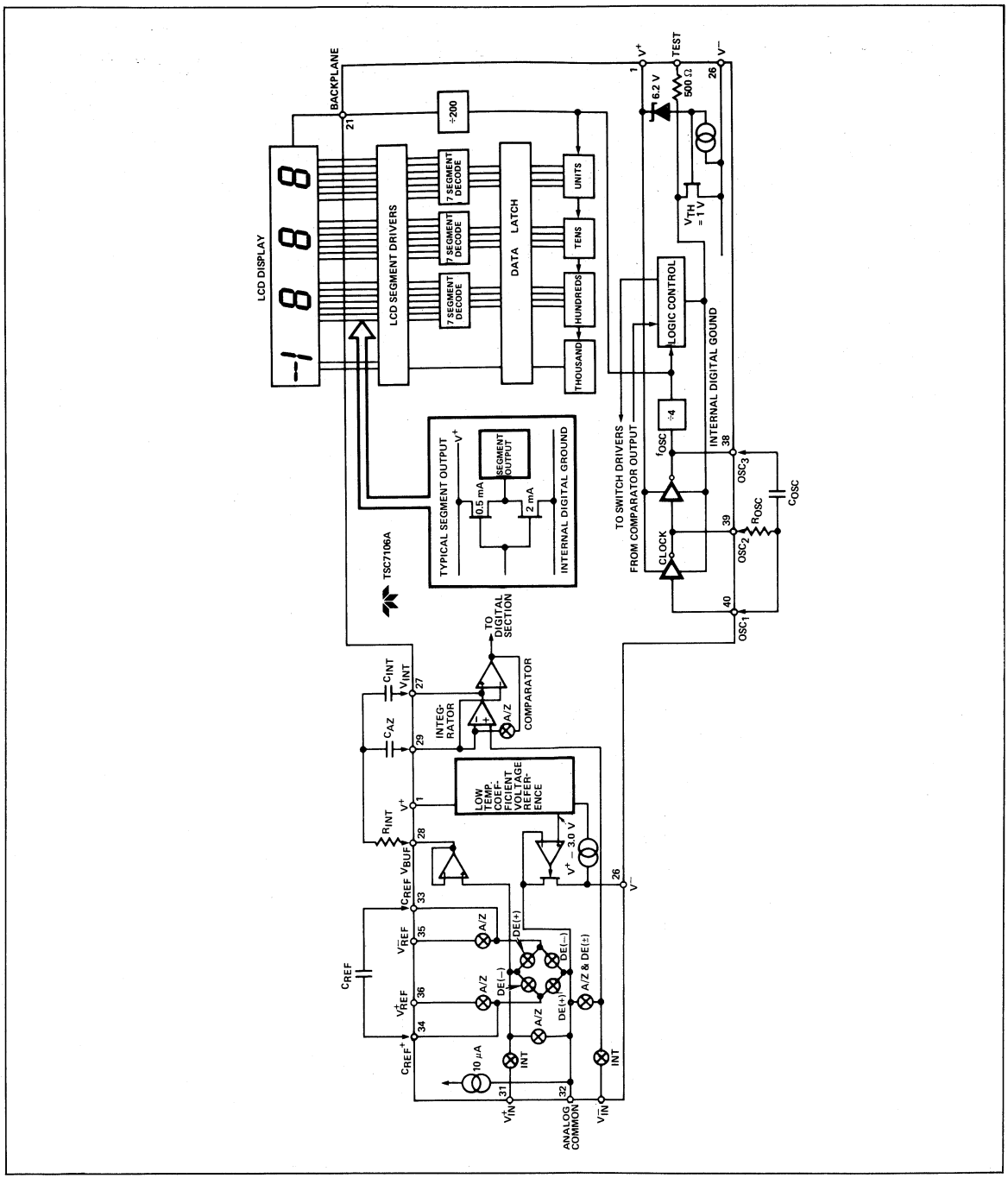


Figure 5: TSC7106A Block Diagram

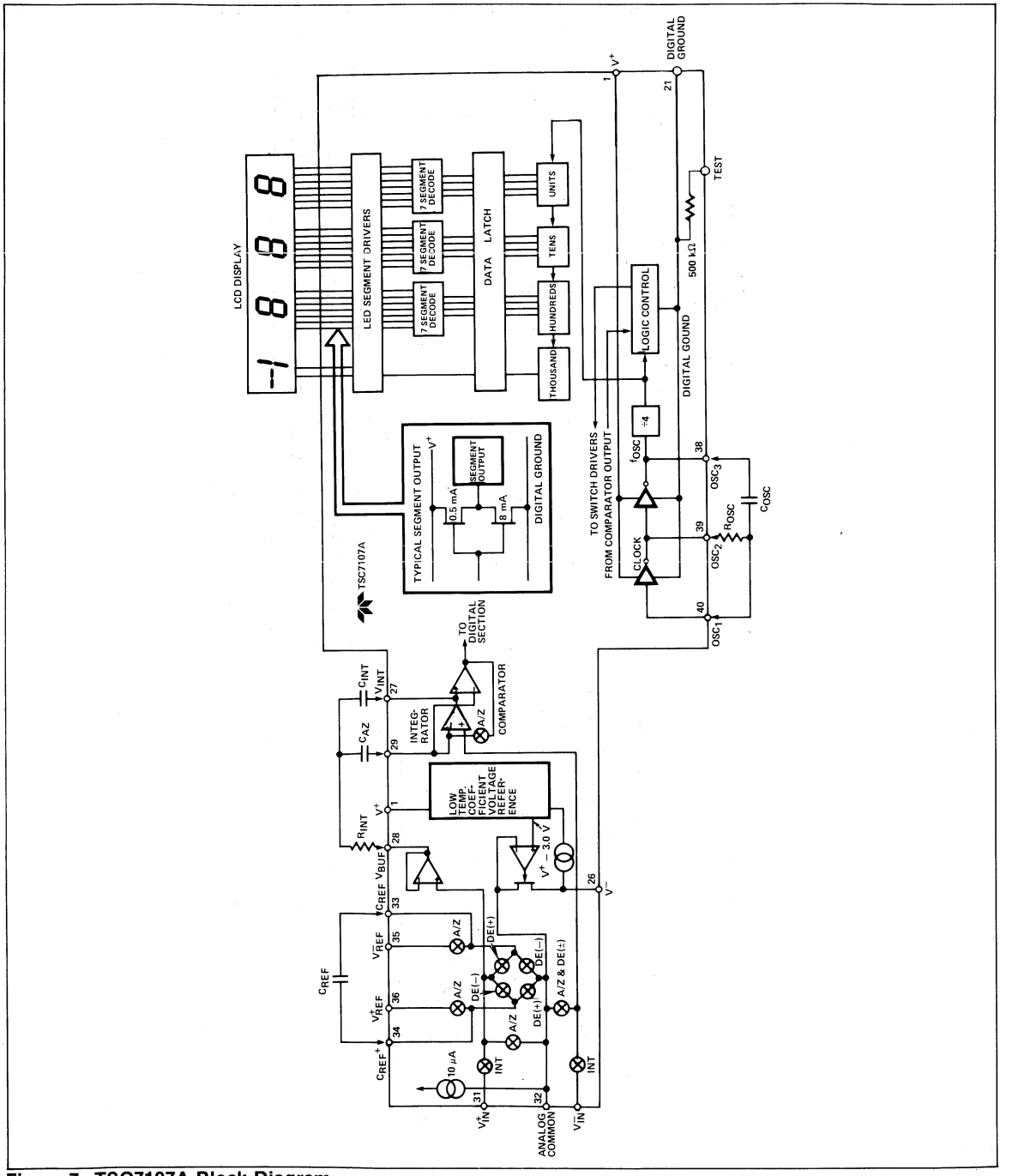


Figure 7: TSC7107A Block Diagram

Analog Section

In addition to the basic signal integrate and deintegrate cycles discussed, the circuit incorporates an auto-zero cycle. This cycle removes buffer amplifier, integrator, and comparator offset voltage error terms from the conversion. A true digital zero reading results without external adjusting potentiometers. A complete conversion consists of three cycles: an auto-zero, signal integrate and reference integrate cycle.

Auto-Zero Cycle

During the auto-zero cycle the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on C_{AZ} compensates for device offset voltages. The offset error referred to the input is less than 10 μV.

The auto-zero cycle length is 1000 to 3000 counts.

Signal Integrate Cycle

The auto-zero loop is opened, the internal differential inputs connect to V_{IN}^{+} and V_{IN}^{-}. The differential input signal is integrated for a fixed time period. The signal integration period is 1000 counts. The externally set clock frequency is divided by four before clocking the internal counters. The integration time period is:

$$T_{SI} = \frac{4}{f_{OSC}} \times 1000$$

where:

f_{OSC} = External Clock Frequency

The differential input voltage must be within the device common-mode range (1 V of either supply) when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, V_{IN}^{-} should be tied to analog common.

Polarity is determined at the end of signal integrate signal phase. The sign bit is a true polarity indication in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and auto-zero residual offsets.

Reference Integrate Cycle

The final phase is reference integrate or de-integrate. V_{IN}^{-} is internally connected to analog common and V_{IN}^{+} is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 2000 counts. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Digital Section (TSC7106A)

The TSC7106A (Figure 5) contains all the segment drivers necessary to directly drive a 3 1/2 digit liquid crystal display (LCD). An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 800. For three conversions/second the backplane frequency is 60 Hz with a 5 V nominal amplitude. When a segment driver is in phase with the backplane signal the segment is "OFF." An out of phase segment drive signal causes the segment to be "ON" or visible. This AC drive configuration results in negligible DC voltage across each LCD segment. This insures long LCD display life. The polarity segment driver is "ON" for negative analog inputs. If V_{IN}^{+} and V_{IN}^{-} are reversed this indicator would reverse.

On the TSC7106A when the test pin is pulled to V^{+} all segments are turned "ON." The display reads -1888. During this mode the LCD segments have a constant DC voltage impressed. Do not leave the display in this mode for more than several minutes. LCD displays may be destroyed if operated with DC levels for extended periods.

The display FONT and the segment drive assignment are shown in Figure 6.

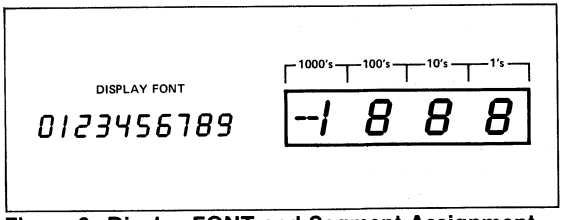


Figure 6: Display FONT and Segment Assignment

In the TSC7106A an internal digital ground is generated from a 6 volt zener diode and a large P channel source follower. This supply is made stiff to absorb the large capacitive currents when the backplane voltage is switched.

Digital Section (TSC7107A)

Figure 7 shows the TSC7107A. It is identical to the TSC7106A except that the regulated supply and back plane drive have been eliminated and the segment drive is typically 8 mA. The 1000 output (pin 19) sinks current from two LED segments, and has a 16 mA drive capability. The TSC7107A is designed to drive common anode LEDs.

In both devices, the polarity indication is "on" for negative analog inputs. If V_{IN}^{-} and V_{IN}^{+} are reversed, this indication can be reversed also, if desired.

The display font is the same as the TSC7106A.

System Timing

The oscillator frequency is divided by 4 prior to clocking the internal decade counters. The three phase measurement cycle takes a total of 4000 counts or 16000 clock pulses. The 4000 count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

- Auto-Zero Phase: 1000 to 3000 Counts
  (4000 to 12000 Clock Pulses)
  For signals less than full-scale the auto-zero phase is assigned the unused reference integrate time period.
- Signal Integrate: 1000 Counts
  (4000 Clock Pulses)
  This time period is fixed. The integration period is:

$$T_{SI} = 4000 \left[\frac{1}{f_{OSC}} \right]$$

  Where f_{OSC} is the externally set clock frequency.
- Reference Integrate: 0 to 2000 Counts
  (0 to 8000 Clock Pulses)

The TSC7106A/7107A are drop replacements for the 7106/7107 parts. External component value changes are not required to benefit from the low drift internal reference.

Clock Circuit

Three clocking methods may be used:
1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

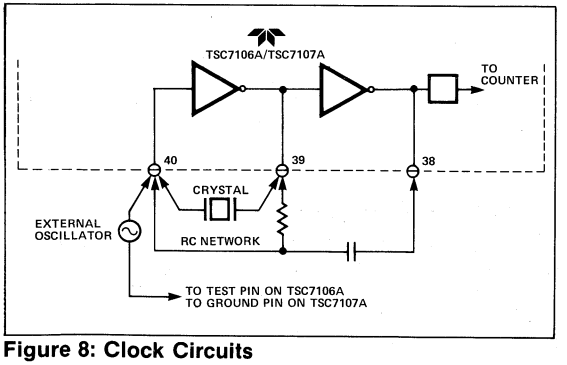


Figure 8: Clock Circuits

Component Value Selection

Auto-Zero Capacitor - C_{AZ}

The C_{AZ} capacitor size has some influence on system noise. A 0.47 μF capacitor is recommended for 200 mV full-scale applications where 1 LSB is 100 μV. A 0.047 μF capacitor is adequate for 2.0 V full-scale applications. A mylar type dielectric capacitor is adequate.

Reference Voltage Capacitor - C_{REF}

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF}. A 0.1 μF capacitor is acceptable when $V_{\overline{IN}}$ is tied to analog common. If a large common-mode voltage exists ($V_{\overline{REF}} \neq$ analog common) and the application requires a 200 mV full-scale increase C_{REF} to 1.0 μF. Rollover error will be held to less than 0.5 count. A mylar type dielectric capacitor is adequate.

Integrating Capacitor - C_{INT}

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Due to the TSC7106A/7107A superior analog common temperature coefficient specification, analog common will normally supply the differential voltage reference. For this case a ±2 V full-scale integrator output swing is satisfactory. For 3 readings/second (f_{OSC} = 48 kHz) a 0.22 μF value is suggested. If a different oscillator frequency is used C_{INT} must be changed in inverse proportion to maintain the nominal ±2 V integrator swing.

An exact expression for C_{INT} is:

$$C_{INT} = \frac{(4000)\left(\frac{1}{f_{OSC}}\right)\left(\frac{V_{FS}}{R_{INT}}\right)}{V_{INT}}$$

Where:

f_{OSC} = Clock frequency at Pin 38
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{ING} = Desired full-scale integrator output swing

C_{INT} must have low dielectric absorption to minimize rollover error. An inexpensive polypropylene capacitor is recommended.

Integrating Resistor - R_{INT}

The input buffer amplifier and integrator are designed with class A output stages. The output stage idling current is 100 μA. The integrator and buffer can supply 20 μA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region but not so large that printed circuit board leakage currents induce errors. For a 200 mV full-scale R_{INT} is 47 kΩ. A 2.0 V full-scale requires 470 kΩ.

Component	Nominal Full-Scale Voltage	
Value	200.0 mV	2.000 V
C_{AZ}	0.47 μF	0.047 μF
R_{INT}	47 kΩ	470 kΩ
C_{INT}	0.22 μF	0.22 μF

Note:
1. f_{OSC} = 48 kHz (3 readings/sec)

Oscillator Components

ROSC (Pin 40 to Pin 39) should be 100 kΩ. COSC is selected from the equation:

$$f_{OSC} = \frac{0.45}{RC}$$

For fOSC of 48 kHz, COSC is 100 pF nominally.

Note that fOSC is divided by four to generate the TSC7106A internal control clock. The backplane drive signal is derived by dividing fOSC by 800.

To achieve maximum rejection of 60 Hz noise pickup, the signal integrate period should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 40 kHz, 33 1/3 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66 2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

Reference Voltage Selection

A full-scale reading (2000 counts) requires the input signal be twice the reference voltage.

Required Full-Scale Voltage*	VREF
200.0 mV	100.0 mV
2.000 V	1.000 V

* $V_{FS} = 2\ V_{REF}$

In some applications a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output is 400 mV for 2000 lb/in². Rather than dividing the input voltage by two the reference voltage should be set to 200 mV. This permits the transducer input to be used directly.

The differential reference can also be used when a digital zero reading is required when VIN is not equal to zero. This is common in temperature measuring instrumentation. A compensating offset voltage can be applied between analog common and V_{IN}^-. The transducer output is connected between V_{IN}^+ and analog common.

The internal voltage reference potential available at analog common will normally be used to supply the converters reference. This potential is stable whenever the supply potential is greater than approximately 7 V. In applications where an externally generated reference voltage is desired refer to Figure 9.

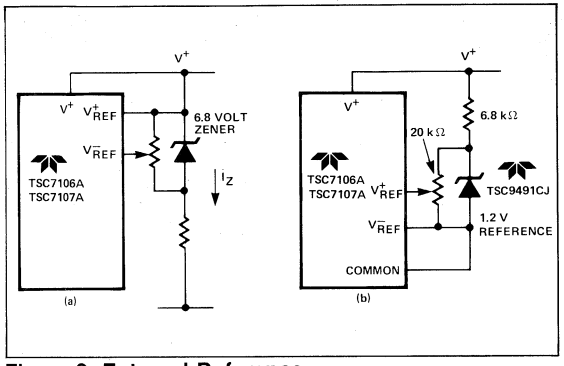


Figure 9: External Reference

Device Pin Functional Description

Differential Signal Inputs

(V_{IN}^+ (Pin 31), V_{IN}^- (Pin 30))

The TSC7106A/TSC7107A is designed with true differential inputs and accepts input signals within the input stage common mode voltage range (VCM). The typical range is $V^+ -1.0$ to $V^- +1$ V. Common-mode voltages are removed from the system when the TSC7106A/TSC7107A operates from a battery or floating power source (isolated from measured system) and V_{IN}^- is connected to analog common (VCOM): See Figure 10.

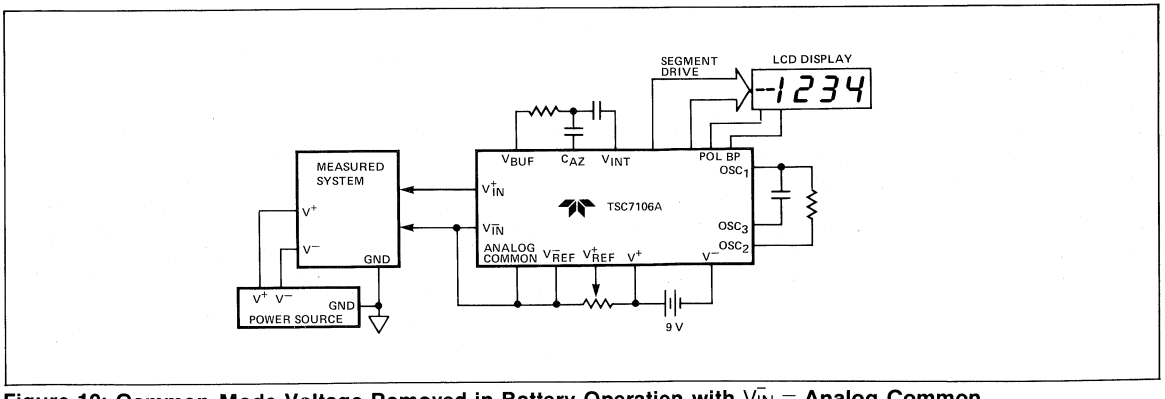


Figure 10: Common-Mode Voltage Removed in Battery Operation with V_{IN}^- = Analog Common

Differential Signal Inputs (Cont.)

In systems where common-mode voltages exist the 86 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. Integrator output saturation must be prevented. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (Figure 11). For such applications the integrator output swing can be reduced below the recommended 2.0 V full-scale swing. The integrator output will swing within 0.3 V of V^+ or V^- without increasing linearity errors.

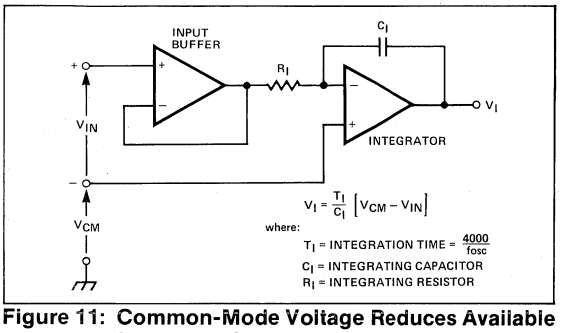


Figure 11: Common-Mode Voltage Reduces Available Integrator Swing. ($V_{COM} \neq V_{IN}$)

Differential Reference
(V^+_{REF} (Pin 36), V^-_{REF} (Pin 39))

The reference voltage can be generated anywhere within the V^+ to V^- power supply range.

To prevent rollover type errors being induced by large common-mode voltages C_{REF} should be large compared to stray node capacitance.

The TSC7106A/TSC7107A circuits have a significantly lower analog common temperature coefficient. This potential gives a very stable voltage suitable for use as a voltage reference. The temperature coefficient of analog common is 20 ppm/° C typically.

Analog Common (Pin 32)

The analog common pin is set at a voltage potential approximately 3.0 V below V^+. The potential is guaranteed to be between 2.7 V and 3.35 V below V^+. Analog common is tied internally to an N channel FET capable of sinking 30 mA. This FET will hold the common line at 3.0 V should an external load attempt to pull the common line toward V^+. Analog common source current is limited to 10 μA. Analog common is therefore easily pulled to a more negative voltage (i.e., below V^+ -3.0 V).

The TSC7106A connects the internal V^+_{IN} and V^-_{IN} inputs to analog common during the auto-zero cycle. During the reference integrate phase V^-_{IN} is connected to analog common. If V^-_{IN} is not externally connected to analog common, a common-mode voltage exists. This is rejected by the converters 86 dB common-mode rejection ratio. In battery operation analog common and V^-_{IN} are usually connected removing common-mode voltage concerns. In systems where V^-_{IN} is connected to the power supply ground or to a given voltage, analog common should be connected to V^-_{IN}.

The analog common pin serves to set the analog section reference or common point. The TSC7106A is specificially designed to operate from a battery or in any measurement system where input signals are not referenced (float) with respect to the TSC7106A power source. The analog common potential of V^+ -3.0 V gives a 6 V end of battery life voltage. The common potential has a 0.001%/% voltage coefficient and 15 Ω output impedance.

With sufficiently high total supply voltage ($V^+ - V^- > 7.0$ V) analog common is a very stable potential with excellent temperature stability — typically 20 ppm/° C. This potential can be used to generate the reference voltage. An external voltage reference will be unnecessary in most cases because of the 50 ppm/° C maximum temperature coefficient. See Internal Voltage Reference discussion.

Test (Pin 37)

The test pin potential is 5 V less than V^+. Test may be used as the negative power supply connection for external CMOS logic. The test pin is tied to the internally generated negative logic supply (Internal Logic Ground) through a 500 Ω resistor in the TSC7106A. The test pin load should be no more than 1 mA.

If test is pulled high to V^+ all segments plus the minus sign will be activated. Do not operate in this mode for more than several minutes with the TSC7106A. With Test = V^+ the LCD Segments are impressed with a DC voltage which will destroy the LCD.

The test pin will sink about 10 mA when pulled to V^+.

Internal Voltage Reference Stability

The analog common voltage termperature stability has been significantly improved (Figure 12). The "A" version of the industry standard circuits allow users to upgrade old systems and design new systems without external voltage references. External R and C values do not need to be changed. Figure 13 shows analog common supplying the necessary voltage reference for the TSC7106A/TSC7107A.

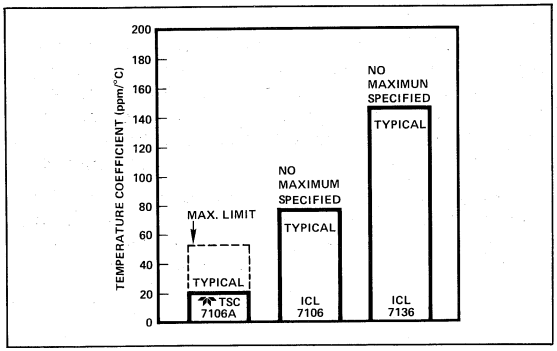


Figure 12: Analog Common Temperature Coefficient

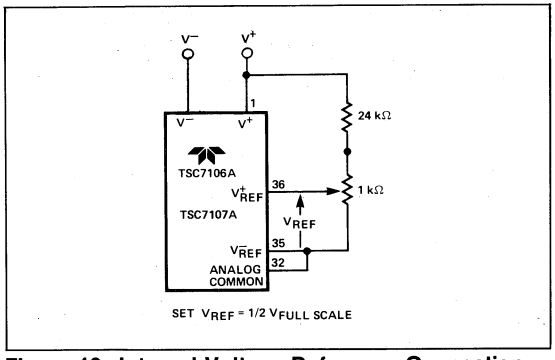


Figure 13: Internal Voltage Reference Connection

TSC7107A Power Supplies

The TSC7107A is designed to work from ±5 V supplies. However, if a negative supply is not available, it can be generated from the clock output with two diodes, two capacitors and an inexpensive IC. Figure 13 shows this application.

In selected applications a negative supply is not required. The conditions to use a single +5 V supply are:

- The input signal can be referenced to the center of the common-mode range of the converter.
- The signal is less than ±1.5 volts.
- An external reference is used.

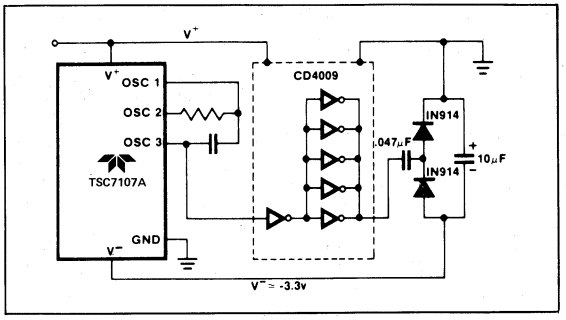


Figure 14: Generating Negative Supply From +5 V

The TSC7660 DC to DC converter may also be used to generate -5 V from +5 V (Figure 15).

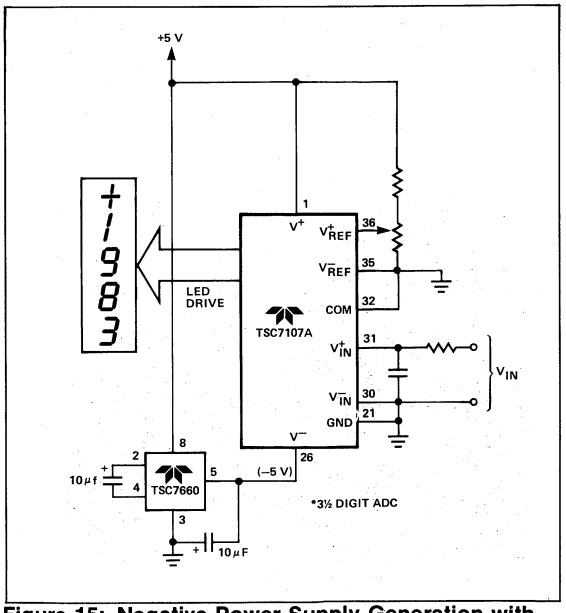


Figure 15: Negative Power Supply Generation with TSC7660.

TSC7107 Power Dissipation Reduction

The TSC7107A sinks the LED display current and this causes heat to build up in the IC package. If the internal voltage reference is used, the changing chip temperature can cause the display to change reading. By reducing package power dissipation such variations can be reduced. By reducing the LED common anode voltage the TSC7107A package power dissipation is reduced.

Figure 16 is a photograph of a curve-trace display showing the relationship between output current and output voltage for a typical TSC7107CPL. Since a typical LED has 1.8 volts across it at 7 mA, and its common anode is connected to +5 V, the TSC7107A output is at 3.2 V (point A on Figure 15). Maximum power dissipation is 8.1 mA X 3.2 V X 24 segments = 622 mW.

Notice, however, that once the TSC7107A output voltage is above two volts, the LED current is essentially constant as output voltage increases. Reducing the output voltage by 0.7 V (point B of Figure 15) results in 7.7 mA of LED current, only a 5 percent reduction. Maximum power dissipation is now only 7.7 mA X 2.5 V X 24 = 462 mW, a reduction of 26%. An output voltage reduction of 1 volt (point C) reduces LED current by 10% (7.3 mA) but power dissipation by 38%! (7.3 mA X 2.2 V X 24 = 385 mW).

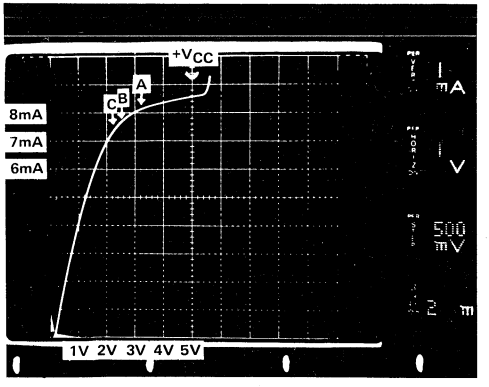


Figure 16: TSC7107A Output Current vs Output Voltage

Reduced power dissipation is very easy to obtain. Fig. 17 shows two ways: either a 5.1 ohm, 1/4 watt resistor or a 1 Amp diode placed in series with the display (but not in series with the TSC7107A). The resistor will reduce the TSC7107A output voltage, when all 24 segments are "ON," to point "C" of Fig. 16. When segments turn off, the output voltage will increase. The diode, on the other hand, will result in a relatively steady output voltage, around point "B."

In addition to limiting maximum power dissipation, the resistor reduces the change in power dissipation as the display changes. This effect is caused by the fact that, as fewer segments are "ON," each "ON" output drops more voltage and current. For the best case of six segments (a "111" display) to worst case (a "1888" display) the resistor will change about 230 mW, while a circuit without the resistor will change about 470 mW. Therefore, the resistor will reduce the effect of display dissipation on reference voltage drift by about 50%.

The change in LED brightness caused by the resistor is almost unnoticeable as more segments turn off. If display brightness remaining steady is very important to the designer, a diode may be used instead of the resistor.

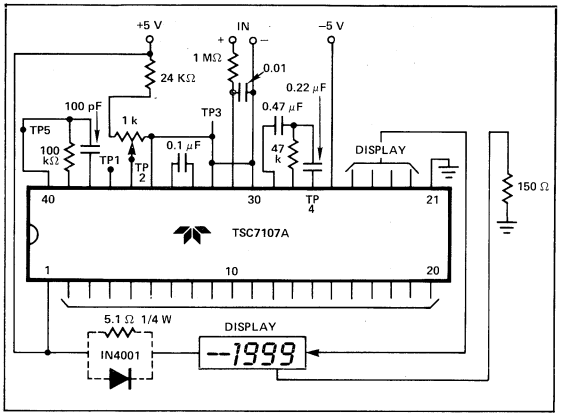


Figure 17: Diode or Resistor Limits Package Power Dissipation.

Applications Information

Liquid Crystal Display Sources

Several LCD manufacturers supply standard LCD displays to interface with the TSC7106A 3 1/2 digit analog-to-digital converter.

Manufacturer	Address/Phone	Representative Part Numbers[1]
Crystaloid Electronics	5282 Hudson Dr., Hudson, OH 44236 216/655-2429	C5335, H5535, T5135, SX440
AND	770 Airport Blvd., Burlingame, CA 94010 415/347-9916	FE 0801 FE 0203
EPSON	3415 Kashikawa St., Torrance, CA 90505 213/534-0360	LD-B709BZ LD-H7992AZ
Hamlin, Inc.	612 E. Lake St., Lake Mills, WI 53551 414/648-2361	3902, 3933, 3903

Note:
1. Contact LCD manufacturer for full product listing/specifications.

Light Emitting Diode Display Sources

Several LED manufacturers supply seven segment digits with and without decimal point annunciators for the TSC7107A.

Manufacturer	Address	Display Type
Hewlett Packard Components	640 Page Mill Rd. Palo Alto, CA 94304	LED
Litronix, Inc.	19000 Homestead Rd. Cupertino, CA 94010	LED
And	770 Airport Blvd. Burlingame, CA 94010	LED

Decimal Point and Annunciator Drive

The test pin is connected to the internally-generated digital logic supply ground through a 500 Ω resistor. The test pin may be used as the negative supply for external CMOS gate segment drivers. LCD display annunciators for decimal points, low battery indication, or function indication may be added without adding an additional supply. No more than 1 mA should be supplied by the test pin. The test pin potential is approximately 5 V below V^+.

Ratiometric Resistance Measurements

The true differential input and differential reference make ratiometric readings possible. Typically in a ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input and the voltage across the known resistor applied to the reference input. If the unknown equals the standard, the display will read 1000. The displayed reading can be determined from the following expression:

$$\text{Displayed Reading} = \frac{\text{R Unknown}}{\text{R Standard}} \times 1000$$

The display will overrange for R Unknown ≥ 2 x R Standard.

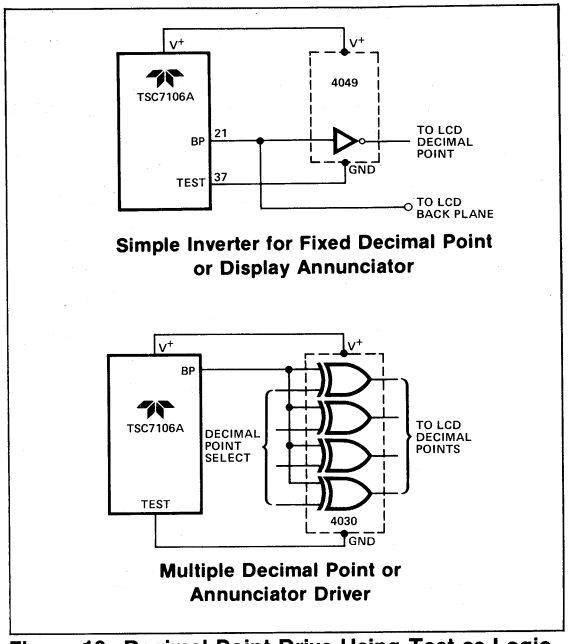


Figure 18: Decimal Point Drive Using Test as Logic Ground.

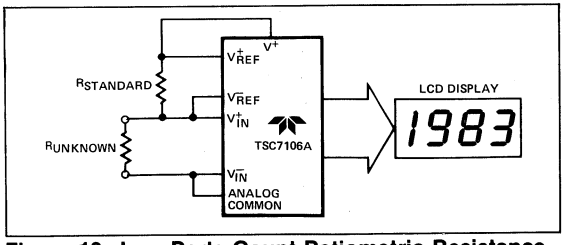


Figure 19: Low Parts Count Ratiometric Resistance Measurement

Application Circuits

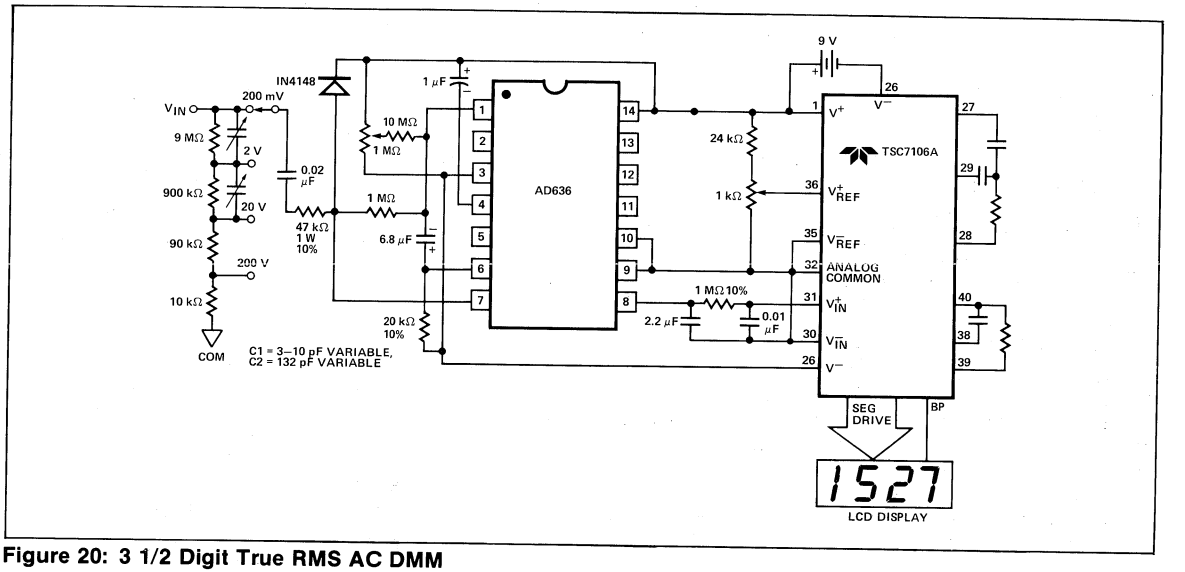


Figure 20: 3 1/2 Digit True RMS AC DMM

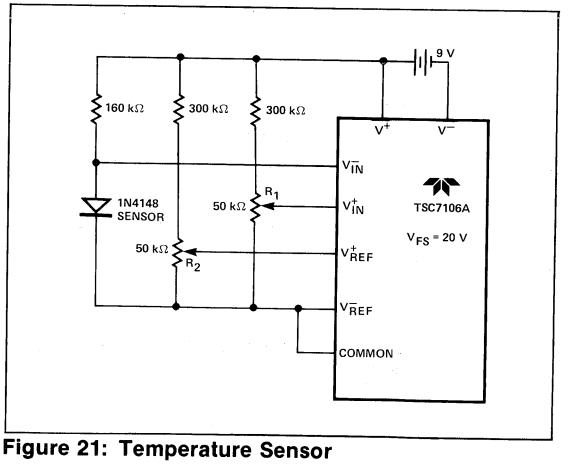


Figure 21: Temperature Sensor

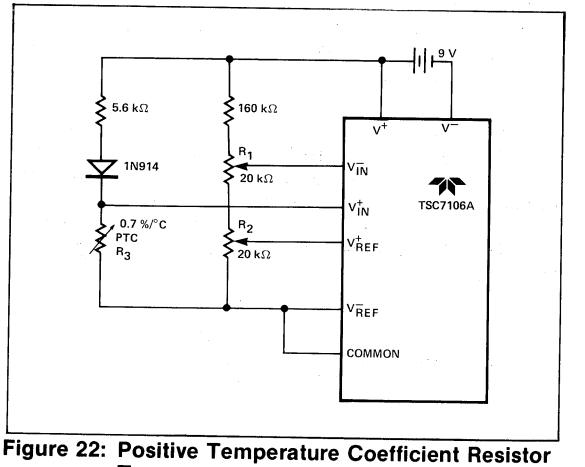


Figure 22: Positive Temperature Coefficient Resistor Temperature Sensor

Application Circuits (Cont.)

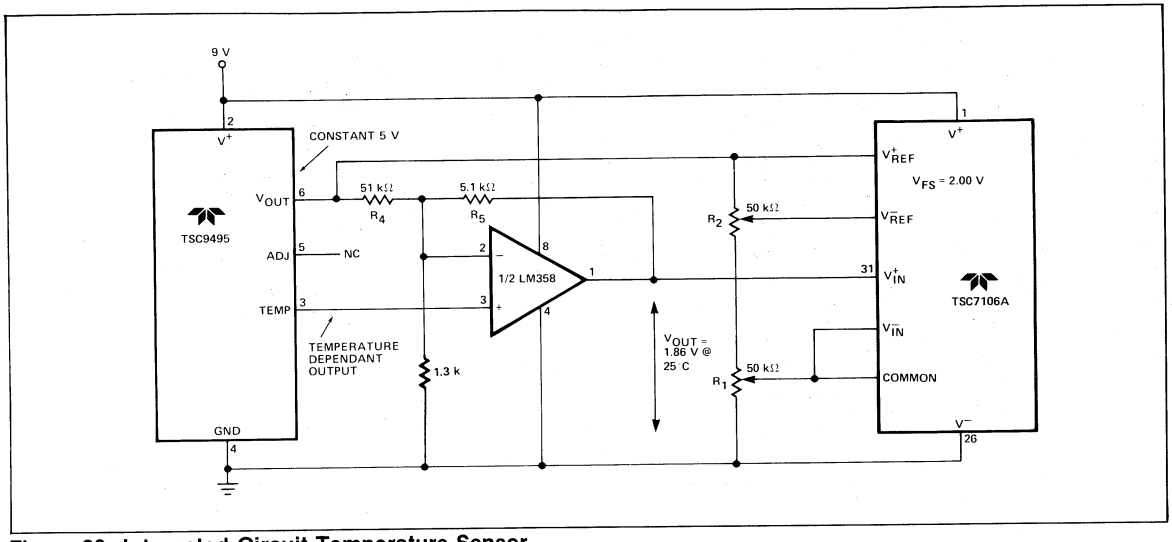


Figure 23: Integrated Circuit Temperature Sensor

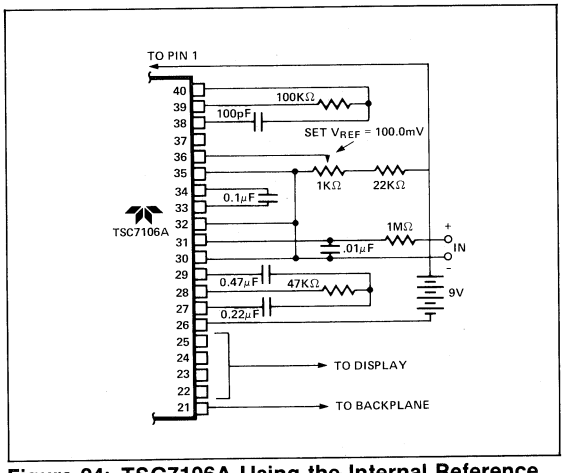


Figure 24: TSC7106A Using the Internal Reference. (200 mV Full-Scale, 3 RPS).

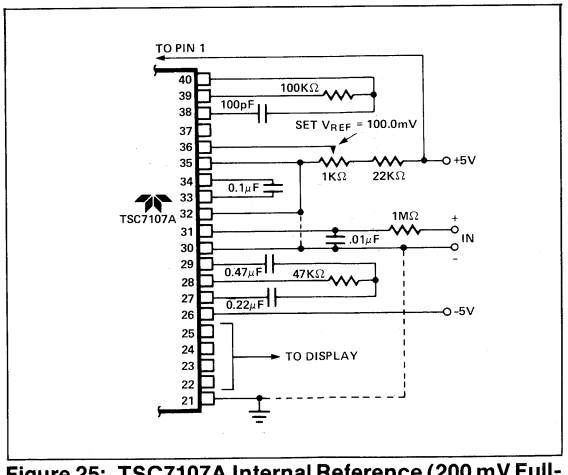


Figure 25: TSC7107A Internal Reference (200 mV Full-Scale, 3 RPS, V_{IN} Tied to GND for Single Ended Inputs).

Application Circuits (Cont.)

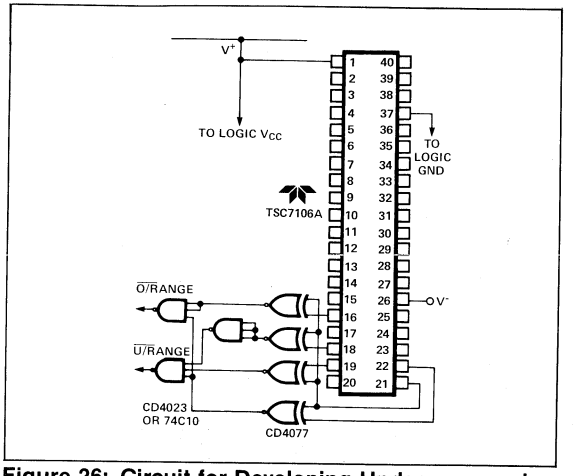


Figure 26: Circuit for Developing Underrange and Overrange Signals from TSC7106A Outputs.

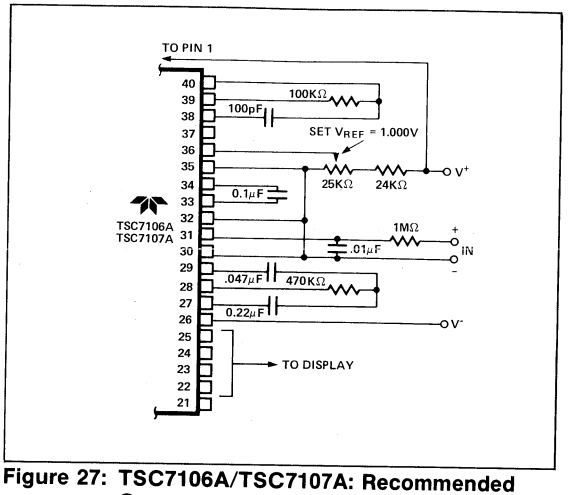


Figure 27: TSC7106A/TSC7107A: Recommended Component Values for 2.00 V Full-Scale.

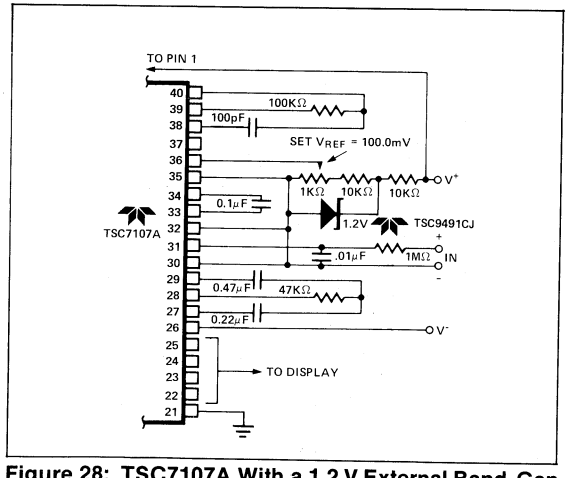


Figure 28: TSC7107A With a 1.2 V External Band-Gap Reference. V_{IN}^- Tied to Common).

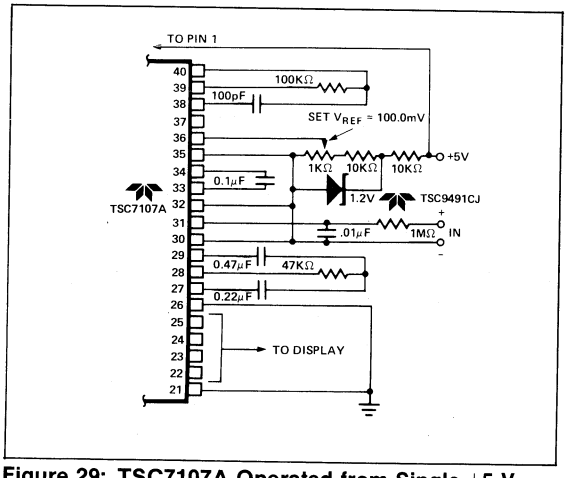


Figure 29: TSC7107A Operated from Single +5 V Supply. An External Reference Must Be Used in This Application.

TELEDYNE SEMICONDUCTOR

TSC7106 (LCD Drive)
TSC7107 (LED Drive)
3 1/2 Digit A/D Converter
• Direct Display Drive
• Automatic Zero Correction

General Description

The TSC7106 and TSC7107 3-1/2 digit CMOS analog-to-digital converters contain all the active components necessary to construct a 0.05% resolution measurement system. Seven segment decoders, polarity and digit drivers, voltage reference and clock circuit are integrated on chip. The TSC7106 drives liquid crystal displays (LCD) and includes a backplane driver. The TSC7107 drives common anode light emitting diode (LED) displays directly with an 8 mA drive current per segment.

A low cost, high resolution indicating meter requires only a display, four resistors, and four capicitors. The TSC7106 low power drain and 9 V battery operation make it ideal for portable applications.

The TSC7106/TSC7107 reduces linearity error to less than 1 count. Rollover error — the difference in readings for equal magnitude but opposite polarity input signals — is below ± 1 count. High impedance differential inputs offer 1 pA leakage current and a $10^{12}\ \Omega$ input impedance. The differential reference input allows ratiometric measurements for ohms or bridge transducer measurements. The 15 μVp-p noise performance guarantees a "rock solid" reading. The auto-zero cycle guarantees a zero display reading with a zero volt input.

The TSC7106/TSC7107 dual slope conversion technique automatically rejects interference signals if the converters integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400 Hz line frequency signals are present.

The TSC7106/TSC7107 are available in a small 60-pin flat package for compact designs. Standard devices are offered in an industrial temperature range and with burn-in lasting for 160 hours at +125° C.

For applications requiring a more temperature stable internal reference voltage refer to the TSC7106A/7107A data sheets. A display hold feature is available on the TSC7116A and TSC7117A converters.

Features

- Drives LCD or LED Displays Directly
- Guaranteed Zero Reading with Zero Input
- Low Noise for Stable Display
  -2.000 V or 200.0 mV Full-Scale Range
- Auto-Zero Cycle Eliminates Need for Zero Adjustment Potentiometer
- True Polarity Indication for Precision Null Applications
- Convenient 9 V Battery Operation (TSC7106)
- High Impedance CMOS Differential Inputs ..... $10^{12}\ \Omega$
- Differential Reference Inputs Simplify Ratiometric Measurements
- Low Power Operation ..... 10 mW

7

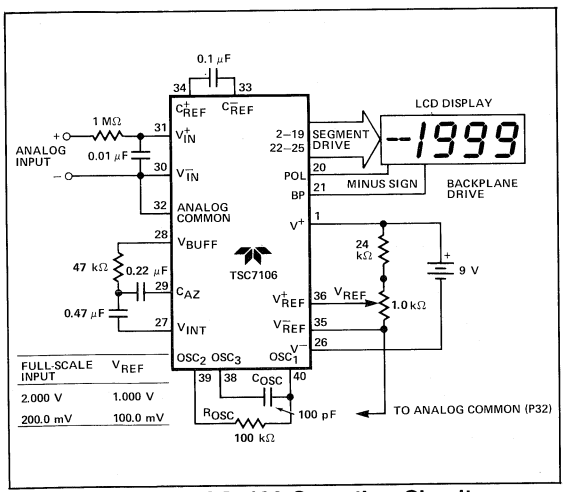


Figure 1: Typical TSC7106 Operating Circuit

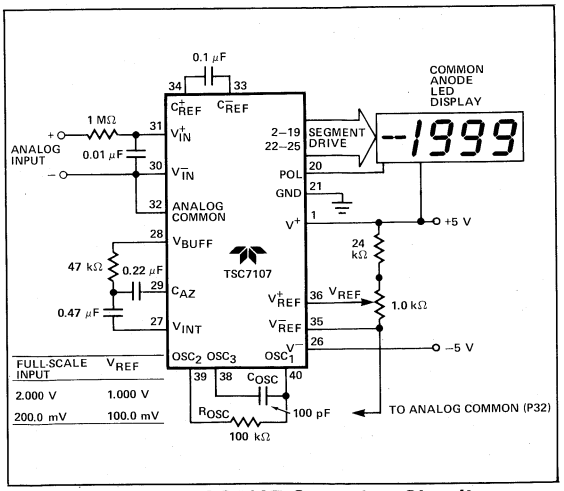


Figure 2: Typical TSC7107 Operating Circuit

Absolute Maximum Ratings

TSC7106

Supply Voltage (V^+ to V^-) ..... 15 V
Analog Input Voltage (either input) (Note 1) .... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... Test to V^+
Power Dissipation (Note 2)
  CerDIP Package ..... 1000 mW
  Plastic Package ..... 800 mW
Operating Temperature
  "C" Devices ..... 0°C to +70°C
  "I" Devices ..... -25°C to +85°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may effect device reliability.

TSC7107

Supply Voltage
  V^+ ..... +6 V
  V^- ..... -9 V
Analog Input Voltage (either input) (Note 1) .... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... GND to V^+
Power Dissipation (Note 1)
  CerDIP Package ..... 1000 mW
  Plastic Package ..... 800 mW
Operating Temperature
  "C" Devices ..... 0°C to +70°C
  "I" Devices ..... -25°C to +85°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Electrical Characteristics (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	V_{IN} = 0.0 V Full-Scale = 200.0 mV	-00.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in Reading for Equal Positive and Negative Reading Near Full-Scale)	$-V_{IN} = +V_{IN} \simeq$ 200.0 mV	-1	±0.2	+1	Counts
Linearity (Max. Deviation From Best Straight Line Fit)	Full-Scale = 200 mV or Full-Scale = 2.000 V	-1	±0.2	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1 V, V_{IN} = 0 V. Full-Scale = 200.0 mV	—	50	—	μV/V
Noise (Pk - Pk Value Not Exceeded 95% of Time)	V_{IN} = 0 V Full-Scale = 200.0 mV	—	15	—	μV
Leakage Current @ Input	V_{IN} = 0 V	—	1	10	pA
Zero Reading Drift	V_{IN} = 0 V "C" Device = 0°C to 70°C V_{IN} = 0 V "I" Device = -25°C to +85°C	— —	0.2 1.0	1 2	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0 mV, "C" Device = 0°C to 70°C (Ext. Ref = 0 ppm/°C) V_{IN} = 199.0 mV "I" Device: -25°C to +85°C	 —	1 —	5 20	ppm/°C ppm/°C
Supply Current (Does Not Include LED Current for 7107)	V_{IN} = 0	—	0.8	1.8	mA
Analog Common Voltage (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog common (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply	—	80	—	ppm/°C
TSC7106 ONLY Pk - Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V
TSC7106 ONLY Pk - Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V

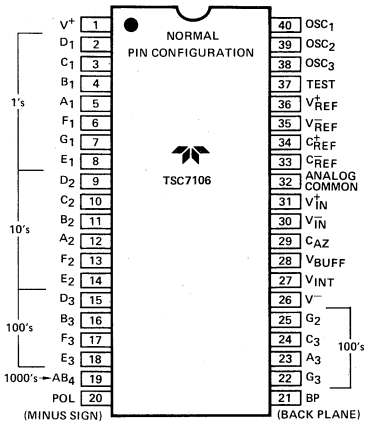
Electrical Characteristics (Note 3) (Continued)

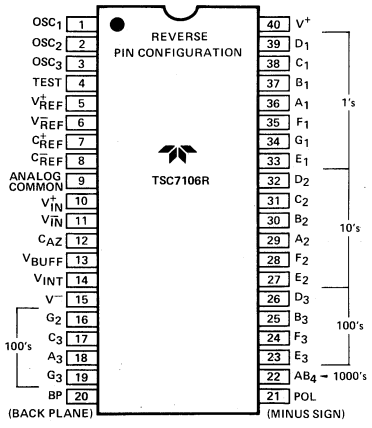
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
TSC7107 ONLY Segment Sinking Current (Except Pin 19)	$V^+ = 5.0$ V Segment Voltage = 3 V	5	8.0	—	mA
TSC7107 ONLY Segment Sinking Current (Pin 19 Only)	$V^+ = 5.0$ V Segment Voltage = 3 V	10	16	—	mA

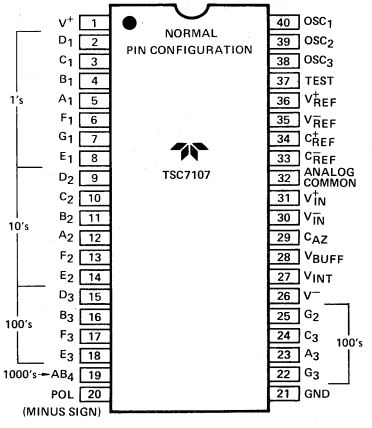
NOTES:
1. Input voltages may exceed the supply voltages provided the input current is limited to ± 100 μA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Unless other wise noted, specifications apply to both the TSC7106 and TSC7107 at $T_A = 25°C$, $f_{CLOCK} = 48$ kHz. TSC7106 is tested in the circuit of Figure 1. TSC7107 is tested in the circuit of Figure 2.
4. Refer to "Differential Input" discussion.
5. Backplane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average dc component is less than 50 mV.

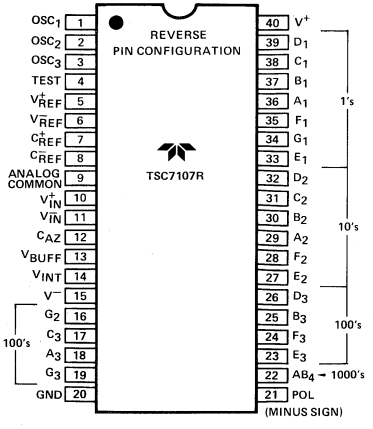
7

Pin Configuration

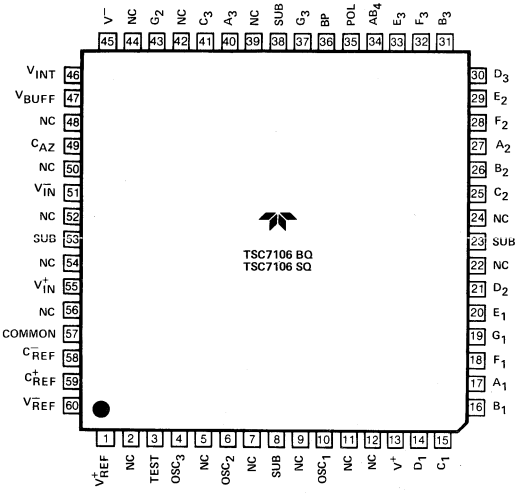




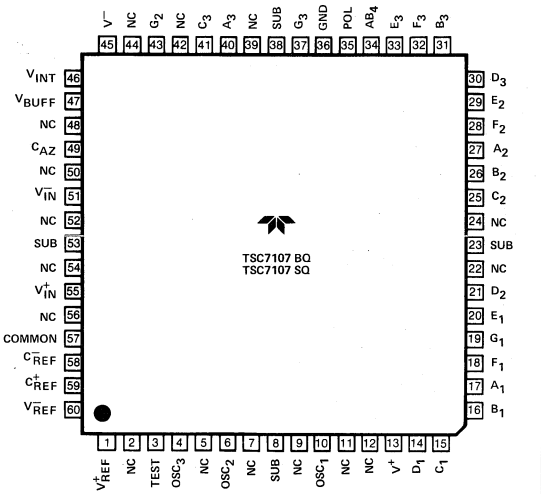




Pin Configuration (Continued)



NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.



NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

Ordering Information

Part No.	Package	Pin Layout	Temp. Range	Display Drive
TSC7106CPL	40-Pin Plastic Dip	Normal	0°C to +70°C	LCD
TSC7106RCPL	40-Pin Plastic Dip	Reverse	0°C to +70°C	LCD
TSC7106IPL	40-Pin Plastic Dip	Normal	-25°C to +85°C	LCD
TSC7106CJL	40-Pin CerDIP	Normal	0°C to +70°C	LCD
TSC7106IJL	40-Pin CerDIP	Normal	-25°C to +85°C	LCD
TSC7106CBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LCD
TSC7106CSQ	60-Pin Plastic Flat Package	Unformed Leads	0°C to +70°C	LCD
TSC7107CPL	40-Pin Plastic Dip	Normal	0°C to +70°C	LED
TSC7107RCPL	40-Pin Plastic Dip	Normal	0°C to +70°C	LED
TSC7107IPL	40-Pin Plastic Dip	Normal	-25°C to +85°C	LED
TSC7107CJL	40-Pin CerDIP	Normal	0°C to +70°C	LED
TSC7107IJL	40-Pin CerDIP	Normal	-25°C to +85°C	LED
TSC7107CBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LED
TSC7107CSQ	60-Pin Plastic Flat Package	Unformed Leads	0°C to +70°C	LED
Devices with Burn-In (160 Hours at +125°C)				
TSC7106CPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C	LCD
TSC7106RCPL/BI	40-Pin Plastic Dip	Reverse	0°C to +70°C	LCD
TSC7106IJL/BI	40-Pin CerDIP	Normal	-25°C to +85°C	LCD
TSC7107CPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C	LED
TSC7107RCPL/BI	40-Pin Plastic Dip	Reverse	0°C to +70°C	LED
TSC7107IJL/BI	40-Pin CerDIP	Normal	-25°C to +85°C	LED

Pin Description

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
1	(40)	13	V^+	Positive supply voltage.
2	(39)	14	D_1	Activates the D section of the units display.
3	(38)	15	C_1	Activates the C section of the units display.
4	(37)	16	B_1	Activates the B section of the units display.
5	(36)	17	A_1	Activates the A section of the units display.
6	(35)	18	F_1	Activates the F section of the units display.
7	(34)	19	G_1	Activates the G section of the units display.
8	(33)	20	E_1	Activates the E section of the units display.
9	(32)	21	D_2	Activates the D section of the units display.
10	(31)	25	C_2	Activates the C section of the tens display.
11	(30)	26	B_2	Activates the B section of the tens display.
12	(29)	27	A_2	Activates the A section of the tens display.
13	(28)	28	F_2	Activates the F section of the tens display.
14	(27)	29	E_2	Activates the E section of the tens display.
15	(26)	30	D_3	Activates the D section of the hundreds display.
16	(25)	31	B_3	Activates the B section of the hundreds display.
17	(24)	32	F_3	Activates the F section of the hundreds display.
18	(23)	33	E_3	Activates the E section of the hundreds display.
19	(22)	34	AB_4	Activates both halves of the 1 in the thousands display.
20	(21)	35	POL	Activates the negative polarity display.
21	(20)	36	BP GND	TSC7106: LCD Backplane drive output. TSC7107: Digital Ground.
22	(19)	37	G_3	Activates the G section of the hundreds display.
23	(18)	40	A_3	Activates the A section of the hundreds display.
24	(17)	41	C_3	Activates the C section of the hundreds display.
25	(16)	43	G_2	Activates the G section of the tens display.
26	(15)	45	V^-	Negative power supply voltage.
27	(14)	46	V_{INT}	Integrator output. Connection point for integration capacitor. See INTEGRATING CAPACITOR section for additional details.
28	(13)	47	V_{BUFF}	Integration resistor connection. Use a 47 kΩ for a 200 mV full-scale range and a 470 kΩ for 2 V full-scale range.
29	(12)	49	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.47 μF capacitor for a 200 mV full-scale, and a 0.047 μF capacitor for a 2 volt full-scale. See paragraph on AUTO-ZERO CAPACITOR for more details.
30	(11)	51	V_{IN}^-	The analog low input is connected to this pin.
31	(10)	55	V_{IN}^+	The analog high input signal is connected to this pin.
32	(9)	57	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on ANALOG COMMON for more details. It also acts as a reference voltage source.
33	(8)	58	C_{REF}^-	See pin 34.
34	(7)	59	C_{REF}^+	A 0.1 μF capacitor is used in most applications. If a large common-mode voltage exists (for example the V_{IN} pin is not at analog common), and a 200 mV scale is used, a 1.0 μF is recommended and will hold the rollover error to 0.5 count.
35	(6)	60	V_{REF}^-	See pin 36.

Pin Description (Cont.)

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
36	(5)	1	V_{REF}^{+}	The analog input required to generate a full-scale output (1,999 counts). Place 100 mV between pins 35 and 36 for 199.9 mV full-scale. Place 1.00 volts between pins 35 and 36 for 2 volts full-scale. See paragraph on REFERENCE VOLTAGE.
37	(4)	3	Test	Lamp test. When pulled high (to V^{+}) all segments will be turned on and the display should read -1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38	(3)	4	OSC_3	See pin 40.
39	(2)	6	OSC_2	See pin 40.
40	(1)	10	OSC_1	Pins 40, 39, 38 make up the oscillator section. For a 48 kHz clock (3 readings per section) connect pin 40 to the junction of a 100 kΩ resistor and a 100 pF capacitor. The 100 kΩ resistor is tied to pin 39 and the 100 pF capacitor is tied to pin 38.

Analog Section

Figure 3 shows the Block Diagram of the Analog Section for the TSC7106 and TSC7107. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) reference (REF).

Auto-Zero Phase

Input high and low are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. The offset referred to the input is less than 10 μV.

Signal Integrate Phase

The auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between V_{IN}^{+} and V_{IN}^{-} for a fixed time. This differential voltage can be within a wide common-mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, V_{IN}^{-} can be tied to analog common to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

Reference Integrate Phase

The final phase is reference integrate or de-integrate. Input low is internally connected to analog common and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacitance on its nodes. If there is a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (-) input voltage will give a roll-over error. By selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worse case condition. (See Component Values Selection.)

Differential Input

The input can accept differential voltages anywhere within the common-mode range of the input amplifier; or specifically from 1.0 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worse case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2 V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

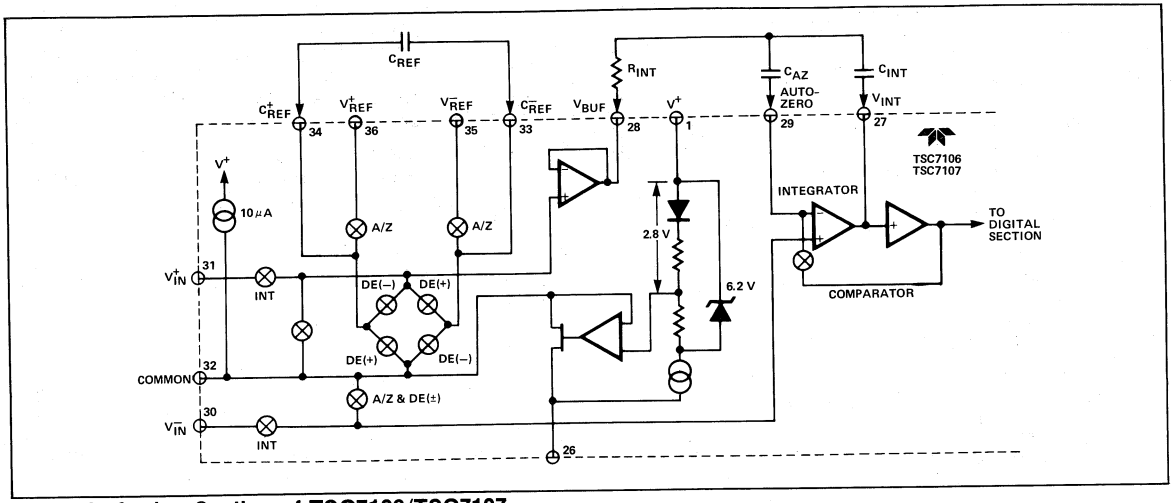


Figure 3: Analog Section of TSC7106/TSC7107

Analog Common

This pin is included primarily to set the common-mode voltage for battery operation (TSC7106) or for any system where the input signals are floating with respect to the power supply. The common pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6 V. However, the analog common has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7 V), the common voltage will have a low voltage coefficient (0.001%/%), low output impedance (≈15 Ω), and a temperature coefficient of 80 ppm/° C typically.

An external reference may be added to improve temperature stability or the TSC7106A/TSC7107A devices with lower analog common temperature drift may be used. The circuit is shown in Figure 4.

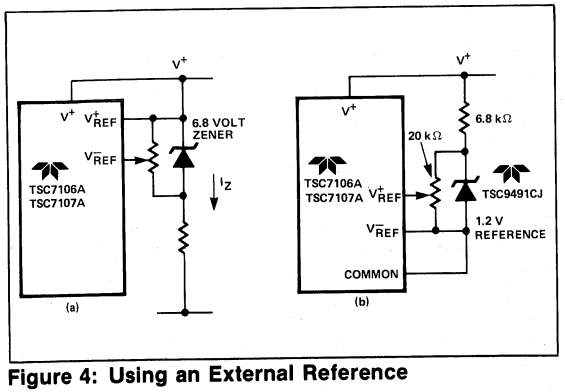


Figure 4: Using an External Reference

Analog common is also used as the V_{IN}^- return during auto-zero and deintegrate. If V_{IN}^- is different from analog common, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications V_{IN}^- will be set at a fixed known voltage (power supply common for instance). In this application, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog common, it should be since this removes the common-mode voltage from the reference system.

Within the IC, analog common is tied to an N-channel FET that can sink 30 mA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10 μA of source current, so common may easily be tied to a more negative voltage thus over-riding the internal reference.

Test

The TEST pin serves two functions. On the TSC7107 it is coupled to the internally generated digital supply through a 500 Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1 mA load should be applied.

The second function is a "lamp test." When TEST is pulled high (to V^+) all segments will be turned on and the display should read -1888. The TEST pin will sink about 10 mA under these conditions.

Caution: On the TSC7106, in the lamp test mode the segments have a constant dc voltage (no square-wave) and may burn the LCD display if left in this mode for several minutes.

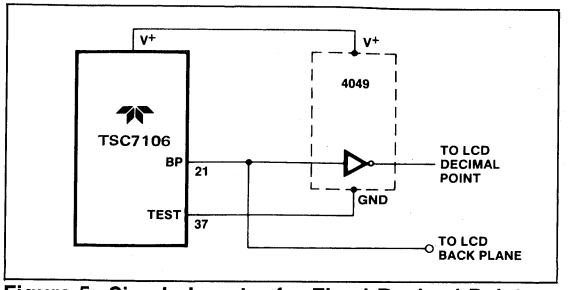


Figure 5: Simple Inverter for Fixed Decimal Point

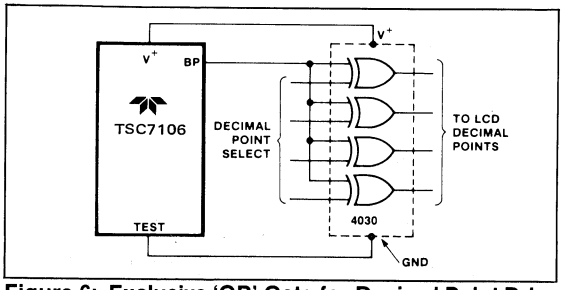


Figure 6: Exclusive 'OR' Gate for Decimal Point Drive

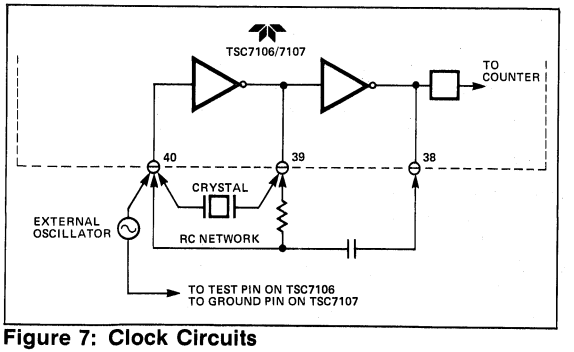


Figure 7: Clock Circuits

Digital Section

Figures 8 and 9 show the digital section for the TSC7106 and TSC7107, respectively. In the TSC7106 (Figure 8), an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases, negligible dc voltage exists across the segments.

Figure 9 is the Digital Section of the TSC7107. It is identical to the TSC7106 except that the regulated supply and back plane drive have been eliminated and the segment drive is typically 8 mA. The 1000 output (pin 19) sinks current from two LED segments, and has a 16 mA drive capability. The TSC7107 is designed to drive common anode LEDs.

In both devices, the polarity indication is "on" for negative analog inputs. If V_{IN}^- and V_{IN}^+ are reversed, this indication can be reversed also, if desired.

System Timing

Figure 9 shows the clocking method used in the TSC7106 and TSC7107. Three clocking methods may be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An RC oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full-scale auto-zero gets the unused portion of reference de-integrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48 kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 48 kHz, 40 kHz, 33-1/3 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66-2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

Component Value Selection

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full-scale where noise is very important, a 0.47 μF capacitor is recommended. On the 2 volt scale, a 0.047 μF capacitor increase the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1 μF capacitor is acceptable in most applications. However, where a large common-mode voltage exists (i.e. the V_{IN}^- pin is not at analog common) and a 200 mV scale is used, a large value is required to prevent to roll-over error. Generally 1.0 μF will hold the roll-over error to 0.5 count in this instance.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the TSC7106 or the TSC7107, when the analog common is used as a reference, a nominal ±2 volt full-scale integrator swing is acceptable. For the TSC7107 with ±5 volt supplies and analog common tied to supply ground, a ±3.5 to

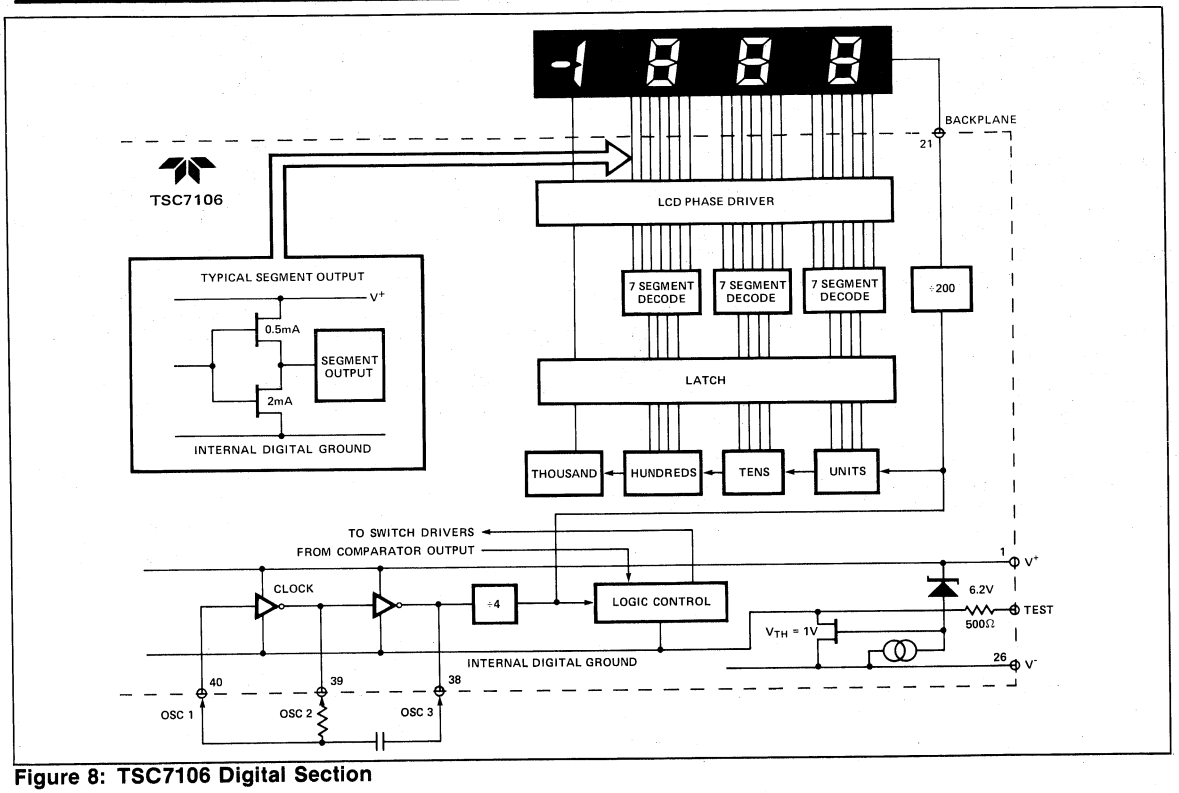


Figure 8: TSC7106 Digital Section

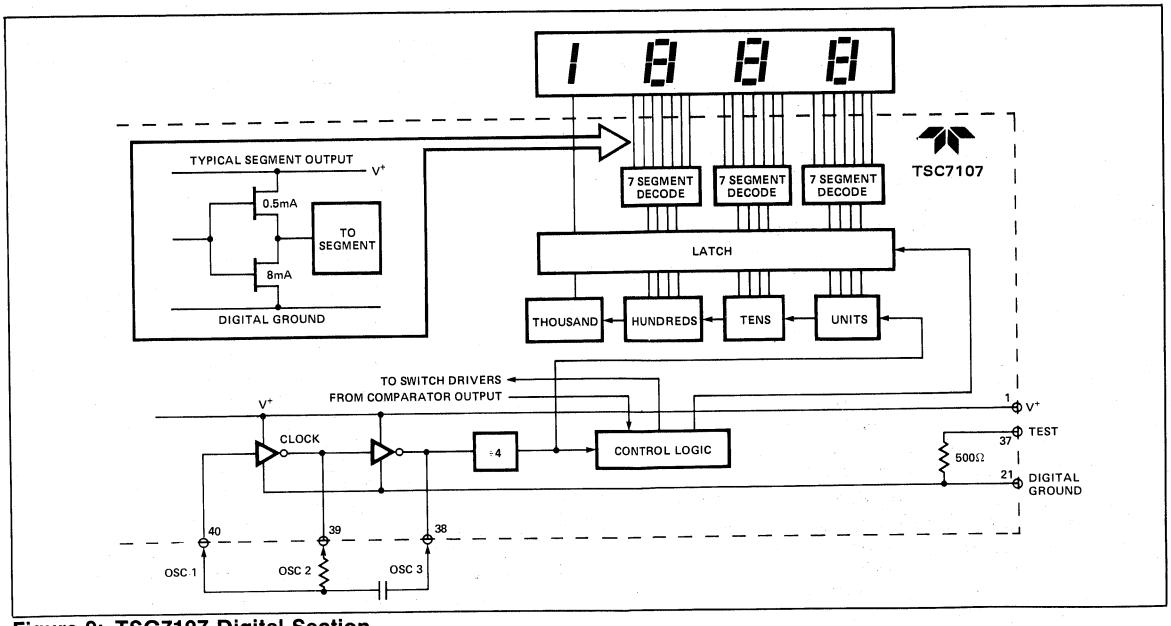


Figure 9: TSC7107 Digital Section

±4 volt swing is nominal. For three readings/second (48 kHz clock) nominal values for C_{INT} are 0.22 μ1F and 0.10 μF, respectively. If different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the output swing.

The integrating capacitor must have low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are recommended for this application.

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100 μA of quiescent current. They can supply 20 μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full-scale, 470 kΩ is near optimum and similarly a 47 kΩ for a 200.0 mV scale.

Oscillator Components

For all ranges of frequency a 100 kΩ resistor is recommended and the capacitor is selected from the equation $f = \frac{45}{RC}$ For 48 kHz clock (3 readings/second), C = 100 pF.

Reference Voltage

The analog input required to generate full-scale output (200 counts) is: $V_{IN} = 2\ V_{REF}$. Thus, for the 200.0 mV and 2.000 volt scale, V_{REF} should equal 100.0 mV and 1.00 volt respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full-scale reading when the voltage form the transducer is 0.682 V. Instead of dividing the input down to 200.0 mV, the designer should use the input voltage directly and select V_{REF} = 0.341 V. Suitable values for integrating resistor and capacitor would be 120 kΩ and 0.22 μF. This makes the system slightly quieter and also avoids a divider network on the input. The TSC7107 with ±5 V supplies can accept input signals up to ±4 V. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between V_{IN}^{+} and common and the variable (or fixed) offset voltage between common and V_{IN}^{-}.

TSC7107 Power Supplies

The TSC7107 is designed to work from ±5 V supplies. However, if a negative supply is not available, it can be generated from the clock output with two diodes, two capacitors and an inexpensive IC. Figure 10 shows this application.

In selected applications no negative supply is required. The conditions to use a single +5 V supply are:

- The input signal can be referenced to the center of the common-mode range of the converter.
- The signal is less than ±1.5 volts.
- An external reference is used.

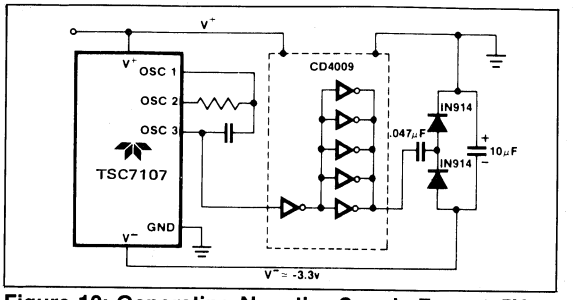


Figure 10: Generating Negative Supply From + 5V

Typical Applications

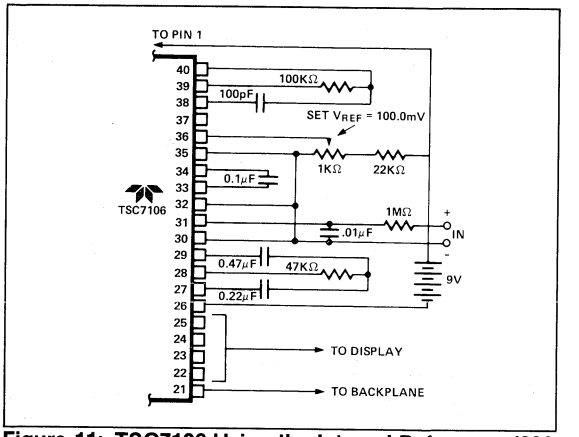


Figure 11: TSC7106 Using the Internal Reference. (200 mV Full-Scale, 3 RPS).

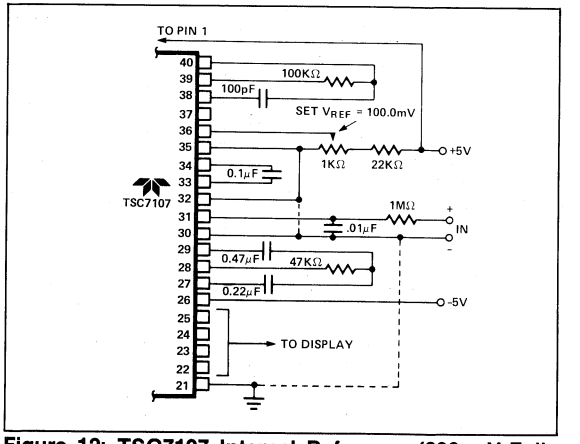


Figure 12: TSC7107 Internal Reference (200 mV Full-Scale, 3 RPS, V_{IN}^{-} Tied to GND for Single Ended Inputs).

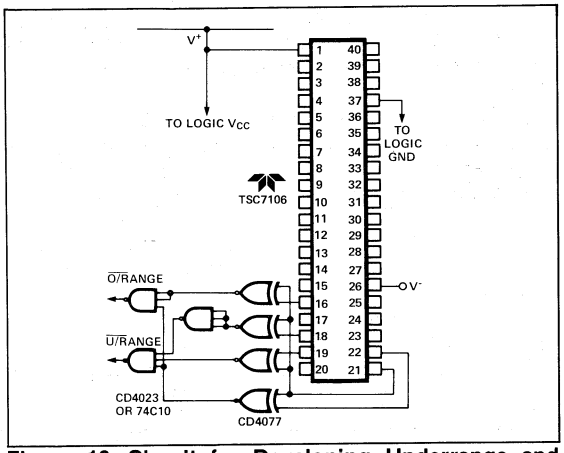


Figure 13: Circuit for Developing Underrange and Overrange Signals from TSC7106 Outputs.

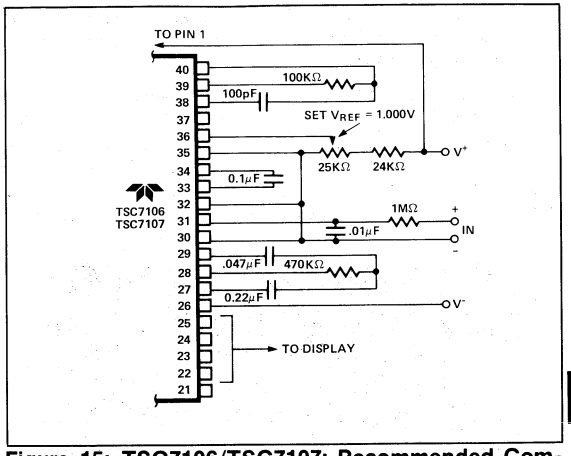


Figure 15: TSC7106/TSC7107: Recommended Component Values for 2.00 V Full-Scale.

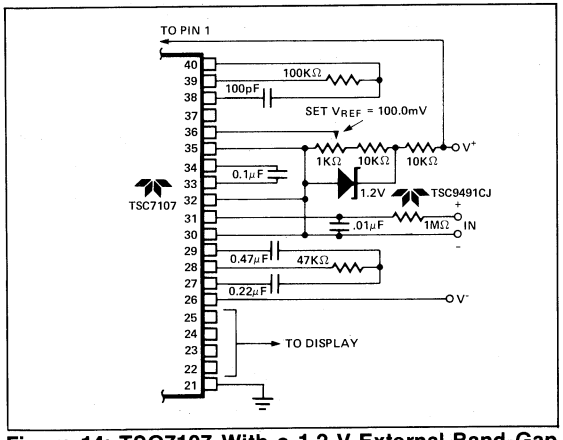


Figure 14: TSC7107 With a 1.2 V External Band-Gap Reference. V_{IN} Tied to Common).

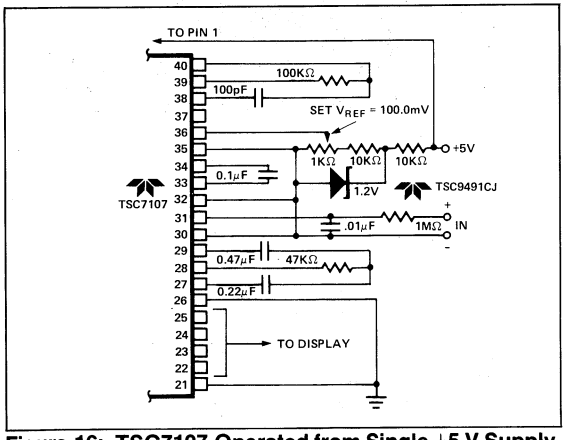


Figure 16: TSC7107 Operated from Single +5 V Supply. An External Reference Must Be Used in This Application.

Applications Information

The TSC7107 sinks the LED display current and this causes heat to build up in the IC package. If the internal voltage reference is used, the changing chip temperature can cause the display to change reading. By reducing package power dissipation such variations can be reduced. By reducing the LED common anode voltage the TSC7107 package power dissipation is reduced.

Figure 17 is a photograph of a curve-tracer display showing the relationship between output current and output voltage for a typical TSC7107CPL. Since a typical LED has 1.8 volts across it at 8 mA, and its common anode is connected to +5 V, the TSC7107 output is at 3.2 V (point A on Fig. 17). Maximum power dissipation is 8.1 mA X 3.2 V X 24 segments = 622 mW.

Notice, however, that once the TSC7107 output voltage is above two volts, the LED current is essentially constant as output voltage increases. Reducing the output voltage by 0.7 V (point B of Figure 17) results in 7.7 mA of LED current, only a 5 percent reduction. Maximum power dissipation is now only 7.7 mA X 2.5 V X 24 = 462 mW, a reduction of 26%. An output voltage reduction of 1 volt (point C) reduces LED current by 10% (7.3 mA) but power dissipation by 38%! (7.3 mA X 2.2 V X 24 = 385 mW).

Reduced power dissipation is very easy to obtain. Fig. 18 shows two ways: either a 5.1 ohm, 1/4 watt resistor or a 1 Amp diode placed in series with the display (but not in series with the TSC7107). The resistor will reduce the TSC7107 output voltage, when all 24 segments are "ON," to point "C" of Fig.

17. When segments turn off, the output voltage will increase. The diode, on the other hand, will result in a relatively steady output voltage, around point "B."

In addition to limiting maximum power dissipation, the resistor reduces the change in power dissipation as the display changes. This effect is caused by the fact that, as fewer segments are "ON," each "ON" output drops more voltage and current. For the best case of six segments (a "111" display) to worst case (a "1888" display) the resistor circuit will change about 230 mW, while a circuit without the resistor will change about 470 mW. Therefore, the resistor will reduce the effect of display dissipation on reference voltage drift by about 50%.

The change in LED brightness caused by the resistor is almost unnoticeable as more segments turn off. If display brightness remaining steady is very important to the designer, diode may be used instead of the resistor.

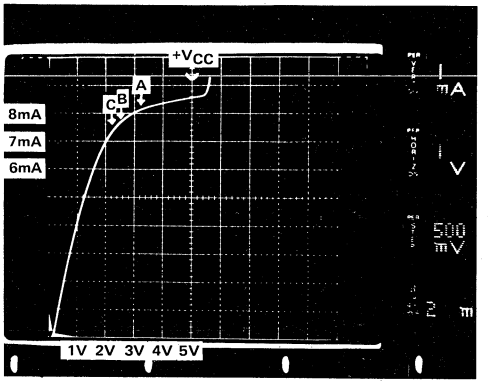


Figure 17: TSC7107 Output Current vs Output Voltage

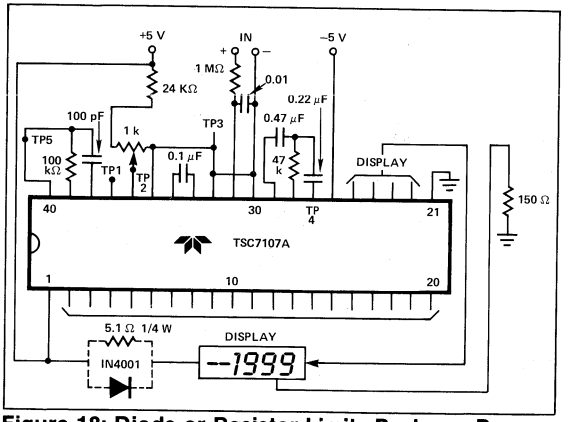
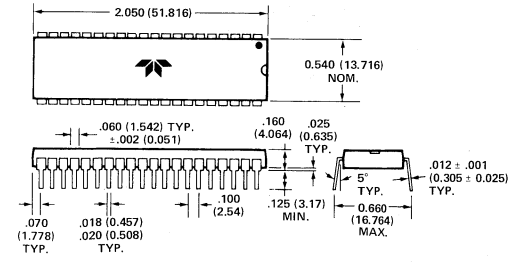
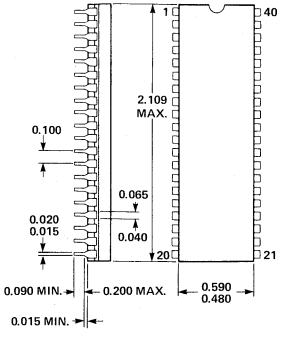


Figure 18: Diode or Resistor Limits Package Power Dissipation

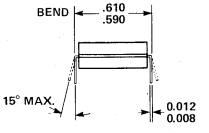
Package Information

40-Pin Plastic Dual-In-Line Package (Package #17)

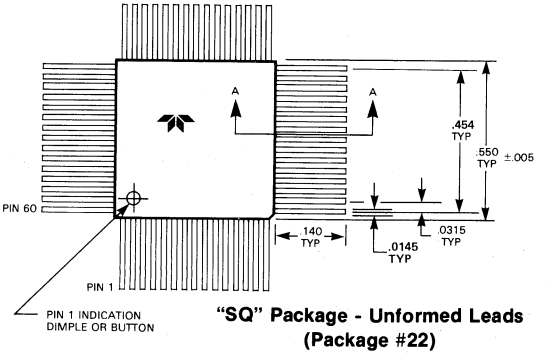




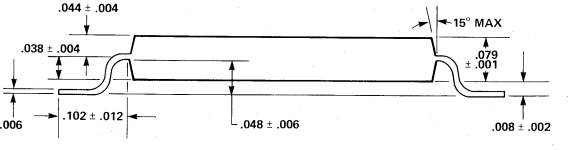
40-Pin CerDIP (Package #20)



60-Pin Flat Package



"SQ" Package - Unformed Leads (Package #22)



"BQ" Package - Formed Leads (Package #21)

TSC7116A (LCD Drive)
TSC7117A (LED Drive)
3 1/2 Digit A/D Converter
• Low Drift Voltage Reference
• Display Hold Function

General Description

The TSC7116A and TSC7117A 3-1/2 digit CMOS analog-to-digital converters contain all the active components necessary to construct a 0.05% resolution measurement system. Seven segment decoders, polarity and digit drivers, voltage reference and clock circuit are integrated on chip. The TSC7116A drives liquid crystal displays (LCD) and includes a backplane driver. The TSC7117A drives common anode light emitting diode (LED) displays directly with an 8 mA drive current per segment.

The TSC7116A/TSC7117A incorporate the display hold (HLDR) function. The displayed reading will remain indefinitely as long as HLDR is held high. Conversions continue but the output data display latches are not updated. The V_{REF}^- or reference low input is not available as it is with the TSC7106/TSC7107. V_{REF}^- is tied internally to analog common in the TSC7116A/TSC7117A devices.

The TSC7116A/TSC7117A feature a precision low drift internal reference. A low drift external reference voltage is normally not required. Existing 7116/7117 systems may be upgraded without changing external components.

The TSC7116A/TSC7117A reduce linearity error to less than 1 count. Rollover error—the difference in readings for equal magnitude but opposite polarity input signals — is below ±1 count. High impedance differential inputs offer 1 pA leakage current and a $10^{12}\ \Omega$ input impedance. The 15 μVp-p noise performance guarantees a "rock solid" reading. The auto-zero cycle guarantees a zero display reading with a zero volt input.

Features

- Internal Reference with Low Temperature Drift ..... 20 ppm/°C Typical, 50 ppm/°C Maximum
- Display Hold Function
- Drives LCD or LED Displays Directly
- Guaranteed Zero Reading with Zero Input
- Low Noise for Stable Display -2.000 V or 200.0 mV Full-Scale Range
- Auto-Zero Cycle Eliminates Need for Zero Adjustment Potentiometer
- True Polarity Indication for Precision Null Applications
- Convenient 9 V Battery Operation (TSC7116A)
- High Impedance CMOS Differential Inputs ..... $10^{12}\ \Omega$
- Low Power Operation ..... 10 mW

The TSC7116A/TSC7117A dual slope conversion technique automatically rejects interference signals if the converters integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400 Hz line frequency signals are present.

The TSC7116A/TSC7117A are available in a small 60-pin flat package for compact designs. Standard devices are offered in an industrial temperature range and with burn-in lasting for 160 hours at +125° C.

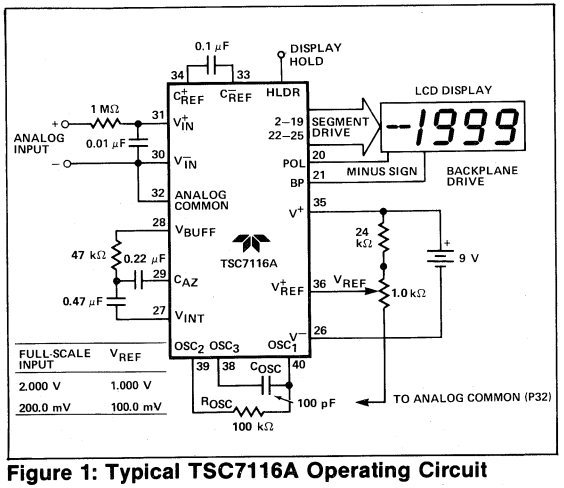


Figure 1: Typical TSC7116A Operating Circuit

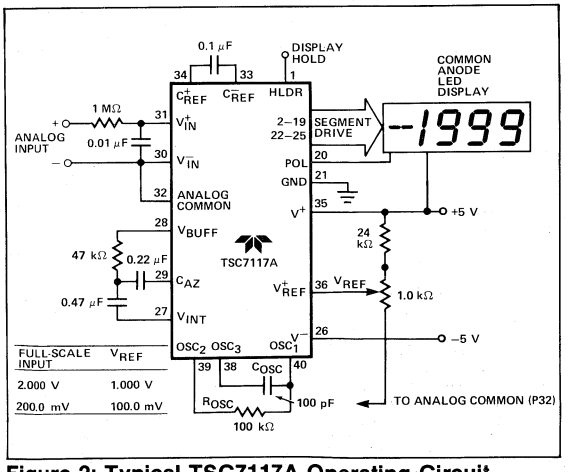


Figure 2: Typical TSC7117A Operating Circuit

Absolute Maximum Ratings

TSC7116A

Supply Voltage (V^+ to V^-) ..... 15 V
Analog Input Voltage (either input) (Note 1) .... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... Test to V^+
Power Dissipation (Note 2)
  CerDIP Package ..... 1000 mW
  Plastic Package ..... 800 mW
Operating Temperature
  "C" Devices ..... 0°C to +70°C
  "I" Devices ..... -25°C to +85°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may effect device reliability.

TSC7117A

Supply Voltage
  V^+ ..... +6 V
  V^- ..... -9 V
Analog Input Voltage (either input) (Note 1) .... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... GND to V^+
Power Dissipation (Note 1)
  CerDIP Package ..... 1000 mW
  Plastic Package ..... 800 mW
Operating Temperature
  "C" Devices ..... 0°C to +70°C
  "I" Devices ..... -25°C to +85°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Electrical Characteristics (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	V_{IN} = 0.0 V Full-Scale = 200.0 mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in Reading for Equal Positive and Negative Reading Near Full-Scale)	$-V_{IN} = +V_{IN} \approx$ 200.0 mV or ≈ 2.000 V	-1	±0.2	+1	Counts
Linearity (Max. Deviation From Best Straight Line Fit)	Full-Scale = 200 mV or Full-Scale = 2.000 V	-1	±0.2	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1 V, V_{IN} = 0 V. Full-Scale = 200.0 mV	—	50	—	µV/V
Noise (Pk - Pk Value Not Exceeded 95% of Time)	V_{IN} = 0 V Full-Scale = 200.0 mV	—	15	—	µV
Leakage Current @ Input	V_{IN} = 0 V	—	1	10	pA
Zero Reading Drift	V_{IN} = 0 V "C" Device = 0°C to 70°C	—	0.2	1	µV/°C
	V_{IN} = 0 V "I" Device = -25°C to +85°C	—	1.0	2	
Scale Factor Temperature Coefficient	V_{IN} = 199.0 mV, "C" Device = 0°C to 70°C (Ext. Ref = 0 ppm/°C)	—	1	5	ppm/°C
	V_{IN} = 199.0 mV "I" Device: -25°C to +85°C	—	—	20	ppm/°C
Input Resistance, Pin 1 (Note 6)		30	70	—	kΩ
V_{IL}, Pin 1 (TSC7116A only)		—	—	Test +1.5	V
V_{IL}, Pin 1 (TSC7117A only)		—	—	GND +1.5	V
V_{IH}, Pin 1 (Both)		V^+ -1.5	—	—	V
Supply Current (Does Not Include LED Current for 7117A)	V_{IN} = 0	—	0.8	1.8	mA
Analog Common Voltage (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply	2.7	3.05	3.35	V
Temp. Coeff. of Analog Common (With Respect to Pos. Supply)	"C" Devices: 0°C to +70°C	—	20	50	ppm/°C
Temp. Coeff. of Analog Common (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply "I" Devices: -25°C to +85°C	—	—	75	ppm/°C

Electrical Characteristics (Cont.)

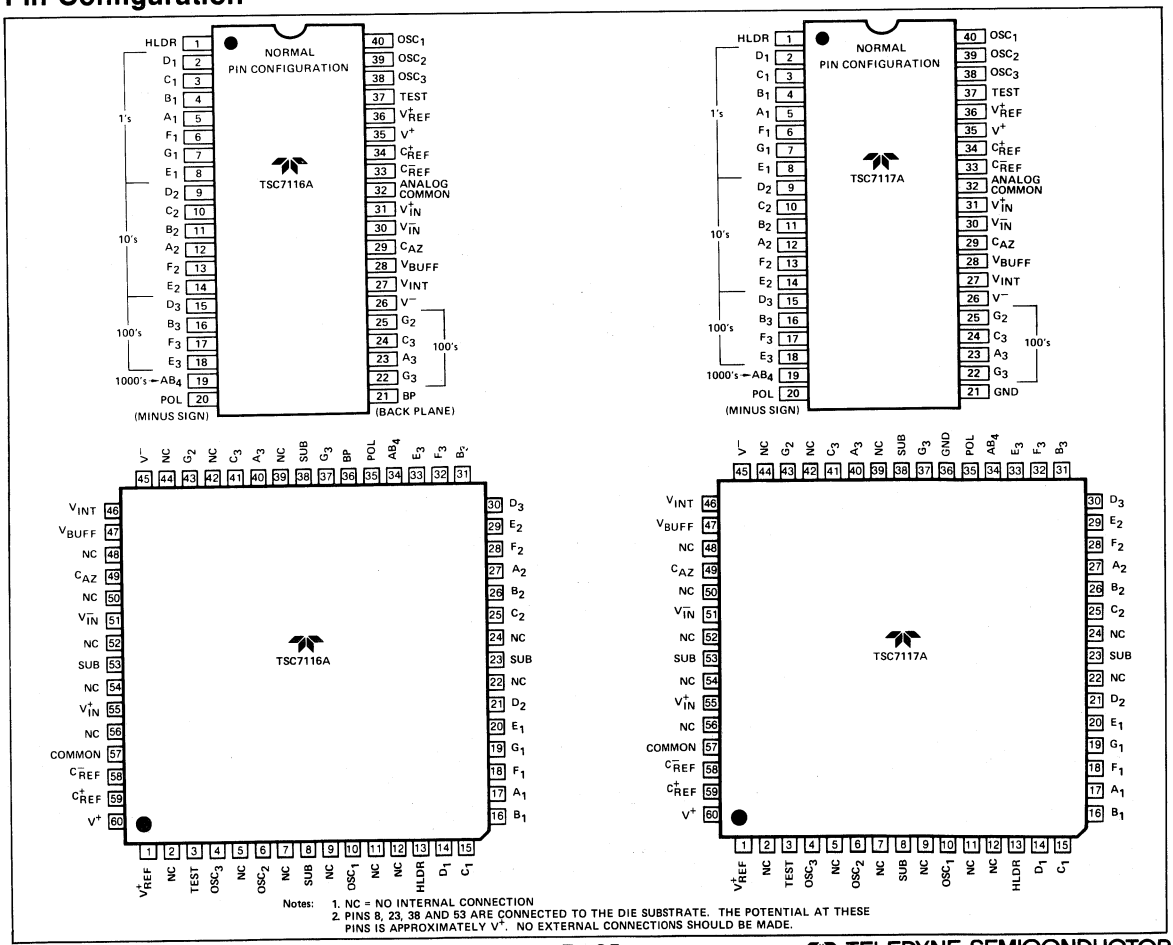
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
TSC7116A ONLY Pk - Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V
TSC7116A ONLY Pk - Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V
TSC7117A ONLY Segment Sinking Current (Except Pin 19)	V^+ = 5.0 V Segment Voltage = 3 V	5	8.0	—	mA
TSC7117A ONLY Segment Sinking Current (Pin 19 Only)	V^+ = 5.0 V Segment Voltage = 3 V	10	16	—	mA

NOTES:

1. Input voltages may exceed the supply voltages provided the input current is limited to ± 100 μA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Unless other wise noted, specifications apply to both the TSC7116A and TSC7117A at T_A = 25° C, f_{CLOCK} = 48 kHz. TSC7116A is tested in the circuit of Figure 1. TSC7117A is tested in the circuit of Figure 2.
4. Refer to "Differential Input" discussion.
5. Backplane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average dc component is less than 50 mV.
6. The TSC7116A logic input has an internal pull-down resistor connected from HLDR, Pin 1, to TEST, Pin 37. The TSC7117A logic input has an internal pull-down resistor connected from HLDR, Pin 1 to GROUND, Pin 21.

7

Pin Configuration



Notes: 1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V^+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

Ordering Information

Part No.	Package	Pin Layout	Temp. Range	Display Drive
TSC7116ACPL	40-Pin Plastic Dip	Normal	0°C to +70°C	LCD
TSC7116AIJL	40-Pin CerDIP	Normal	-25°C to +85°C	LCD
TSC7116ACBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LCD
TSC7116ACSQ	60-Pin Plastic Flat Package	Unformed Leads	0°C to +70°C	LCD
TSC7117ACPL	40-Pin Plastic Dip	Normal	0°C to +70°C	LED
TSC7117AIJL	40-Pin CerDIP	Normal	-25°C to +85°C	LED
TSC7117ACBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LED
TSC7117ACSQ	60-Pin Plastic Flat Package	Unformed Leads	0°C to +70°C	LED
Devices with Burn-In (160 Hours at +125°C)				
TSC7116ACPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C	LCD
TSC7117ACPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C	LED

Pin Description

40-Pin DIP Pin Number Normal	60-Pin Flat Package Pin Number	Name	Description
1	13	HLDR	Hold Pin, Logic 1 holds present display reading.
2	14	D_1	Activates the D section of the units display.
3	15	C_1	Activates the C section of the units display.
4	16	B_1	Activates the B section of the units display.
5	17	A_1	Activates the A section of the units display.
6	18	F_1	Activates the F section of the units display.
7	19	G_1	Activates the G section of the units display.
8	20	E_1	Activates the E section of the units display.
9	21	D_2	Activates the D section of the units display.
10	25	C_2	Activates the C section of the tens display.
11	26	B_2	Activates the B section of the tens display.
12	27	A_2	Activates the A section of the tens display.
13	28	F_2	Activates the F section of the tens display.
14	29	E_2	Activates the E section of the tens display.
15	30	D_3	Activates the D section of the hundreds display.
16	31	B_3	Activates the B section of the hundreds display.
17	32	F_3	Activates the F section of the hundreds display.
18	33	E_3	Activates the E section of the hundreds display.
19	34	AB_4	Activates both halves of the 1 in the thousands display.
20	35	POL	Activates the negative polarity display.
21	36	BP GND	TSC7116A: LCD Backplane drive output. TSC7117A: Digital Ground.
22	37	G_3	Activates the G section of the hundreds display.
23	40	A_3	Activates the A section of the hundreds display.
24	41	C_3	Activates the C section of the hundreds display.
25	43	G_2	Activates the G section of the tens display.
26	45	V^-	Negative power supply voltage.
27	46	V_{INT}	Integrator output. Connection point for integration capacitor. See INTEGRATING CAPACITOR section for additional details.
28	47	V_{BUFF}	Integration resistor connection. Use a 47 kΩ for a 200 mV full-scale range and a 470 kΩ for 2 V full-scale range.

Pin Description (Cont.)

40-Pin DIP Pin Number Normal	60-Pin Flat Package Pin Number	Name	Description
29	49	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.47 μF capacitor for a 200 mV full-scale, and a 0.047 μF capacitor for a 2 volt full-scale. See paragraph on AUTO-ZERO CAPACITOR for more details.
30	51	V_{IN}^-	The analog low input is connected to this pin.
31	55	V_{IN}^+	The analog high input signal is connected to this pin.
32	57	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on ANALOG COMMON for more details. It also acts as a reference voltage source.
33	58	C_{REF}^-	See pin 34.
34	59	C_{REF}^+	A 0.1 μF capacitor is used in most applications. If a large common-mode voltage exists (for example the V_{IN} pin is not at analog common), and a 200 mV scale is used, a 1.0 μF is recommended and will hold the rollover error to 0.5 count.
35	60	V^+	Positive Power Supply Voltage.
36	1	V_{REF}^+	The analog input required to generate a full-scale output (1,999 counts). Place 100 mV between pins 32 and 36 for 199.9 mV full-scale. Place 1.00 volts between pins 32 and 36 for 2 volts full-scale. See paragraph on REFERENCE VOLTAGE.
37	3	Test	Lamp test. When pulled high (to V^+) all segments will be turned on and the display should read -1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38	4	OSC_3	See pin 40.
39	6	OSC_2	See pin 40.
40	10	OSC_1	Pins 40, 39, 38 make up the oscillator section. For a 48 kHz clock (3 readings per section) connect pin 40 to the junction of a 100 kΩ resistor and a 100 pF capacitor. The 100 kΩ resistor is tied to pin 39 and the 100 pF capacitor is tied to pin 38.

Analog Section

Figure 3 shows the Block Diagram of the Analog Section for the TSC7116A and TSC7117A. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) reference (REF).

Auto-Zero Phase

Input high and low are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. The offset referred to the input is less than 10 μV.

Signal Integrate Phase

The auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between V_{IN}^+ and V_{IN}^- for a fixed time. This differential voltage can be within a wide common-mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, V_{IN}^- can be tied to analog common to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

Reference Integrate Phase

The final phase is reference integrate or de-integrate. Input low is internally connected to analog common and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Reference

The positive reference voltage (V_{REF}^+) is referenced to analog common.

Differential Input

The input can accept differential voltages anywhere within the common-mode range of the input amplifier; or specifically from 1.0 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worse case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of

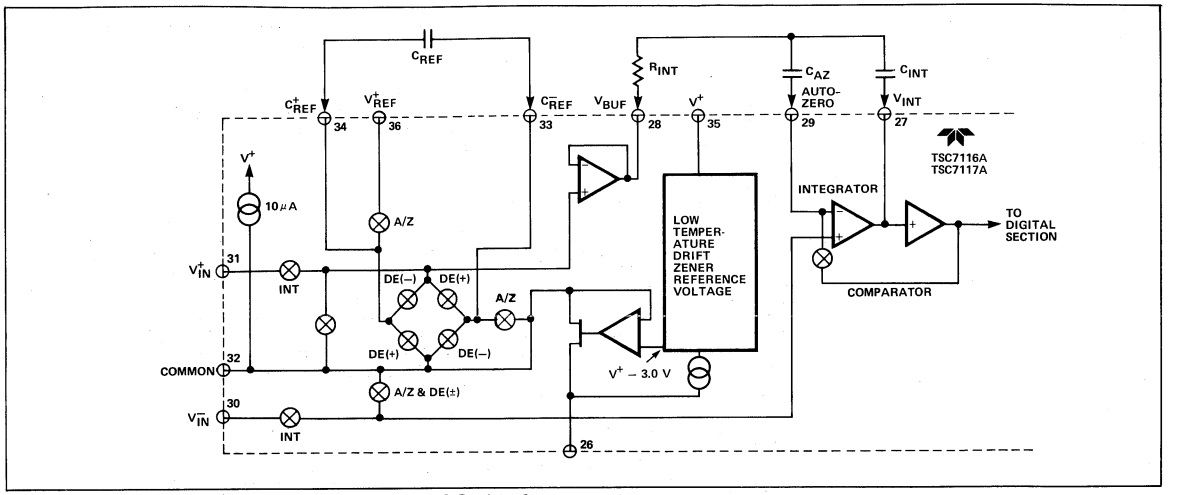


Figure 3: Analog Section of TSC7116A/TSC7117A

its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2 V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

Analog Common

This pin is included primarily to set the common-mode voltage for battery operation (TSC7116A) or for any system where the input signals are floating with respect to the power supply. The common pin sets a voltage that is approximately 3.0 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6 V. However, the analog common has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7 V), the common voltage will have a low voltage coefficient (0.001%/%), low output impedance (≈15 Ω), and a temperature coefficient of 20 ppm/° C typically.

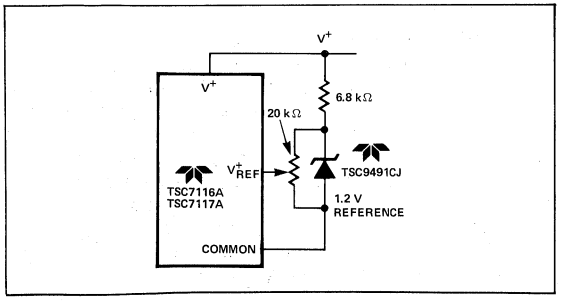


Figure 4: Using an External Reference

An external reference may be may be used if necessary. The circuit is shown in Figure 4.

Analog common is also used as the V_{IN}^- return during auto-zero and deintegrate. If V_{IN}^- is different from analog common, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications V_{IN}^- will be set at a fixed known voltage (power supply common for instance). In this application, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog common, it should be since this removes the common-mode voltage from the reference system.

Within the IC, analog common is tied to an N-channel FET that can sink 30 mA or more of current to hold the voltage 3.0 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10 μA of source current, so common may easily be tied to a more negative voltage thus over-riding the internal reference.

Test

The TEST pin serves two functions. On the TSC7117A it is coupled to the internally generated digital supply through a 500 Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1 mA load should be applied.

The second function is a "lamp test." When TEST is pulled high (to V^+) all segments will be turned on and the display should read -1888. The TEST pin will sink about 10 mA under these conditions.

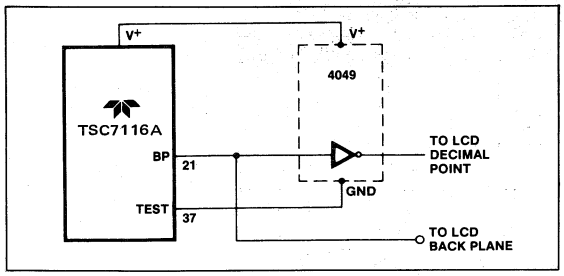


Figure 5: Simple Inverter for Fixed Decimal Point

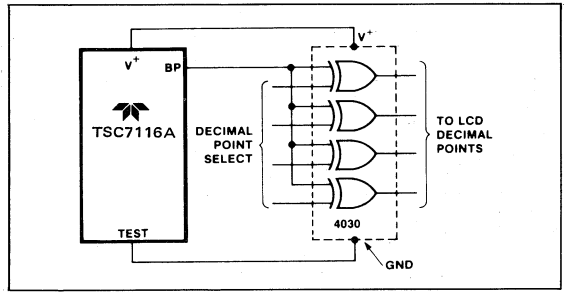


Figure 6: Exclusive "OR" Gate for Decimal Point Drive

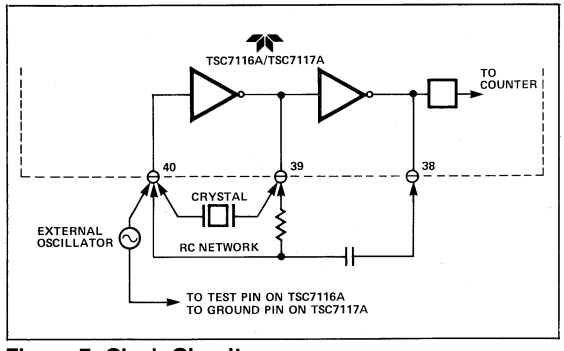


Figure 7: Clock Circuits

Digital Section

Figures 8 and 9 show the digital section for the TSC7116A and TSC7117A, respectively. In the TSC7116A (Figure 8), an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases, negligible dc voltage exists across the segments.

Figure 9 is the Digital Section of the TSC7117A. It is identical to the TSC7116A except that the regulated supply and back plane drive have been eliminated and the segment drive is typically 8 mA. The 1000 output (pin 19) sinks current from two LED segments, and has a 16 mA drive capability. The TSC7117A is designed to drive common anode LEDs.

In both devices, the polarity indication is "on" for negative analog inputs. If V_{IN}^- and V_{IN}^+ are reversed, this indication can be reversed also, if desired.

System Timing

Figure 9 shows the clocking method used in the TSC7116A and TSC7117A. Three clocking methods may be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An RC oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full-scale auto-zero gets the unused portion of reference de-integrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48 kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 48 kHz, 40 kHz, 33-1/3 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66-2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

HOLD Reading Input

When HLDR is at a logic "HI" the latch will not be updated. A/D conversions will continue but will not be updated until the HLDR is returned to "LOW". To continuously update the display connect to TEST (TSC7116A) or GROUND (TSC7117A) or disconnect. This input is CMOS compatible with 70K typical resistance to TEST (TSC7116A) or GROUND (TSC7117A).

Component Value Selection

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full-scale where noise is very important, a 0.47 μF capacitor is recommended. On the 2 volt scale, a 0.047 μF capacitor increase the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1 μF capacitor is acceptable in most applications. However, where a large common-mode voltage exists (i.e. the V_{IN}^- pin is not at analog common) and a 200 mV scale is used, a large value is required to prevent to roll-over error. Generally 1.0 μF will hold the roll-over error to 0.5 count in this instance.

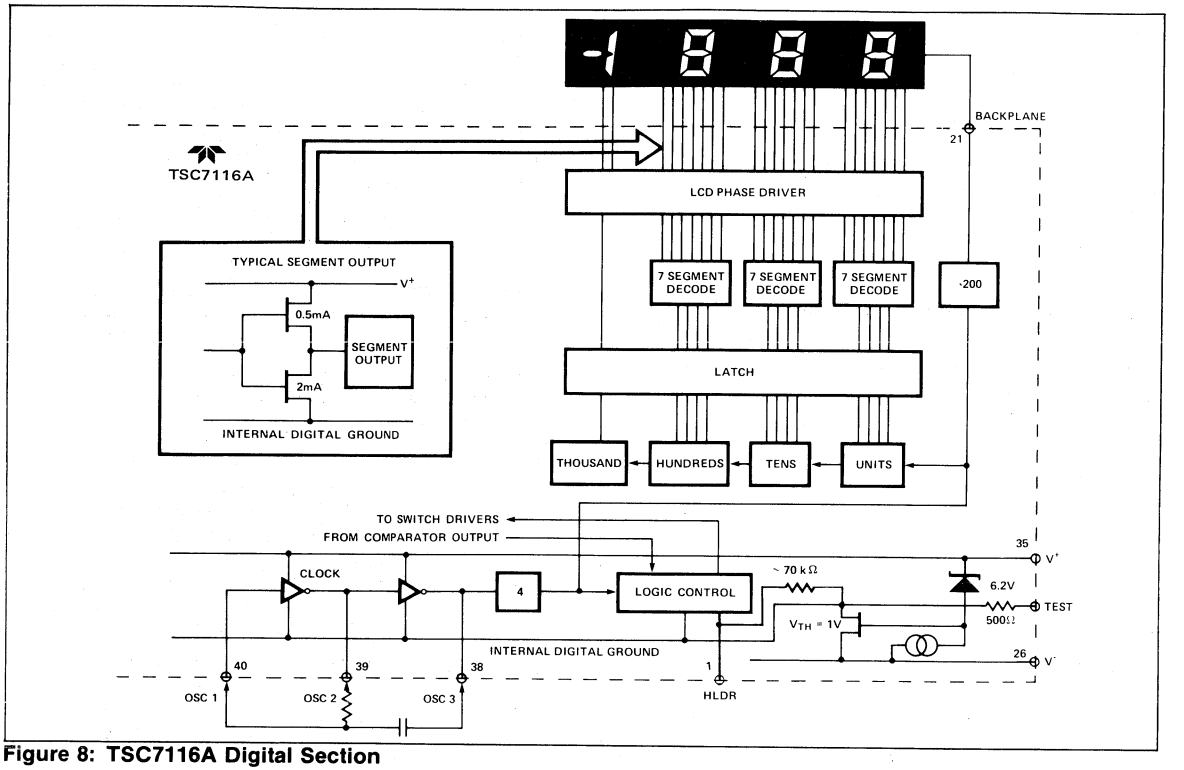


Figure 8: TSC7116A Digital Section

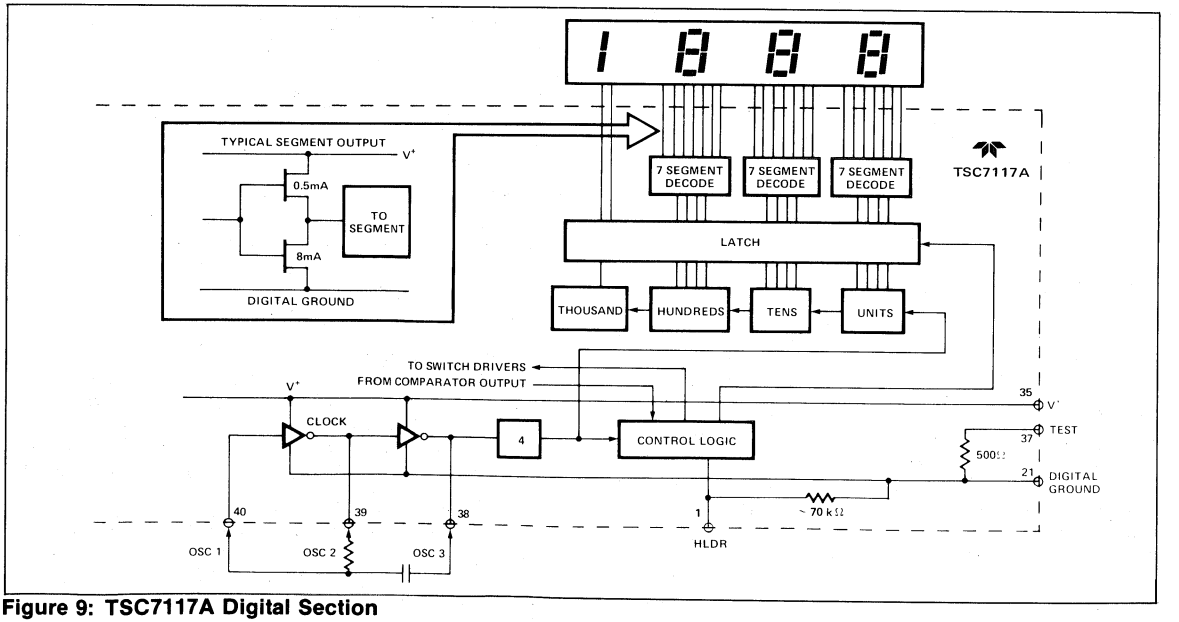


Figure 9: TSC7117A Digital Section

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the TSC7116A or the TSC7117A, when the analog common is used as a reference, a nominal ±2 volt full-scale integrator swing is acceptable. For the TSC7117A with ±5 volt supplies and analog common tied to supply ground, a ±3.5 to ±4 volt swing is nominal. For three readings/second (48 kHz clock) nominal values for C_{INT} are 0.22 μF and 0.10 μF, respectively. If different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the output swing.

The integrating capacitor must have low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are recommended for this application.

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100 μA of quiescent current. They can supply 20 μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full-scale, 470 kΩ is near optimum and similarly a 47 kΩ for a 200.0 mV scale.

Oscillator Components

For all ranges of frequency a 100 kΩ resistor is recommended and the capacitor is selected from the equation $f = \frac{45}{RC}$. For 48 kHz clock (3 readings/second), C = 100 pF.

Reference Voltage

To generate full-scale output (2000 counts) the analog input required is: $V_{IN} = 2\,V_{REF}$. Thus, for the 200.0 mV and 2.000 volt scale, V_{REF} should equal 100.0 mV and 1.00 volt respectively. In many applications where the A/D is connected to a transducer, there will exist a scale factor between the input voltage and the digital reading. For instance, in a measuring system, the designer might like to have a full-scale reading when the voltage from the transducer is 700 mV. Instead of dividing the input down to 200.0 mV, the designer should use the input voltage directly and select $V_{REF} = 350$ mV. Suitable values for integrating resistor and capacitor would be 120 kΩ and 0.22 μF. This makes the system slightly quieter and also avoids a divider network on the input. The TSC7117A with ±5 V supplies can accept input signals up to ±4 V. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between V_{IN}^+ and common and the variable (or fixed) offset voltage between common and V_{IN}^-.

TSC7117A Power Supplies

The TSC7117A is designed to work from ±5 V supplies. However, if a negative supply is not available, it can be generated from the clock output with two diodes, two capacitors and an inexpensive IC. Figure 10 shows this application.

In selected applications no negative supply is required. The conditions to use a single +5 V supply are:

- The input signal can be referenced to the center of the common-mode range of the converter.
- The signal is less than ±1.5 volts.
- An external reference is used.

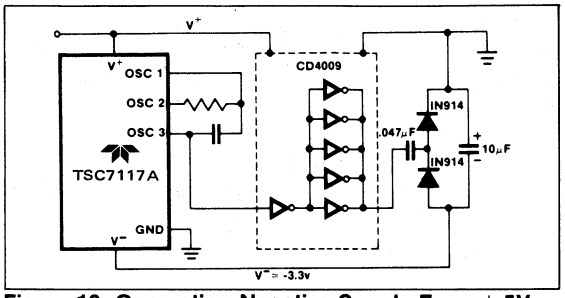


Figure 10: Generating Negative Supply From + 5V

Typical Applications

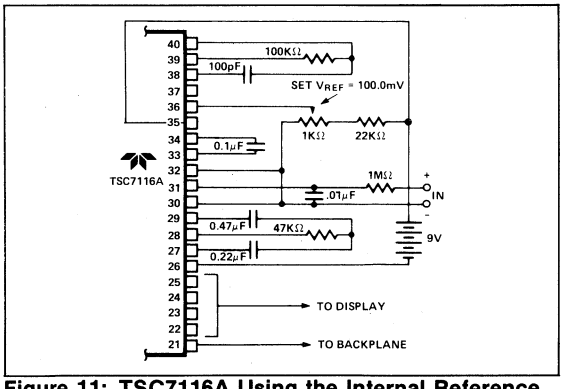


Figure 11: TSC7116A Using the Internal Reference (200 mV Full-Scale, 3 RPS)

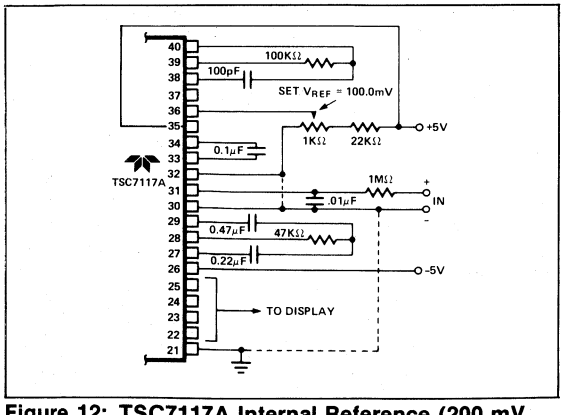


Figure 12: TSC7117A Internal Reference (200 mV Full-Scale, 3 RPS, V_{IN}^- Tied to GND for Single Ended Inputs).

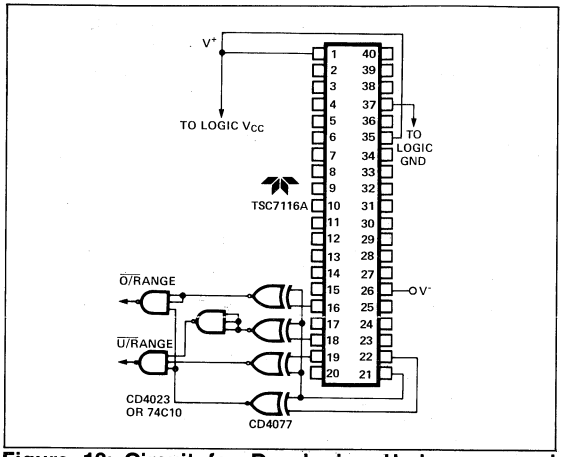


Figure 13: Circuit for Developing Underrange and Overrange Signals from TSC7116A Outputs.

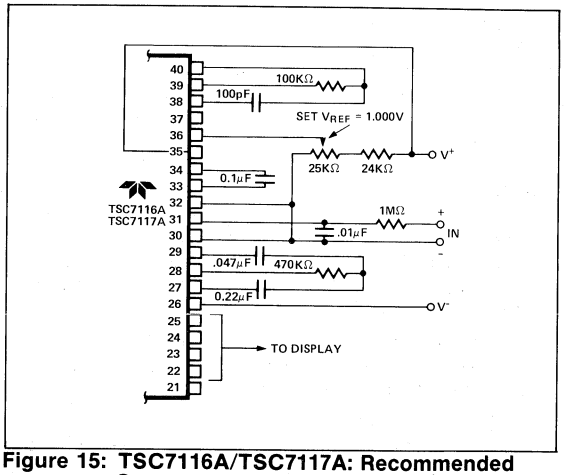


Figure 15: TSC7116A/TSC7117A: Recommended Component Values for 2.00 V Full-Scale.

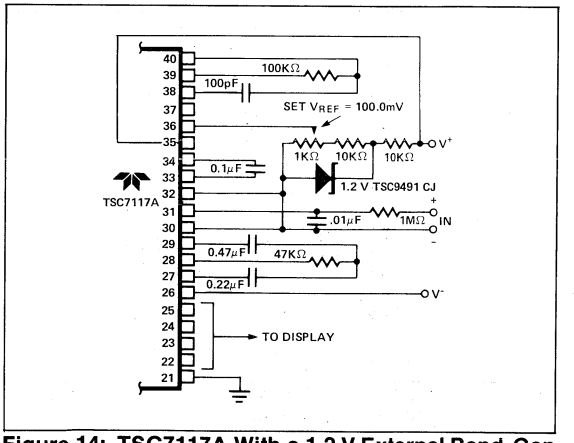


Figure 14: TSC7117A With a 1.2 V External Band-Gap Reference. VIN Tied to Common).

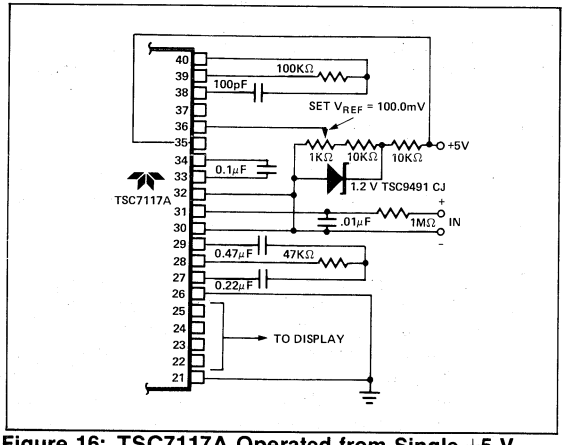


Figure 16: TSC7117A Operated from Single +5 V Supply. An External Reference Must Be Used in This Application.

Applications Information

The TSC7117A sinks the LED display current and this causes heat to build up in the IC package. If the internal voltage reference is used, the changing chip temperature can cause the display to change reading. By reducing package power dissipation such variations can be reduced. By reducing the LED common anode voltage the TSC7117A package power dissipation is reduced.

Figure 17 is a photograph of a curve-tracer display showing the relationship between output current and output voltage for a typical TSC7117ACPL. Since a typical LED has 1.8 volts across it at 8 mA, and its common anode is connected to +5 V, the TSC7117A output is at 3.2 V (point A on Fig. 17). Maximum power dissipation is 8.1 mA X 3.2 V X 24 segments = 622 mW.

Notice, however, that once the TSC7117A output voltage is above two volts, the LED current is essentially constant as output voltage increases. Reducing the output voltage by 0.7 V (point B of Figure 17) results in 7.7 mA of LED current, only a 5 percent reduction. Maximum power dissipation is now only 7.7 mA X 2.5 V X 24 = 462 mW, a reduction of 26%. An output voltage reduction of 1 volt (point C) reduces LED current by 10% (7.3 mA) but power dissipation by 38%! (7.3 mA X 2.2 V X 24 = 385 mW).

Reduced power dissipation is very easy to obtain. Fig. 18 shows two ways: either a 5.1 ohm, 1/4 watt resistor or a 1 Amp diode placed in series with the display (but not in series with the TSC7117). The resistor will reduce the TSC7117A output voltage, when all 24 segments are "ON," to point "C" of Fig.

17. When segments turn off, the output voltage will increase. The diode, on the other hand, will result in a relatively steady output voltage, around point "B."

In addition to limiting maximum power dissipation, the resistor reduces the change in power dissipation as the display changes. This effect is caused by the fact that, as fewer segments are "ON," each "ON" output drops more voltage and current. For the best case of six segments (a "111" display) to worst case (a "1888" display) the resistor circuit will change about 230 mW, while a circuit without the resistor will change about 470 mW. Therefore, the resistor will reduce the effect of display dissipation on reference voltage drift by about 50%.

The change in LED brightness caused by the resistor is almost unnoticeable as more segments turn off. If display brightness remaining steady is very important to the designer, diode may be used instead of the resistor.

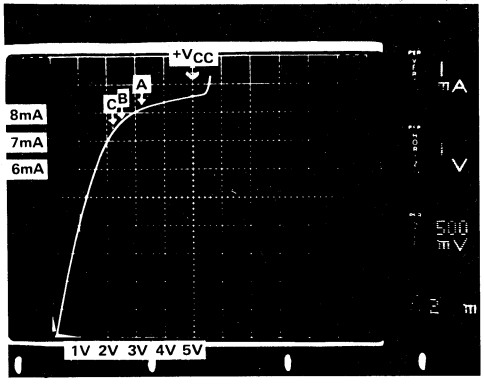


Figure 17: TSC7117A Output Current vs. Output Voltage

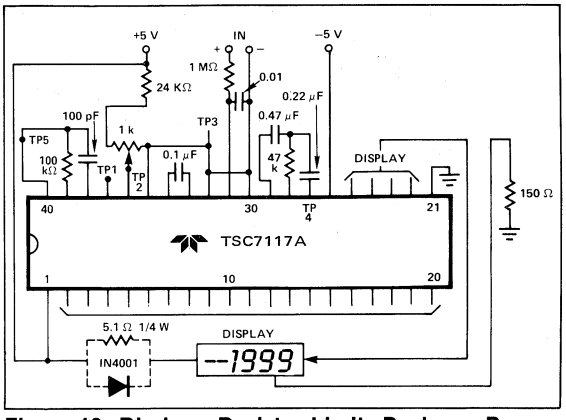
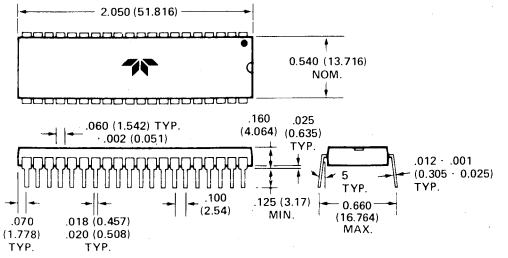


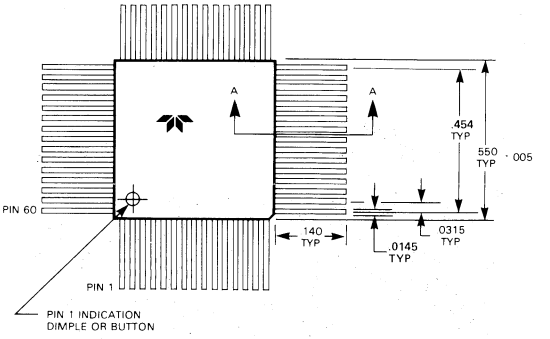
Figure 18: Diode or Resistor Limits Package Power Dissipation

Package Information

40-Pin Plastic Dual-In-Line Package
(Package #17)

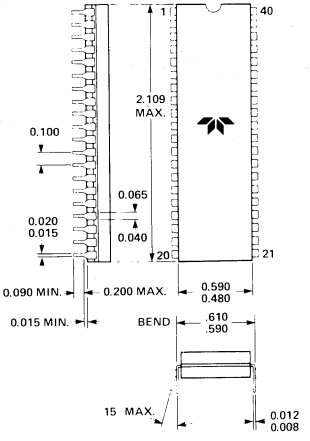


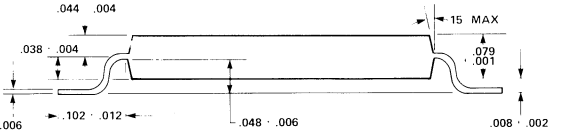
60-Pin Plastic Flat Package



"SQ" Package — Unformed Leads
(Package #22)

40-Pin CerDIP
(Package #20)





"BQ" Package — Formed Leads
(Package #21)

TSC7116 (LCD Drive)
TSC7117 (LED Drive)
3 1/2 Digit A/D Converter
- **Direct Display Drive**
- **Display Hold Function**

General Description

The TSC7116 and TSC7117 3-1/2 digit CMOS analog-to-digital converters contain all the active components necessary to construct a 0.05% resolution measurement system. Seven segment decoders, polarity and digit drivers, voltage reference and clock circuit are integrated on chip. The TSC7116 drives liquid crystal displays (LCD) and includes a backplane driver. The TSC7117 drives common anode light emitting diode (LED) displays directly with an 8 mA drive current per segment.

The TSC7116/TSC7117 incorporates the display hold (HLDR) function. the displayed reading will remain indefinitely as long as HLDR is held high. Conversions continue but the output data display latches are not updated. The V_{REF}^- or reference low input is not available as it is with the TSC7106/TSC7107. V_{REF}^- is tied internally to analog common in the TSC7116/TSC7117 devices.

A low cost, high resolution indicating meter requires only a display, four resistors, and four capicitors. The TSC7116 low power drain and 9 V battery operation make it ideal for portable applications.

The TSC7116/TSC7117 reduce linearity error to less than 1 count. Rollover error — the difference in readings for equal magnitude but opposite polarity input signals — is below ±1 count. High impedance differential inputs offer 1 pA leakage current and a 10^{12} Ω input impedance. The 15 μVp-p noise performance guarantees a "rock solid" reading. The auto-zero cycle guarantees a zero display reading with a zero volt input.

Features

- Display Hold Function
- Drives LCD or LED Displays Directly
- Guaranteed Zero Reading with Zero Input
- Low Noise for Stable Display
  -2.000 V or 200.0 mV Full-Scale Range
- Auto-Zero Cycle Eliminates Need for Zero Adjustment Potentiometer
- True Polarity Indication for Precision Null Applications
- Convenient 9 V Battery Operation (TSC7116)
- High Impedance CMOS Differential Inputs ..... 10^{12} Ω
- Low Power Operation ..... 10 mW

The TSC7116/TSC7117 dual slope conversion technique automatically rejects interference signals if the converters integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400 Hz line frequency signals are present.

The TSC7116/TSC7117 are available in a small 60-pin flat package for compact designs. Standard devices are offered in an industrial temperature range and with burn-in lasting for 160 hours at +125°C.

For applications requiring a more temperature stable internal reference voltage refer to the TSC7116A/7107A data sheets.

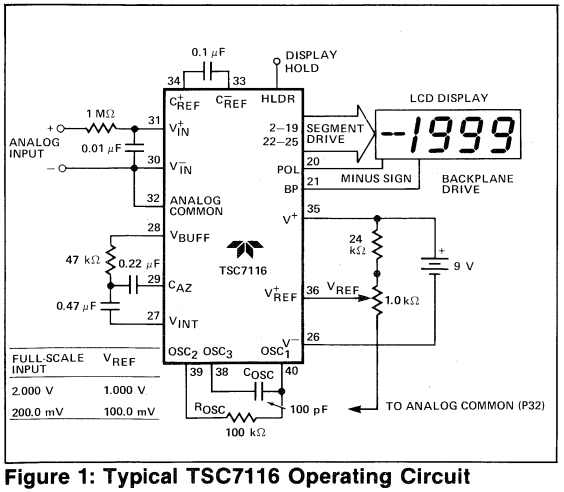


Figure 1: Typical TSC7116 Operating Circuit

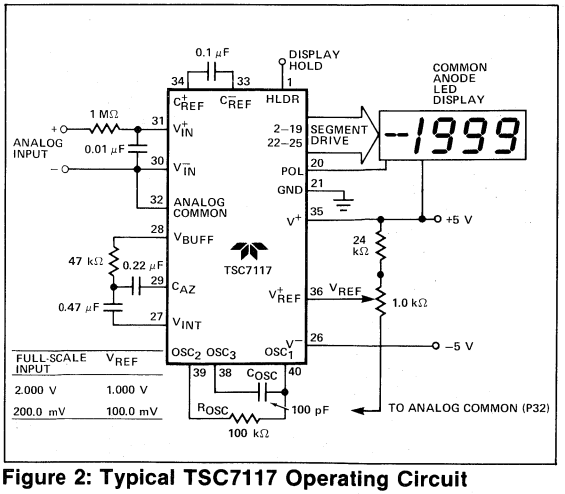


Figure 2: Typical TSC7117 Operating Circuit

Absolute Maximum Ratings

TSC7116

Supply Voltage (V^+ to V^-) ..... 15 V
Analog Input Voltage (either input) (Note 1) .... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... Test to V^+
Power Dissipation (Note 2)
  CerDIP Package ..... 1000 mW
  Plastic Package ..... 800 mW
Operating Temperature
  "C" Devices ..... 0°C to +70°C
  "I" Devices ..... -25°C to +85°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may effect device reliability.

TSC7117

Supply Voltage
  V^+ ..... +6 V
  V^- ..... -9 V
Analog Input Voltage (either input) (Note 1) .... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... GND to V^+
Power Dissipation (Note 1)
  CerDIP Package ..... 1000 mW
  Plastic Package ..... 800 mW
Operating Temperature
  "C" Devices ..... 0°C to +70°C
  "I" Devices ..... -25°C to +85°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Electrical Characteristics (Note 3)

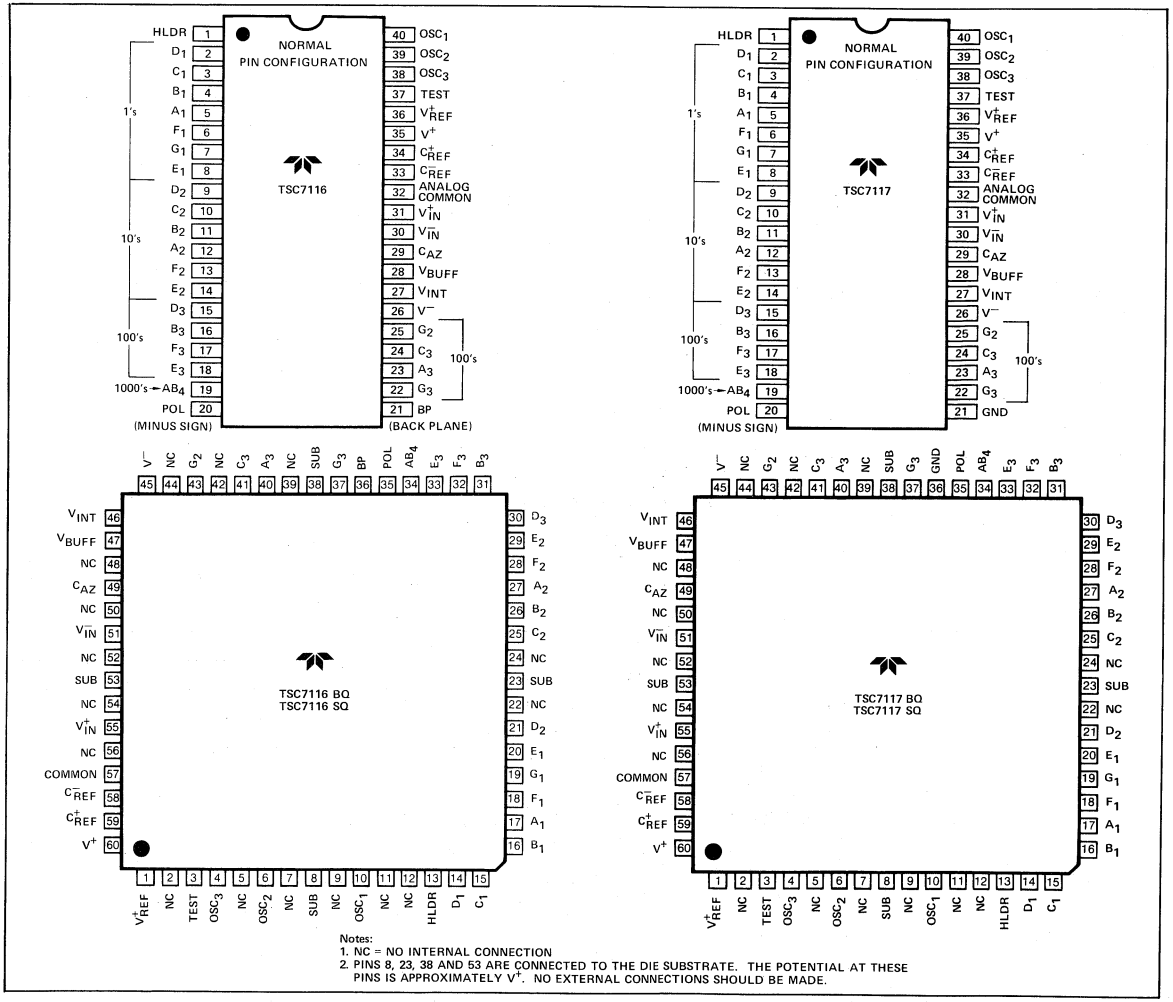
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
Zero Input Reading	V_{IN} = 0.0 V Full-Scale = 200.0 mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in Reading for Equal Positive and Negative Reading Near Full-Scale)	$-V_{IN} = +V_{IN} \approx$ 200.0 mV	-1	±0.2	+1	Counts
Linearity (Max. Deviation From Best Straight Line Fit)	Full-Scale = 200 mV or Full-Scale = 2.000 V	-1	±0.2	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1 V, V_{IN} = 0 V. Full-Scale = 200.0 mV	—	50	—	μV/V
Noise (Pk - Pk Value Not Exceeded 95% of Time)	V_{IN} = 0 V Full-Scale = 200.0 mV	—	15	—	μV
Leakage Current @ Input	V_{IN} = 0 V	—	1	10	pA
Zero Reading Drift	V_{IN} = 0 V "C" Device = 0°C to 70°C V_{IN} = 0 V "I" Device = -25°C to +85°C	— —	0.2 1.0	1 2	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0 mV, "C" Device = 0°C to 70°C (Ext. Ref = 0 ppm/°C) V_{IN} = 199.0 mV "I" Device: -25°C to +85°C	— —	1 —	5 20	ppm/°C ppm/°C
Input Resistance, Pin 1 (Note 6)		30	70	—	kΩ
V_{IL}, Pin 1 (TSC7116 only)		—	—	Test +1.5	V
V_{IL}, Pin 1 (TSC7117 only)		—	—	GND +1.5	V
V_{IH}, Pin 1 (Both)		V^+ -1.5	—	—	V
Supply Current (Does Not Include LED Current for 7107)	V_{IN} = 0	—	0.8	1.8	mA
Analog Common Voltage (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog common (With Respect to Pos. Supply)	25 kΩ Between Common and Pos. Supply	—	80	—	ppm/°C
TSC7116 ONLY Pk - Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V

Electrical Characteristics (Cont.)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
TSC7116 ONLY Pk - Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9 V	4	5	6	V
TSC7117 ONLY Segment Sinking Current (Except Pin 19)	V^+ = 5.0 V Segment Voltage = 3 V	5	8.0	—	mA
TSC7117 ONLY Segment Sinking Current (Pin 19 Only)	V^+ = 5.0 V Segment Voltage = 3 V	10	16	—	mA

NOTES:
1. Input voltages may exceed the supply voltages provided the input current is limited to ± 100 μA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Unless other wise noted, specifications apply to both the TSC7116 and TSC7117 at T_A = 25°C, f_{CLOCK} = 48 kHz. TSC7116 is tested in the circuit of Figure 1. TSC7117 is tested in the circuit of Figure 2.
4. Refer to "Differential Input" discussion.
5. Backplane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average dc component is less than 50 mV.
6. The TSC7116 logic input has an internal pull-down resistor connected from HLDR, Pin 1, to TEST, Pin 37. The TSC7117 logic input has an internal pull-down resistor connected from HLDR, Pin 1 to GROUND, Pin 21.

Pin Configuration



Notes:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V^+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

Ordering Information

Part No.	Package	Pin Layout	Temp. Range	Display Drive
TSC7116CPL	40-Pin Plastic Dip	Normal	0°C to +70°C	LCD
TSC7116IPL	40-Pin Plastic Dip	Normal	-25°C to +85°C	LCD
TSC7116CJL	40-Pin CerDIP	Normal	0°C to +70°C	LCD
TSC7116IJL	40-Pin CerDIP	Normal	-25°C to +85°C	LCD
TSC7116CBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LCD
TSC7116CSQ	60-Pin Plastic Flat Package	Unformed Leads	0°C to +70°C	LCD
TSC7117CPL	40-Pin Plastic Dip	Normal	0°C to +70°C	LED
TSC7117IPL	40-Pin Plastic Dip	Normal	-25°C to +85°C	LED
TSC7117CJL	40-Pin CerDIP	Normal	0°C to +70°C	LED
TSC7117IJL	40-Pin CerDIP	Normal	-25°C to +85°C	LED
TSC7117CBQ	60-Pin Plastic Flat Package	Formed Leads	0°C to +70°C	LED
TSC7117CSQ	60-Pin Plastic Flat Package	Unformed Leads	0°C to +70°C	LED
Devices with Burn-In (160 Hours at +125°C)				
TSC7116CPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C	LCD
TSC7117CPL/BI	40-Pin Plastic Dip	Normal	0°C to +70°C	LED

Pin Description

40-Pin DIP Pin Number	60-Pin Flat Package Pin Number	Name	Description
1	13	HLDR	Hold Pin, Logic 1 holds present display reading.
2	14	D_1	Activates the D section of the units display.
3	15	C_1	Activates the C section of the units display.
4	16	B_1	Activates the B section of the units display.
5	17	A_1	Activates the A section of the units display.
6	18	F_1	Activates the F section of the units display.
7	19	G_1	Activates the G section of the units display.
8	20	E_1	Activates the E section of the units display.
9	21	D_2	Activates the D section of the units display.
10	25	C_2	Activates the C section of the tens display.
11	26	B_2	Activates the B section of the tens display.
12	27	A_2	Activates the A section of the tens display.
13	28	F_2	Activates the F section of the tens display.
14	29	E_2	Activates the E section of the tens display.
15	30	D_3	Activates the D section of the hundreds display.
16	31	B_3	Activates the B section of the hundreds display.
17	32	F_3	Activates the F section of the hundreds display.
18	33	E_3	Activates the E section of the hundreds display.
19	34	AB_4	Activates both halves of the 1 in the thousands display.
20	35	POL	Activates the negative polarity display.
21	36	BP GND	TSC7116: LCD Backplane drive output. TSC7117: Digital Ground.
22	37	G_3	Activates the G section of the hundreds display.
23	40	A_3	Activates the A section of the hundreds display.
24	41	C_3	Activates the C section of the hundreds display.
25	43	G_2	Activates the G section of the tens display.
26	45	V^-	Negative power supply voltage.
27	46	V_{INT}	Integrator output. Connection point for integration capacitor. See INTEGRATING CAPACITOR section for additional details.

Pin Description (Cont.)

40-Pin DIP Pin Number Normal	60-Pin Flat Package Pin Number	Name	Description
28	47	V_{BUFF}	Integration resistor connection. Use a 47 kΩ for a 200 mV full-scale range and a 470 kΩ for 2 V full-scale range.
29	49	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.47 μF capacitor for a 200 mV full-scale, and a 0.047 μF capacitor for a 2 volt full-scale. See paragraph on AUTO-ZERO CAPACITOR for more details.
30	51	V_{IN}^-	The analog low input is connected to this pin.
31	55	V_{IN}^+	The analog high input signal is connected to this pin.
32	57	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on ANALOG COMMON for more details. It also acts as a reference voltage source.
33	58	C_{REF}^-	See pin 34.
34	59	C_{REF}^+	A 0.1 μF capacitor is used in most applications. If a large common-mode voltage exists (for example the V_{IN} pin is not at analog common), and a 200 mV scale is used, a 1.0 μF is recommended and will hold the rollover error to 0.5 count.
35	60	V^+	Positive Power Supply Voltage.
36	1	V_{REF}^+	The analog input required to generate a full-scale output (1,999 counts). Place 100 mV between pins 32 and 36 for 199.9 mV full-scale. Place 1.00 volts between pins 32 and 36 for 2 volts full-scale. See paragraph on REFERENCE VOLTAGE.
37	3	Test	Lamp test. When pulled high (to V^+) all segments will be turned on and the display should read -1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38	4	OSC_3	See pin 40.
39	6	OSC_2	See pin 40.
40	10	OSC_1	Pins 40, 39, 38 make up the oscillator section. For a 48 kHz clock (3 readings per section) connect pin 40 to the junction of a 100 kΩ resistor and a 100 pF capacitor. The 100 kΩ resistor is tied to pin 39 and the 100 pF capacitor is tied to pin 38.

Analog Section

Figure 3 shows the Block Diagram of the Analog Section for the TSC7116 and TSC7117. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) reference (REF).

Auto-Zero Phase

Input high and low are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. The offset referred to the input is less than 10 μV.

Signal Integrate Phase

The auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between V_{IN}^+ and V_{IN}^- for a fixed time. This differential voltage can be within a wide common-mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, V_{IN}^- can be tied to analog common to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

Reference Integrate Phase

The final phase is reference integrate or de-integrate. Input low is internally connected to analog common and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Reference

The positive reference voltage (V_{REF}^+) is referenced to analog common.

Differential Input

The input can accept differential voltages anywhere within the common-mode range of the input amplifier; or specifically from 1.0 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worse case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of

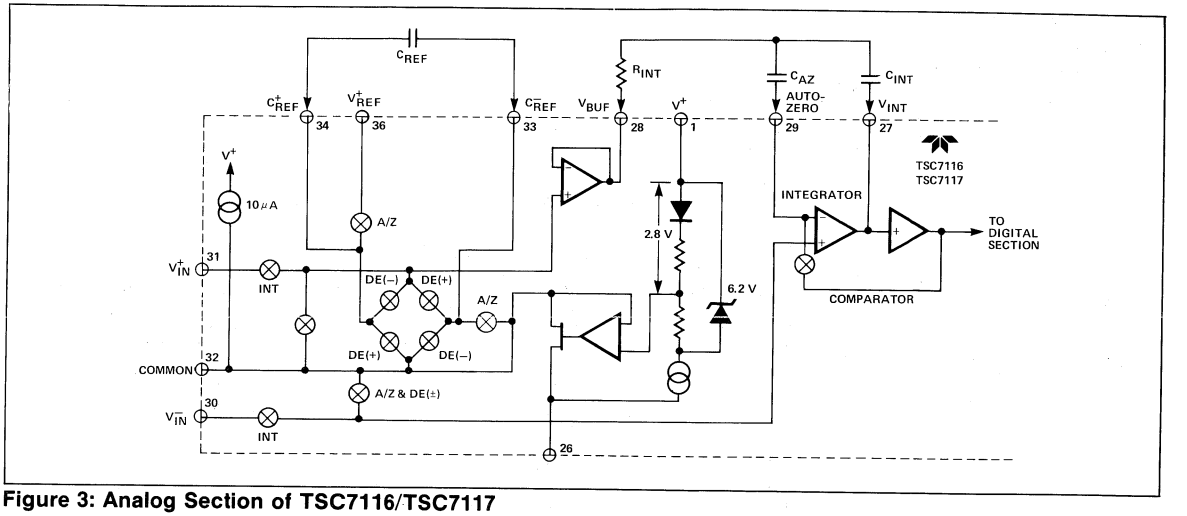


Figure 3: Analog Section of TSC7116/TSC7117

its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2 V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

Analog Common

This pin is included primarily to set the common-mode voltage for battery operation (TSC7116) or for any system where the input signals are floating with respect to the power supply. The common pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6 V. However, the analog common has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7 V), the common voltage will have a low voltage coefficient (0.001%/%), low output impedance (≈15 Ω), and a temperature coefficient of 80 ppm/° C typically.

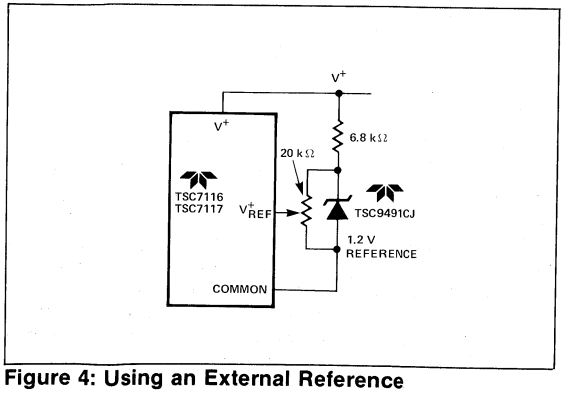


Figure 4: Using an External Reference

An external reference may be added to improve temperature stability or the TSC7116A/TSC7117A devices with lower analog common temperature drift may be used. The circuit is shown in Figure 4.

Analog common is also used as the V_{IN}^- return during auto-zero and deintegrate. If V_{IN}^- is different from analog common, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications V_{IN}^- will be set at a fixed known voltage (power supply common for instance). In this application, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog common, it should be since this removes the common-mode voltage from the reference system.

Within the IC, analog common is tied to an N-channel FET that can sink 30 mA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10 μA of source current, so common may easily be tied to a more negative voltage thus over-riding the internal reference.

Test

The TEST pin serves two functions. On the TSC7117 it is coupled to the internally generated digital supply through a 500 Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1 mA load should be applied.

The second function is a "lamp test." When TEST is pulled high (to V^+) all segments will be turned on and the display should read -1888. The TEST pin will sink about 10 mA under these conditions.

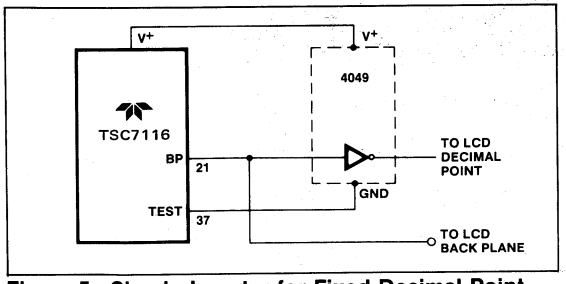


Figure 5: Simple Inverter for Fixed Decimal Point

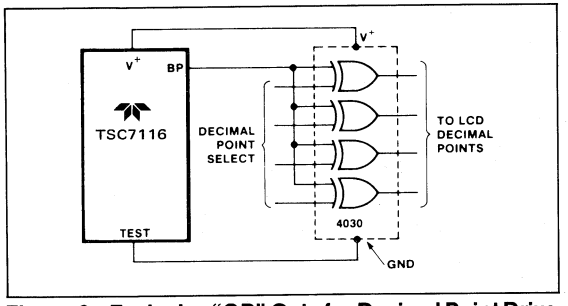


Figure 6: Exclusive "OR" Gate for Decimal Point Drive

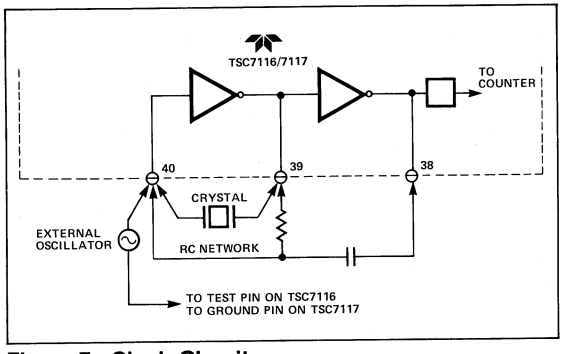


Figure 7: Clock Circuits

Digital Section

Figures 8 and 9 show the digital section for the TSC7116 and TSC7117, respectively. In the TSC7116 (Figure 8), an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases, negligible dc voltage exists across the segments.

Figure 9 is the Digital Section of the TSC7117. It is identical to the TSC7116 except that the regulated supply and back plane drive have been eliminated and the segment drive is typically 8 mA. The 1000 output (pin 19) sinks current from two LED segments, and has a 16 mA drive capability. The TSC7117 is designed to drive common anode LEDs.

In both devices, the polarity indication is "on" for negative analog inputs. If V_{IN}^- and V_{IN}^+ are reversed, this indication can be reversed also, if desired.

System Timing

Figure 9 shows the clocking method used in the TSC7116 and TSC7117. Three clocking methods may be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An RC oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full-scale auto-zero gets the unused portion of reference de-integrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48 kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 48 kHz, 40 kHz, 33-1/3 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66-2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

HOLD Reading Input

When HLDR is at a logic "HI" the latch will not be updated. A/D conversions will continue but will not be updated until the HLDR is returned to "LOW". To continuously update the display connect to TEST (TSC7116) or GROUND (TSC7117) or disconnect. This input is CMOS compatible with 70K typical resistance to TEST (TSC7116) or GROUND (TSC7117).

Component Value Selection

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full-scale where noise is very important, a 0.47 μF capacitor is recommended. On the 2 volt scale, a 0.047 μF capacitor increase the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1 μF capacitor is acceptable in most applications. However, where a large common-mode voltage exists (i.e. the V_{IN}^- pin is not at analog common) and a 200 mV scale is used, a large value is required to prevent to roll-over error. Generally 1.0 μF will hold the roll-over error to 0.5 count in this instance.

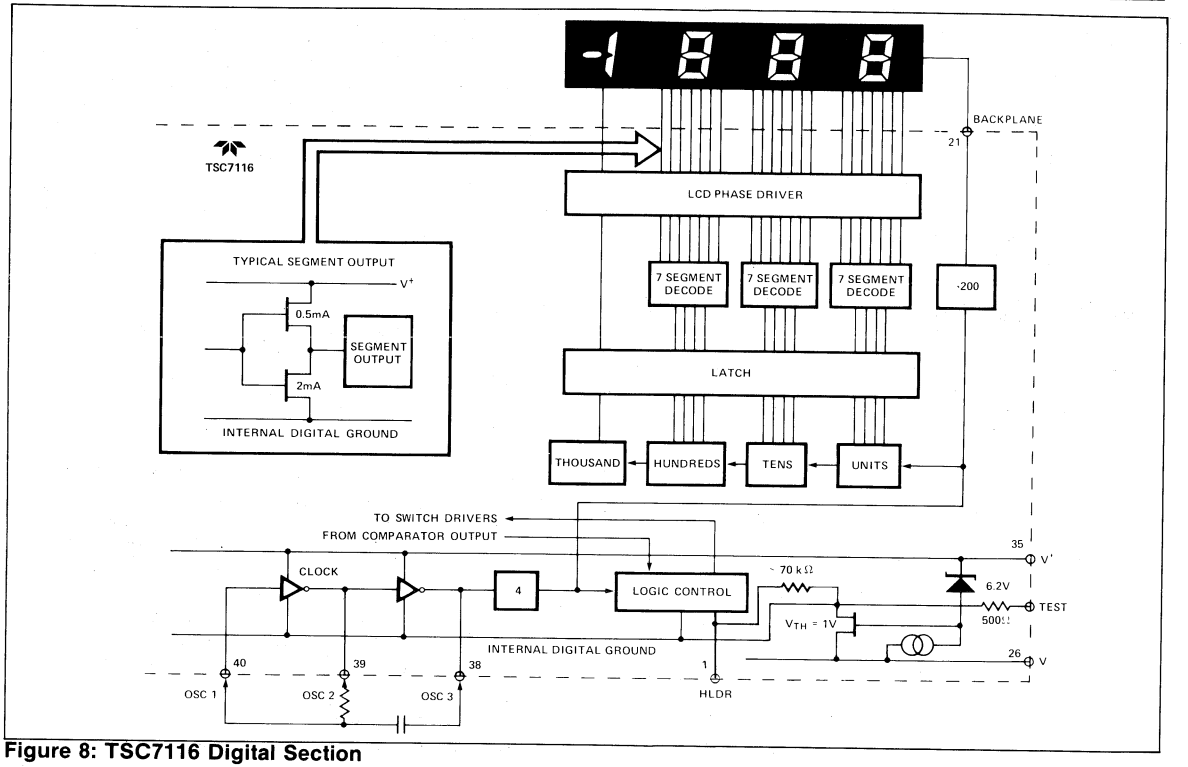


Figure 8: TSC7116 Digital Section

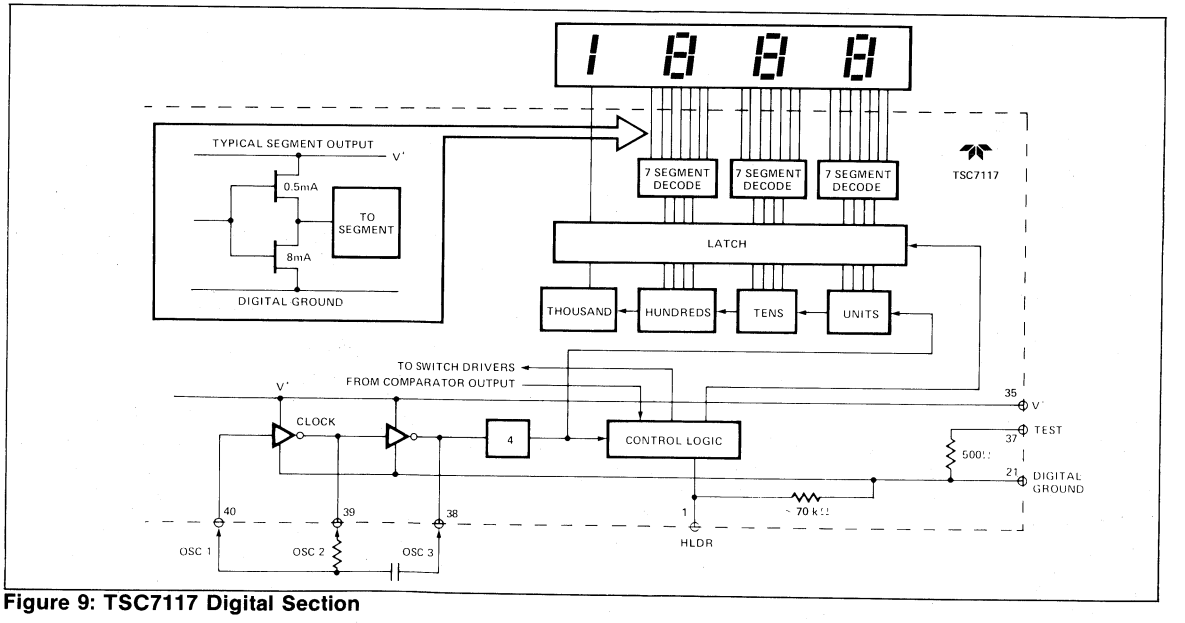


Figure 9: TSC7117 Digital Section

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the TSC7116 or the TSC7117, when the analog common is used as a reference, a nominal ±2 volt full-scale integrator swing is acceptable. For the TSC7117 with ±5 volt supplies and analog common tied to supply ground, a ±3.5 to ±4 volt swing is nominal. For three readings/second (48 kHz clock) nominal values for C_{INT} are 0.22 μ1F and 0.10 μF, respectively. If different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the output swing.

The integrating capacitor must have low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are recommended for this application.

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100 μA of quiescent current. They can supply 20 μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full-scale, 470 kΩ is near optimum and similarly a 47 kΩ for a 200.0 mV scale.

Oscillator Components

For all ranges of frequency a 100 kΩ resistor is recommended and the capacitor is selected from the equation $f = \frac{45}{RC}$. For 48 kHz clock (3 readings/second), C = 100 pF.

Reference Voltage

To generate full-scale output (2000 counts) the analog input required is: $V_{IN} = 2\,V_{REF}$. Thus, for the 200.0 mV and 2.000 volt scale, V_{REF} should equal 100.0 mV and 1.00 volt respectively. In many applications where the A/D is connected to a transducer, there will exist a scale factor between the input voltage and the digital reading. For instance, in a measuring system, the designer might like to have a full-scale reading when the voltage from the transducer is 700 mV. Instead of dividing the input down to 200.0 mV, the designer should use the input voltage directly and select $V_{REF} = 350$ mV. Suitable values for integrating resistor and capacitor would be 120 kΩ and 0.22 μF. This makes the system slightly quieter and also avoids a divider network on the input. The TSC7117 with ±5 V supplies can accept input signals up to ±4 V. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between V_{IN}^{+} and common and the variable (or fixed) offset voltage between common and V_{IN}^{-}.

TSC7117 Power Supplies

The TSC7117 is designed to work from ±5 V supplies. However, if a negative supply is not available, it can be generated from the clock output with two diodes, two capacitors and an inexpensive IC. Figure 10 shows this application.

In selected applications no negative supply is required. The conditions to use a single +5 V supply are:

- The input signal can be referenced to the center of the common-mode range of the converter.
- The signal is less than ±1.5 volts.
- An external reference is used.

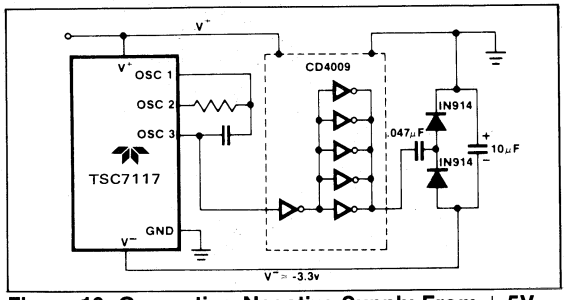


Figure 10: Generating Negative Supply From + 5V

Typical Applications

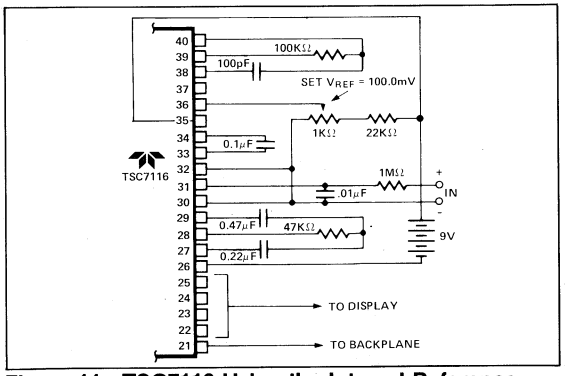


Figure 11: TSC7116 Using the Internal Reference (200 mV Full-Scale, 3 RPS)

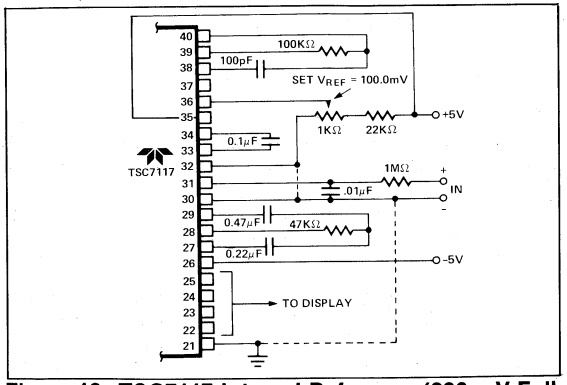


Figure 12: TSC7117 Internal Reference (200 mV Full-Scale, 3 RPS, V_{IN} Tied to GND for Single Ended Inputs).

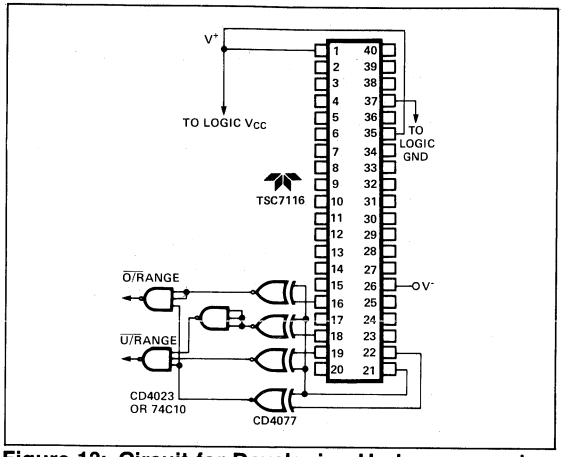


Figure 13: Circuit for Developing Underrange and Overrange Signals from TSC7116 Outputs.

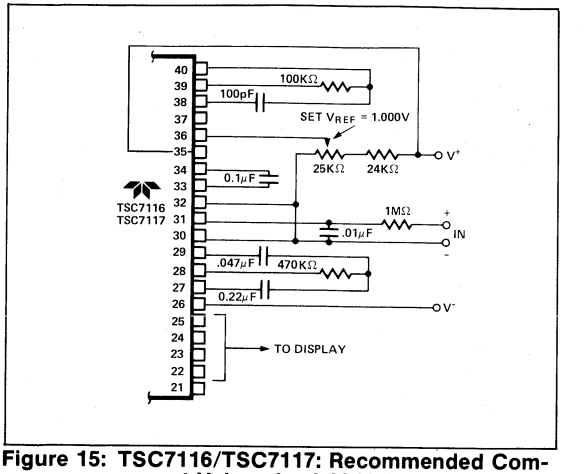


Figure 15: TSC7116/TSC7117: Recommended Component Values for 2.00 V Full-Scale.

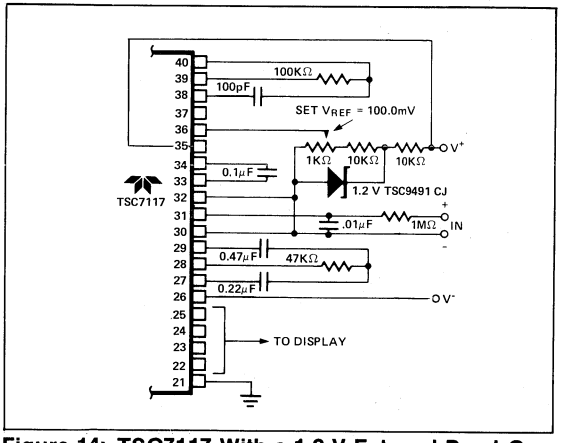


Figure 14: TSC7117 With a 1.2 V External Band-Gap Reference. V_{IN} Tied to Common).

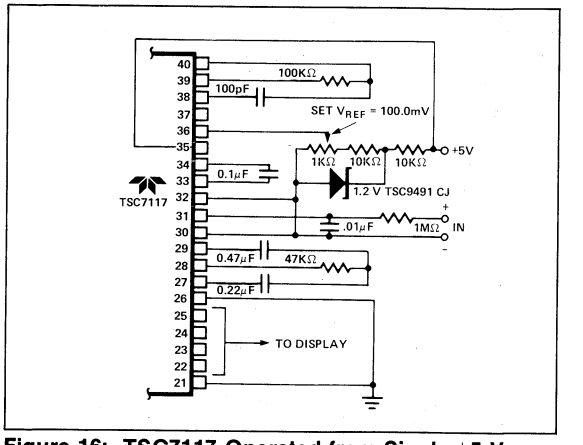


Figure 16: TSC7117 Operated from Single +5 V Supply. An External Reference Must Be Used in This Application.

Applications Information

The TSC7117 sinks the LED display current and this causes heat to build up in the IC package. If the internal voltage reference is used, the changing chip temperature can cause the display to change reading. By reducing package power dissipation such variations can be reduced. By reducing the LED common anode voltage the TSC7117 package power dissipation is reduced.

Figure 17 is a photograph of a curve-tracer display showing the relationship between output current and output voltage for a typical TSC7117CPL. Since a typical LED has 1.8 volts across it at 8 mA, and its common anode is connected to +5 V, the TSC7117 output is at 3.2 V (point A on Fig. 17). Maximum power dissipation is 8.1 mA X 3.2 V X 24 segments = 622 mW.

Notice, however, that once the TSC7117 output voltage is above two volts, the LED current is essentially constant as output voltage increases. Reducing the output voltage by 0.7 V (point B of Figure 17) results in 7.7 mA of LED current, only a 5 percent reduction. Maximum power dissipation is now only 7.7 mA X 2.5 V X 24 = 462 mW, a reduction of 26%. An output voltage reduction of 1 volt (point C) reduces LED current by 10% (7.3 mA) but power dissipation by 38%! (7.3 mA X 2.2 V X 24 = 385 mW).

Reduced power dissipation is very easy to obtain. Fig. 18 shows two ways: either a 5.1 ohm, 1/4 watt resistor or a 1 Amp diode placed in series with the display (but not in series with the TSC7117). The resistor will reduce the TSC7117 output voltage, when all 24 segments are "ON," to point "C" of Fig.

17. When segments turn off, the output voltage will increase. The diode, on the other hand, will result in a relatively steady output voltage, around point "B."

In addition to limiting maximum power dissipation, the resistor reduces the change in power dissipation as the display changes. This effect is caused by the fact that, as fewer segments are "ON," each "ON" output drops more voltage and current. For the best case of six segments (a "111" display) to worst case (a "1888" display) the resistor circuit will change about 230 mW, while a circuit without the resistor will change about 470 mW. Therefore, the resistor will reduce the effect of display dissipation on reference voltage drift by about 50%.

The change in LED brightness caused by the resistor is almost unnoticeable as more segments turn off. If display brightness remaining steady is very important to the designer, diode may be used instead of the resistor.

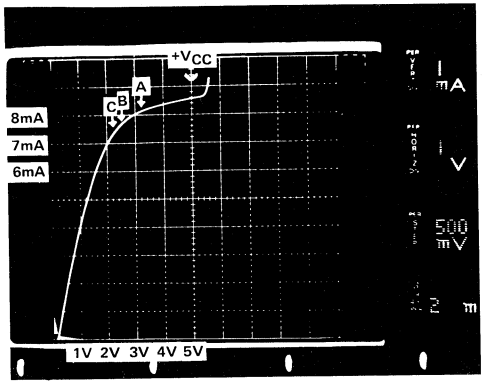


Figure 17: TSC7117 Output Current vs Output Voltage

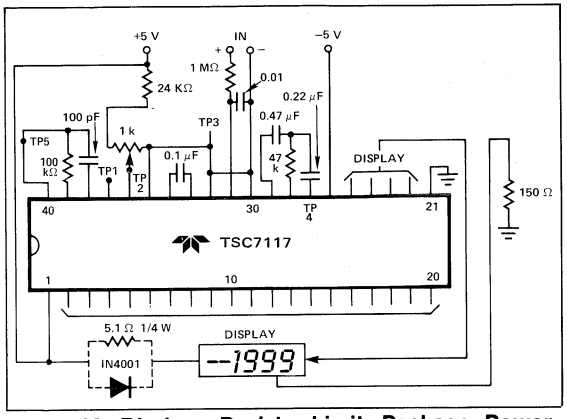
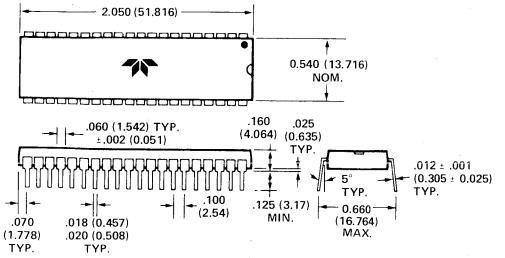


Figure 18: Diode or Resistor Limits Package Power Dissipation

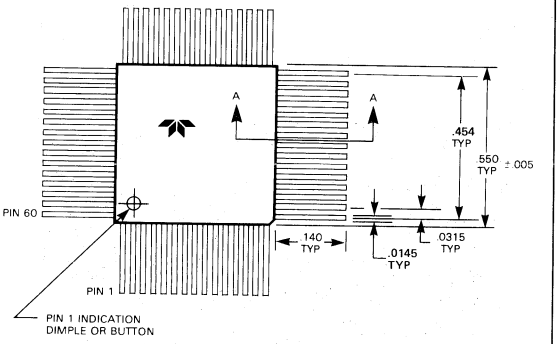
7

Package Information

40-Pin Plastic Dual-In-Line Package
(Package #17)

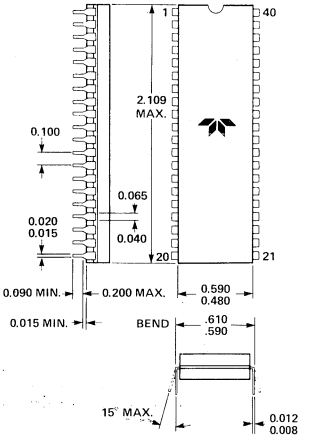


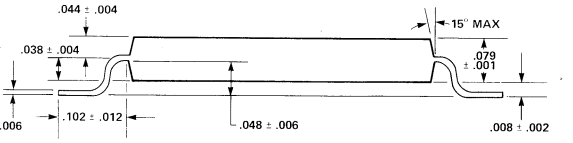
60-Pin Plastic Flat Package



"SQ" Package — Unformed Leads
(Package #22)

40-Pin CerDIP
(Package #20)





"BQ" Package — Formed Leads
(Package #21)

TSC7126A
3 1/2 Digit A/D Converter
• Low Power Dissipation - 900 μW Max.
• 35 ppm/°C Internal Reference

General Description

The TSC7126A is a low power 3 1/2 Digit LCD display analog to digital converter that allows existing 7126 based systems to be upgraded. An improved internal zener reference voltage circuit maintains the analog common temperature drift to 35 ppm/°C typically. A 75 ppm/°C maximum limit is guaranteed. This represents a 2 to 4 times improvement over similar 3 1/2 digit converters.

Existing TSC7126 or ICL7126 based systems may be upgraded without changing external passive component values. The costly, space consuming external reference source may be removed. Power dissipation is a low 900 μW maximum. Long battery life is guaranteed; a key design consideration in portable or battery back-up systems.

The TSC7126A limits linearity error to less than 1 count on 200 mV or 2.00 V full-scale ranges. Rollover error - the difference in readings for equal magnitude but opposite polarity input signals - is below ±1 count. High impedance differential inputs offer 1 pA leakage currents and a 10^{12} Ω input impedance. The differential reference input allows ratiometric measurements for ohms or bridge transducer measurements. The 15 μV_{p-p} noise performance guarantees a "rock solid" reading. The auto zero cycle guarantees a zero display readout for a zero volt input.

The single chip CMOS TSC7126A incorporates all the active devices for a 3 1/2 digit analog to digital converter to directly drive an LCD display. The internal oscillator, precision voltage reference and display segment/backplane drivers simplify system integration, reduce board space requirements and lower total cost. A low cost, high resolution -0.05% - indicating meter requires only a display, four resistors, four capacitors and a 9 V battery. The flat package option eases the mechanical design of low cost, hand held multimeters.

The TSC7126A dual slope conversion technique rejects interference signals if the converters integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400 Hz line frequency signals are present.

Typical Applications

- Thermometry
- Bridge Readouts (Strain Gauges, Load Cells, Null Detectors)
- Digital Meters
  - Voltage/Current/Ohms/Power
  - pH
  - Capacitance/Inductance
  - Fluid Flow Rate/Viscosity/Level
  - Humidity
  - Position
- Digital Scales
- Panel Meters
- LVDT Indicators
- Portable Instrumentation
- Power Supply Readouts
- Process Monitors
- Gaussometers
- Photometers

Features

- Internal Reference With Low Temperature Drift ..... 35 ppm/°C Typical, 75 ppm/°C Maximum
- Guaranteed Zero Reading With Zero Input
- Low Noise ..... 15 μV_{p-p}
- High Resolution (0.05%) and Wide Dynamic Range (72 dB)
- Low Input Leakage Current ..... 1 pA Typical, 10 pA Maximum
- Direct LCD Drive - No External Components.
- Precision Null Detection With True Polarity at Zero
- High Impedance Differential Input
- Convenient 9 V Battery Operation With Low Power Dissipation ..... 500 μW Typical, 900 μW Maximum
- Internal Clock Circuit
- Improved Drop-In Replacement For ICL7126 that offers Low Analog Common Voltage Drift
- Available in Compact Flat Package
- Industrial Temperature Range Device Available

Ordering Information

Part No.	Package	Pin Layout	Temp. Range	Reference Temp. Coefficient
TSC7126ACPL	40-Pin Plastic Dip	Normal	0°C to 70°C	75 ppm/°C Max
TSC7126ARCPL	40-Pin Plastic Dip	Reversed	0°C to 70°C	75 ppm/°C Max
TSC7126AIJL	40-Pin CerDIP	Normal	-25°C to +85°C	100 ppm/°C Max
TSC7126ACBQ	60-Pin Plastic Flat	Formed Leads	0°C to 70°C	75 ppm/°C Max
TSC7126ACSQ	60-Pin Plastic Flat	Unformed Leads	0°C to 70°C	75 ppm/°C Max
Devices with 160 Hour. +125°C Burn-In				
TSC7126ACPL/BI	40-Pin Plastic Dip	Normal	0°C to 70°C	75 ppm/°C Max
TSC7126AIJL/BI	40-Pin CerDIP	Normal	-25°C to +85°C	100 ppm/°C Max

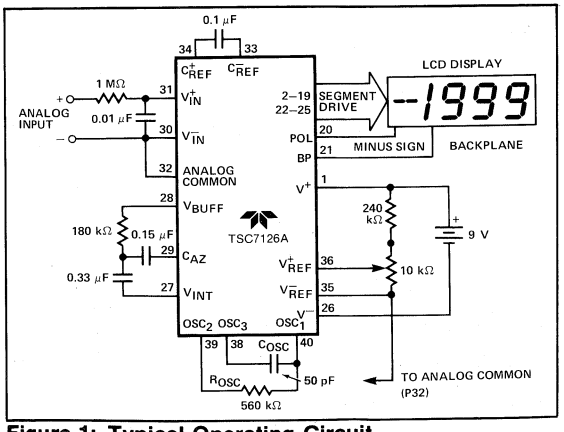


Figure 1: Typical Operating Circuit

Absolute Maximum Ratings

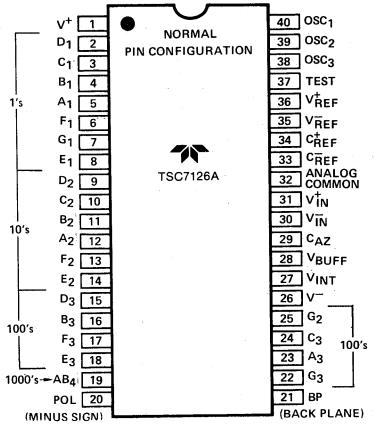
Supply Voltage (V^+ to V^-) ..... 15 V
Analog Input Voltage (either input)[1] ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... Test to V^+
Power Dissipation [2]
CerDIP Package (J) ..... 1000 mW
Plastic Package (P) ..... 800 mW
Epoxy Flat Package (B, S) ..... 500 mW
Operating Temperature
("C" Devices) ..... 0°C to +70°C
("I" Devices) ..... -25°C to +85°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300 °C

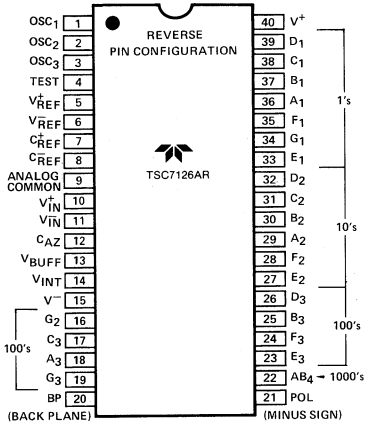
Electrical Characteristics: V_S = 9 V, f_{clock} = 16 kHz and T_A = 25°C unless otherwise noted.

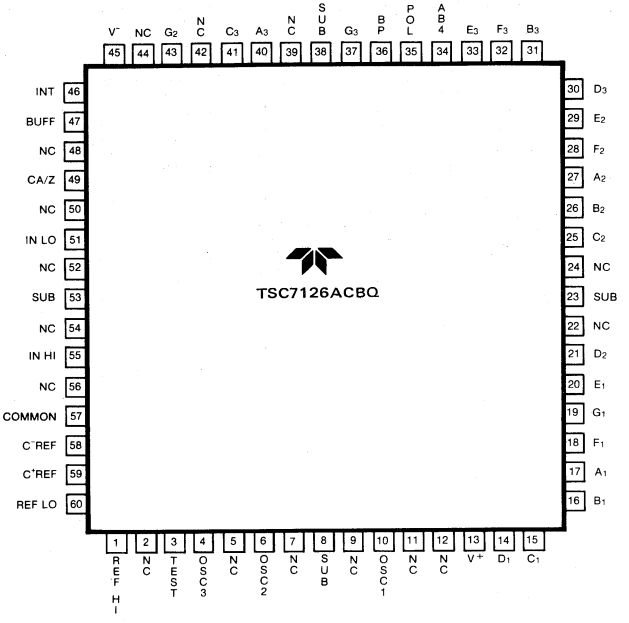
TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC7126A MIN	TYP	MAX	UNIT
INPUT	1	—	Zero Input Reading	V_{IN} = 0.0 V, Full-Scale = 200.0 mV	-000.0	±000.0	+000.0	Digital Reading
	2	—	Zero Reading Drift	V_{IN} = 0.0 V, 0°C ≤ T_A ≤ 70°C	—	0.2	1	μV/°C
	3	—	Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
	4	NL	Linearity Error	Full-Scale = 200 mV or 2.000 V. Max. Deviation from Best Straight Line.	-1	±0.2	+1	Counts
	5	—	Rollover Error	-V_{IN} = +V_{IN} ≈ 200.0 mV	-1	±0.2	+1	Counts
	6	E_N	Noise	V_{IN} = 0 V, Full-Scale = 200.0 mV	—	15	—	μV_{p-p}
	7	I_L	Input Leakage Current	V_{IN} = 0 V	—	1	10	pA
	8	CMRR	Common-Mode Rejection Ratio	V_{CM} = ±1 V, V_{IN} = 0 V Full-Scale = 200.0 mV	—	50	—	μV/V
	9	—	Scale Factor Temperature Coefficient	V_{IN} = 199.0 mV, 0z ≤ T_A ≤ 70°C Ext. Ref. Temp. Coeff. = 0 ppm/°C	—	1	5	ppm/°C
ANALOG COMMON	10	V_{CTC}	Analog Common Temperature Coefficient	250 kΩ Between Commom and V^+ 0°C ≤ T_A ≤ 70°C "C" Commercial Temp. Range Devices	—	35	75	ppm/°C
	11	V_{CTC}	Analog Common Temperature Coefficient	250 kΩ Between Common and V^+ -25°C ≤ T_A ≤ 85°C "I" Industrial Temp. Range Devices	—	35	100	ppm/°C
	12	V_C	Analog Common Voltage	250 kΩ Between Common and V^+	2.7	3.05	3.35	V
LCD DRIVE	13	V_{SD}	LCD Segment Drive Voltage	V^+ to V^- = 9 V	4	5	6	V_{p-p}
	14	V_{BD}	LCD Backplane Drive Voltage	V^+ to V^- = 9 V	4	5	6	V_{p-p}
SUPPLY	15	I_S	Power Supply Current	V_{IN} = 0 V, V^+ to V^- = 9 V, Note 7	—	55	100	μA

Notes:
1. Input voltages may exceed the supply voltages when the input current is limited to 100 μA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Static sensitive device. Unused devices should be stored in conductive material to protect devices from static discharge and static fields.
4. Refer to "Differential Input" discussion.
5. Backplane drive is in phase with segment drive for 'off' segment and 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50 mV.
6. See Figure 1.
7. During auto-zero phase, current is 10-20 μA higher. A 48 kHz oscillator, increases current by 8 μA (typ.). Common current not included.

Pin Configuration







NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V^+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

Pin Description

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
1	(40)	13	V^+	Positive supply voltage.
2	(39)	14	D_1	Activates the D section of the units display.
3	(38)	15	C_1	Activates the C section of the units display.
4	(37)	16	B_1	Activates the B section of the units display.
5	(36)	17	A_1	Activates the A section of the units display.
6	(35)	18	F_1	Activates the F section of the units display.
7	(34)	19	G_1	Activates the G section of the units display.
8	(33)	20	E_1	Activates the E section of the units display.
9	(32)	21	D_2	Activates the D section of the units display.

Pin Description (Cont.)

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
10	(31)	25	C_2	Activates the C section of the tens display.
11	(30)	26	B_2	Activates the B section of the tens display.
12	(29)	27	A_2	Activates the A section of the tens display.
13	(28)	28	F_2	Activates the F section of the tens display.
14	(27)	29	E_2	Activates the E section of the tens display.
15	(26)	30	D_3	Activates the D section of the hundreds display.
16	(25)	31	B_3	Activates the B section of the hundreds display.
17	(24)	32	F_3	Activates the F section of the hundreds display.
18	(23)	33	E_3	Activates the E section of the hundreds display.
19	(22)	34	AB_4	Activates both halves of the 1 in the thousands display.
20	(21)	35	POL	Activates the negative polarity display.
21	(20)	36	BP	Backplane drive output.
22	(19)	37	G_3	Activates the G section of the hundreds display.
23	(18)	40	A_3	Activates the A section of the hundreds display.
24	(17)	41	C_3	Activates the C section of the hundreds display.
25	(16)	43	G_2	Activates the G section of the tens display.
26	(15)	45	V^-	Negative power supply voltage.
27	(14)	46	V_{INT}	The integrating capacitor should be selected to give the maximum voltage swing that ensures component tolerance build up will not allow the integrator output to saturate. When analog common is used as a reference and the conversion rate is 3 readings per second, a 0.047 μF capacitor may be used. The capacitor must have a low dielectric constant to prevent roll-over errors. See INTEGRATING CAPACITOR section for additional details.
28	(13)	47	V_{BUFF}	Integration resistor connection. Use a 180 kΩ for a 200 mV full-scale range and a 180 MΩ for 2 V full scale range.
29	(12)	49	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.33 μF capacitor for a 200 mV full-scale, and a 0.033 μF capacitor for a 2 volt full-scale. See paragraph on AUTO-ZERO CAPACITOR for more details.
30	(11)	51	V_{IN}^-	The low input is connected to this pin.
31	(10)	55	V_{IN}^+	The high input signal is connected to this pin.
32	(9)	57	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on ANALOG COMMON for more details. It also acts as a reference voltage source.
33	(8)	58	C_{REF}^-	See pin 34.
34	(7)	59	C_{REF}^+	A 0.1 μF capacitor is used in most applications. If a large common mode voltage exists (for example the V_{IN} pin is not at analog common), and a 200 mV scale is used, a 1.0 μF is recommended and will hold the rollover error to 0.5 count.
35	(6)	60	V_{REF}^-	See pin 36.
36	(5)	1	V_{REF}^+	The analog input required to generate a full-scale output (1,999 counts). Place 100 mV between pins 35 and 36 for 199.9 mV full-scale. Place 1.00 volts between pins 35 and 36 for 2 volts full-scale. See paragraph on REFERENCE VOLTAGE.
37	(4)	3	Test	Lamp test. When pulled high (to V^+) all segments will be turned on and the display should read -1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38	(3)	4	OSC_3	See pin 40.
39	(2)	6	OSC_2	See pin 40.
40	(1)	10	OSC_1	Pins 40, 39, 38 make up the oscillator section. For a 48 kHz clock (3 readings per section) connect pin 40 to the junction of a 180 kΩ resistor and a 50 pF capacitor. The 180 kΩ resistor is tied to pin 39 and the 50 pF capacitor is tied to pin 38.

General Theory of Operation

Dual Slope Conversion Principles

The TSC7126A is a dual slope, integrating analog-to-digital converter. An understanding of the dual slope conversion technique will aid in following the detailed TSC7126A operation theory.

The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period (T_{SI}). Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal (T_{RI}).

In a simple dual slope converter a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

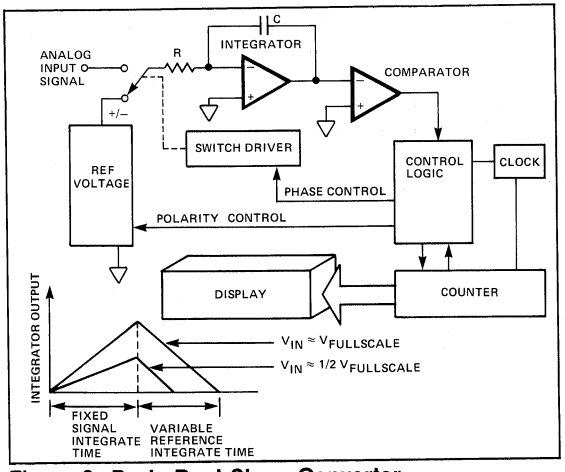


Figure 2: Basic Dual Slope Converter

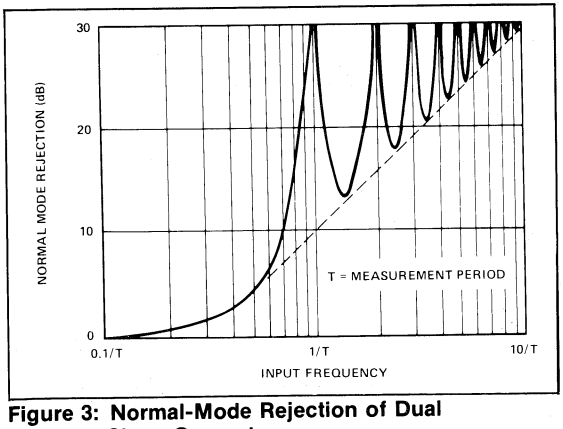


Figure 3: Normal-Mode Rejection of Dual Slope Converter

A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{RC}\int_0^{T_{SI}} V_{IN}(t)dt = \frac{V_R T_{RI}}{RC}$$

where:

V_R = Reference Voltage
T_{SI} = Signal Integration Time (Fixed)
T_{RI} = Reference Voltage Integration Time (Variable)

For a constant V_{IN}:

$$V_{IN} = V_R \frac{T_{RI}}{T_{SI}}$$

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments. Interfering signals with frequency components at multiples of the averaging period will be attenuated. Integrating ADCs commonly operate with the signal integration period set to a multiple of the 50/60 Hz power line period.

Analog Section

In addition to the basic signal integrate and deintegrate cycles discussed above the TSC7126A design incorporates an auto-zero cycle. This cycle removes buffer amplifier, integrator, and comparator offset voltage error terms from the conversion. A true digital zero reading results without external adjusting potentiometers. A complete conversion consists of three cycles: an auto-zero, signal integrate and reference integrate cycle.

Auto-Zero Cycle

During the auto-zero cycle the differential input signal is disconnected from the circuit by opening internal analog gates. The internal nodes are shorted to analog common (ground) to establish a zero input condition. Additional analog gates close a feedback loop around the integrator and comparator. This loop permits comparator offset voltage error compensation. The voltage level established on C_{AZ} compensates for device offset voltages. The auto-zero cycle residual is typically 10 -15 μV.

The auto-zero cycle length is 1000 to 3000 clock periods.

Signal Integration Cycle

The auto-zero loop is opened and the internal differential inputs connect to V_{IN}^+ and V_{IN}^-. The differential input signal is integrated for a fixed time period. The TSC7126A signal integration period is 1000 clock periods or counts. The externally set clock frequency is divided by four before clocking the internal counters. The intergration time period is:

$$T_{SI} = \frac{4}{f_{OSC}} \times 1000$$

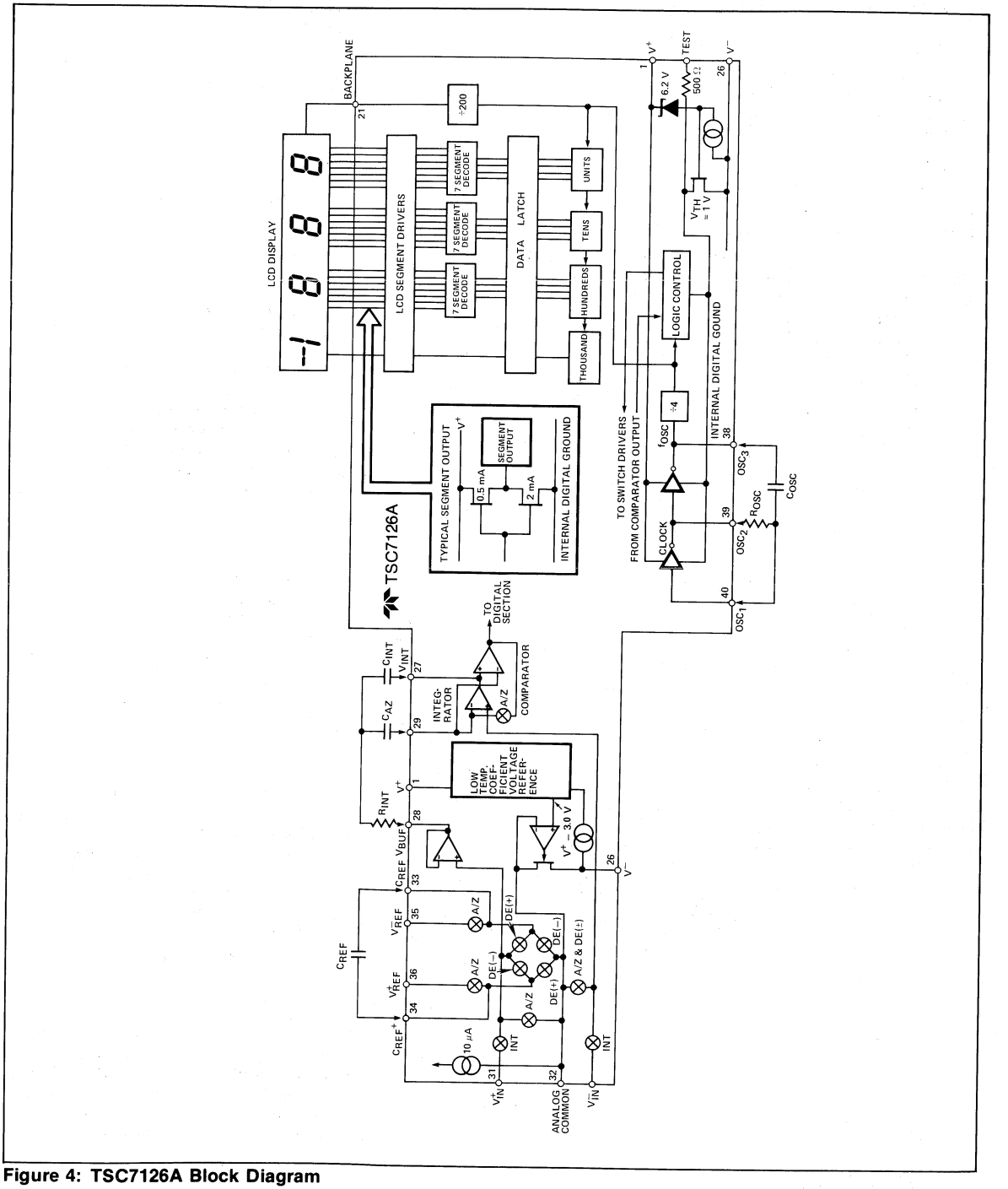


Figure 4: TSC7126A Block Diagram

where:

f_{OSC} = External Clock Frequency

The differential input voltage must be within the device common-mode range when the converter and measured system share the same power supply common (ground). If the converter and measured system do not share the same power supply common, V_{IN}^- should be tied to analog common.

Polarity is determined at the end of signal integrate signal phase. The sign bit is a true polarity indication in that signals less than 1 LSB are correctly determined. This allows precision null detection limited only by device noise and auto-zero residual offsets.

Reference Integrate Cycle:

The final phase is reference integrate or deintegrate. V_{IN}^- is internally connected to analog common and V_{IN}^+ is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal and is between 0 and 2000 internal clock periods. The digital reading displayed is

$$1000 \frac{V_{IN}}{V_{REF}}$$

Digital Section

The TSC7126A contains all the segment drivers necessary to directly drive a 3-1/2 digit liquid crystal display (LCD). An LCD backplane driver is included. The backplane frequency is the external clock frequency divided by 800. For three conversions/second the backplane frequency is 60 Hz with a 5 V nominal amplitude. When a segment driver is in phase with the backplane signal the segment is "OFF." An out of phase segment drive signal causes the segment to be "ON" or visible. This AC drive configuration results in negligible DC voltage across each LCD segment. This insures long LCD display life. The polarity segment driver is "ON" for negative analog inputs. If V_{IN}^+ and V_{IN}^- are reversed this indicator would reverse.

On the TSC7126A when the test pin is pulled to V^+ all segments are turned "ON." The display reads -1888. During this mode the LCD segments have a constant DC voltage impressed. Do not leave the display in this mode for more than several minutes. LCD displays may be destroyed if operated with DC levels for extended periods.

The display FONT and segment drive assignment are shown in Figure 5.

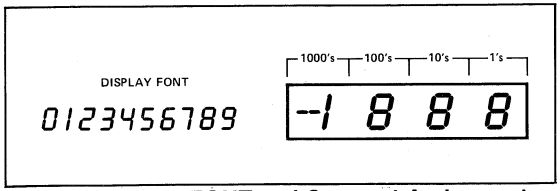


Figure 5: Display FONT and Segment Assignment.

System Timing

The oscillator frequency is divided by 4 prior to clocking the internal decade counters. The three phase measurement cycle takes a total of 4000 counts or 16000 clock pulses. The 4000 count cycle is independent of input signal magnitude.

Each phase of the measurement cycle has the following length:

- Auto-Zero Phase: 1000 to 3000 Counts
  (4000 to 12000 Clock Pulses)
  For signals less than full-scale the auto-zero phase is assigned the unused reference integrate time period.
- Signal Integrate: 1000 Counts
  (4000 Clock Pulses)
  This time period is fixed. The integration period is:

$$T_{SI} = 4000 \left[\frac{1}{f_{OSC}}\right]$$

  Where f_{OSC} is the externally set clock frequency.
- Reference Integrate: 0 to 2000 Counts
  (0 to 8000 Clock Pulses)

The TSC7126A is a drop in replacement for the TSC7126 and ICL7126 that offers a greatly improved internal reference temperature coefficient. No external component value changes are required to upgrade existing designs.

Component Value Selection

Auto-Zero Capacitor - C_{AZ}

The C_{AZ} capacitor size has some influence on system noise. A 0.33 μF capacitor is recommended for 200 mV full-scale applications where 1 LSB is 100 μV. A 0.033 μF capacitor is adequate for 2.0 V full-scale applications. A mylar type dielectric capacitor is adequate.

Reference Voltage Capacitor - C_{REF}

The reference voltage used to ramp the integrator output voltage back to zero during the reference integrate cycle is stored on C_{REF}. A 0.1 μF capacitor is acceptable when V_{IN}^- is tied to analog common. If a large common-mode voltage exists (V_{REF}^- ≠ analog common) and the application requires a 200 mV full-scale increase C_{REF} to 1.0 μF. Rollover error will be held to less than 0.5 count. A mylar type dielectric capacitor is adequate.

Integrating Capacitor - C_{INT}

C_{INT} should be selected to maximize integrator output voltage swing without causing output saturation. Due to the TSC7126A superior analog common temperature coefficient specification, analog common will normally supply the differential voltage reference. For this case a ±2 V full-scale integrator output swing is satisfactory. For 3 readings/second (f_{OSC} = 48 kHz) a 0.047 value is suggested. For one reading per second 0.15 μF is recommended.If a different oscillator frequency is used C_{INT} must be changed in inverse proportion to maintain the nominal ±2 V integrator swing.

An exact expression for C_{INT} is:

$$C_{INT} = \frac{(4000)\left(\frac{1}{f_{OSC}}\right)\left(\frac{V_{FS}}{R_{INT}}\right)}{V_{INT}}$$

Where:

f_{OSC} = Clock frequency at Pin 38
V_{FS} = Full-scale input voltage
R_{INT} = Integrating resistor
V_{INT} = Desired full-scale integrator output swing

At three readings per seccond, a 750 Ω resistor should be placed in series with C_{INT}. This increases accuracy by compensating for comparator delay. C_{INT} must have low dielectric absorption to minimize roll-over error. An inexpensive polypropylene capacitor is recommended.

Integrating Resistor - R_{INT}

The input buffer amplifier and integrator are designed with class A output stages. The output stage idling current is 6 μA. The integrator and buffer can supply 1 μA drive currents with negligible linearity errors. R_{INT} is chosen to remain in the output stage linear drive region but not so large that printed circuit board leakage currents induce errors. For a 200 mV full-scale R_{INT} is 180 kΩ. A 2.0 V full-scale requires 1.8 mΩ.

Component	Nominal Full-Scale Voltage	
Value	200.0 mV	2.000 V
C_{AZ}	0.33 μF	0.033 μF
R_{INT}	180 kΩ	1.8 MΩ
C_{INT}	0.047 μF	0.047 μF

Note:
1. f_{OSC} = 48 kHz (3 readings/sec)

Oscillator Components

C_{OSC} should be 50 pF. R_{OSC} is selected from the equation:

$$f_{OSC} = \frac{0.45}{RC}$$

Note that f_{OSC} is divided by four to generate the TSC7126A internal control clock. The backplane drive signal is derived by dividing f_{OSC} by 800.

To achieve maximum rejection of 60 Hz noise pickup, the signal integrate period should be a multiple of 60 Hz. Oscillator frequencies of 240 kHz, 120 kHz, 80 kHz, 60 kHz, 40 kHz, 33 1/3 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 200 kHz, 100 kHz, 66 2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

Reference Voltage Selection

A full-scale reading (2000 counts) requires the input signal be twice the reference voltage.

Required Full-Scale Voltage *	V_{REF}
200.0 mV	100.0 mV
2.000 V	1.000 V

* $V_{FS} = 2\ V_{REF}$

In some applications a scale factor other than unity may exist between a transducer output voltage and the required digital reading. Assume, for example, a pressure transducer output is 400 mV for 2000 lb/in^2. Rather than dividing the input voltage by two the reference voltage should be set to 200 mV. This permits the transducer input to be used directly.

The differential reference can also be used when a digital zero reading is required when V_{IN} is not equal to zero. This is common in temperature measuring instrumentation. A compensating offset voltage can be applied between analog common and V_{IN}^-. The transducer output is connected between V_{IN}^+ and analog common.

Device Pin Functional Description

Differential Signal Inputs (V_{IN}^+ (Pin 31), V_{IN}^- (Pin 30))

The TSC7126A is designed with true differential inputs and accepts input signals within the input stage common-mode

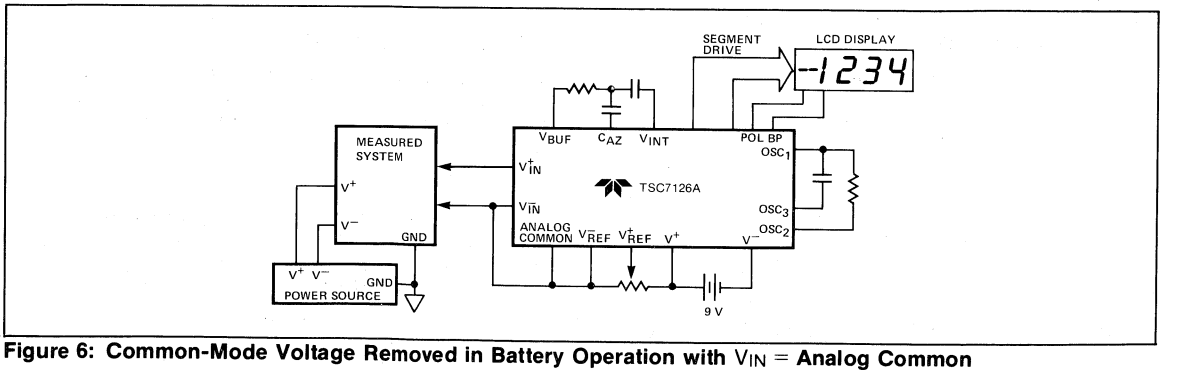


Figure 6: Common-Mode Voltage Removed in Battery Operation with V_{IN} = Analog Common

voltage range (V_{CM}). The typical range is $V^+ - 1.0$ to $V^- + 1$ V. Common-mode voltages are removed from the system when the TSC7126A operates from a battery or floating power source (Isolated from measured system) and V_{IN}^- is connected to analog common (V_{COM}): See Figure 6.

In systems where common-mode voltages exist the TSC7126A 86 dB common-mode rejection ratio minimizes error. Common-mode voltages do, however, affect the integrator output level. Integrator output saturation must be prevented. A worse case condition exists if a large positive V_{CM} exists in conjunction with a full-scale negative differential signal. The negative signal drives the integrator output positive along with V_{CM} (Figure 7). For such applications the integrator output swing can be reduced below the recommended 2.0 V full-scale swing. The integrator output will swing within 0.3 V of V^+ or V^- without increased linearity error.

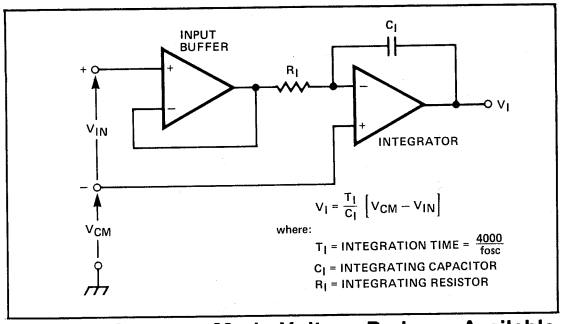


Figure 7: Common-Mode Voltage Reduces Available Integrator Swing. ($V_{COM} \neq V_{IN}$)

Differential Reference
(V_{REF}^+ (Pin 36), V_{REF}^-(Pin 39))

The reference voltage can be generated anywhere within the V^+ to V^- power supply range.

To prevent rollover type errors being induced by large common-mode voltages C_{REF} should be large compared to stray node capacitance.

The TSC7126A offers a significantly improved analog common temperature coefficient. This potential provides a very stable voltage suitable for use as a voltage reference. The temperature coefficient of analog common is 20 ppm/° C typically.

Analog Common (Pin 32)

The analog common pin is set at a voltage potential approximately 3.0 V below V^+. The potential is guaranteed to be between 2.7 V and 3.35 V below V^+. Analog common is tied internally to an N channel FET capable of sinking 30 mA. This FET will hold the common line at 3.0 V should an external load attempt to pull the common line toward V^+. Analog common source current is limited to 10 μA. Analog common is therefore easily pulled to a more negative voltage (i.e., below V^+ -3.0 V).

The TSC7126A connects the internal V_{IN}^+ and V_{IN}^+ inputs to analog common during the auto-zero cycle. During the reference integrate phase V_{IN}^- is connected to analog common. If V_{IN}^- is not externally connected to analog common, a common-mode voltage exists. This is rejected by the converters 86 dB common-mode rejection ratio. In battery operation analog common and V_{IN}^- are usually connected removing common-mode voltage concerns. In systems where V_{IN}^- is connected to the power supply ground or to a given voltage, analog common should be connected to V_{IN}^-.

The analog common pin serves to set the analog section reference or common point. The TSC7126A is specifically designed to operate from a battery or in any measurement system where input signals are not referenced (float) with respect to the TSC7126A power source. The analog common potential of V^+ -3.0 V gives a 7 V end of battery life voltage. The common potential has a 0.001%/% voltage coefficient and a 15 Ω output impedance.

With sufficiently high total supply voltage (V^+-V^- >7.0 V) analog common is a very stable potential with excellent temperature stability - typically 35 ppm/° C. This potential can be used to generate the TSC7126A reference voltage. An external voltage reference will be unnecessary in most cases because of the 35 ppm/° C temperature coefficient. See TSC7126A Internal Voltage Reference discussion.

Test (Pin 37)

The test pin potential is 5 V less than V^+. Test may be used as the negative power supply connection for external CMOS logic. The test pin is tied to the internally generated negative logic supply through a 500 Ω resistor. The test pin load should be no more than 1 mA. See the applications section for additional information on using test as a negative digital logic supply.

If test is pulled high to V^+ all segments plus the minus sign will be activated. Do not operate in this mode for more than several minutes. With Test = V^+ the LCD Segments are impressed with a DC voltage which will destroy the LCD.

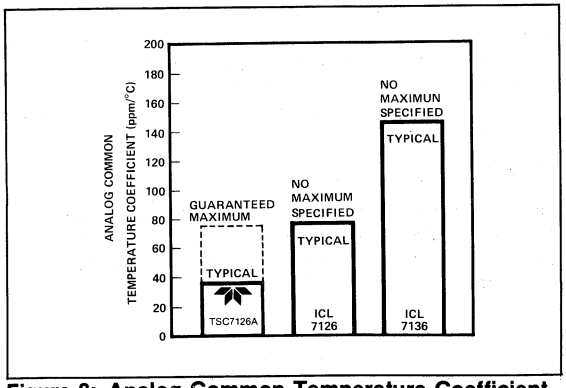


Figure 8: Analog Common Temperature Coefficient

TSC7126A Internal Voltage Reference

The TSC7126A analog common voltage temperature stability has been significantly improved (Figure 8). The "A" version of the industry standard 7126 device will allow users to upgrade old systems and design new systems without external voltage references. External R and C values do not need to be changed. Figure 9 shows analog common supplying the necessary voltage reference for the TSC7126A.

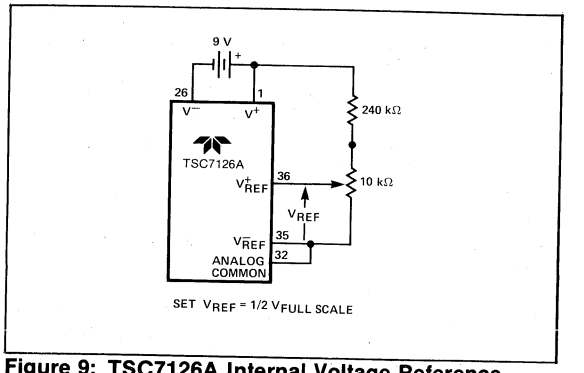


Figure 9: TSC7126A Internal Voltage Reference Connection

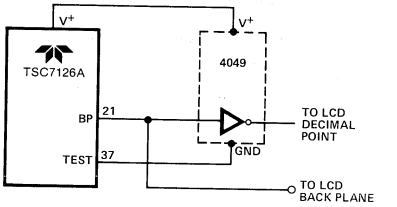
Applications Information

Liquid Crystal Display Sources

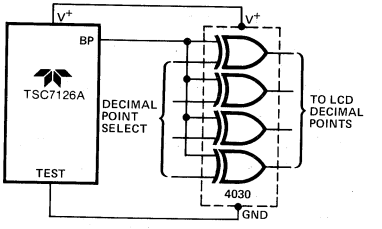
Several LCD manufacturers supply standard LCD displays to interface with the TSC7126A 3 1/2 digit analog-to-digital converter.

Manufacturer	Address/Phone	Representative Part Numbers[1]
Crystaloid Electronics	5282 Hudson Dr., Hudson, OH 44236 216/655-2429	C5335, H5535, T5135, SX440
AND	770 Airport Blvd., Burlingame, CA 94010 415/347-9916	FE 0801 FE 0203
EPSON	3415 Kashikawa St., Torrance, CA 90505 213/534-0360	LD-B709BZ LD-H7992AZ
Hamlin, Inc.	612 E. Lake St., Lake Mills, WI 53551 414/648-2361	3902, 3933, 3903

Note:
1. Contact LCD manufacturer for full product listing/specifications.



Simple Inverter for Fixed Decimal Point or Display Annunciator



Multiple Decimal Point or Annunciator Driver

Decimal Point and Annunciator Drive

The test pin is connected to the internally-generated digital logic supply ground through a 500 Ω resistor. The test pin may be used as the negative supply for external CMOS gate segment drivers. LCD display annunciators for decimal points, low battery indication, or function indication may be added without adding an additional supply. No more than 1 mA should be supplied by the test pin. The test pin potential is approximately 5 V below V^+.

Flat Package

The TSC7126A is available in an epoxy 60-pin flat package. The "BQ" device leads are bent while the "SQ" device leads are unformed (straight). A test socket for the TSC7126ACSQ device is available:

Part No.: IC 51-42
Manufacturer: Yamaichi
Distribution: Nepenthe Distribution
2471 East Bayshore
Suite 520
Palo Alto, CA 94043
(415) 856-9332

Ratiometric Resistance Measurements

The TSC7126A true differential input and differential reference make ratiometric readings possible. In ratiometric operation, an unknown resistance is measured with respect to a known standard resistance. No accurately defined reference voltage is needed.

The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input and the voltage across the known resistor applied to the reference input. If the unknown equals the standard, the display will read 1000. The displayed reading can be determined from the following expression:

$$\text{Displayed Reading} = \frac{\text{R Unknown}}{\text{R Standard}} \times 1000$$

The display will overrange for R Unknown ≥2 x R Standard.

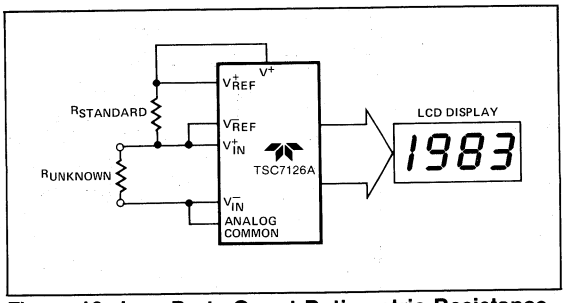
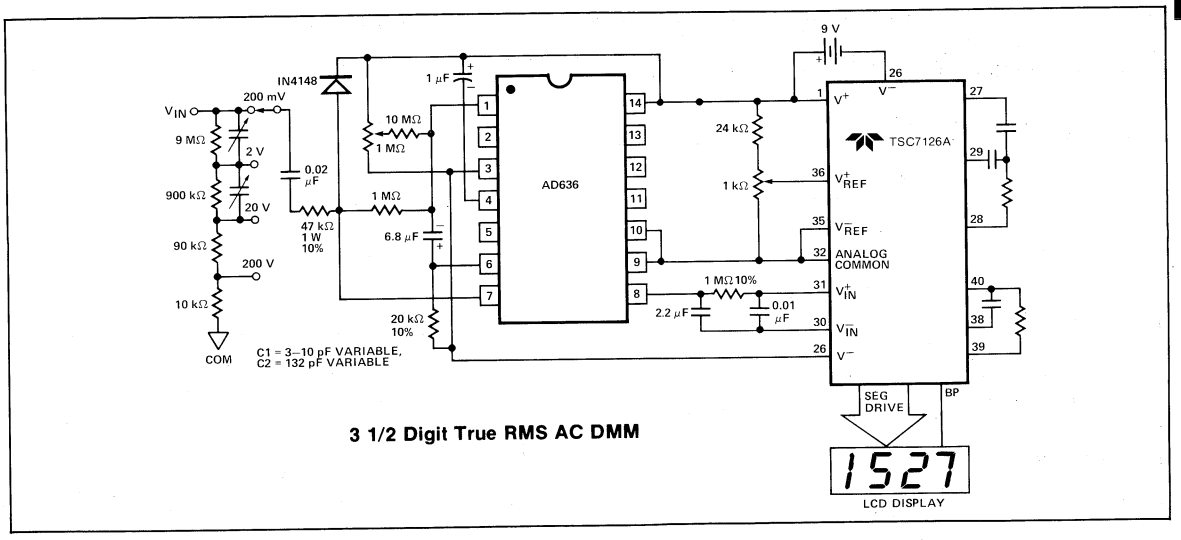


Figure 10: Low Parts Count Ratiometric Resistance Measurement

7



3 1/2 Digit True RMS AC DMM

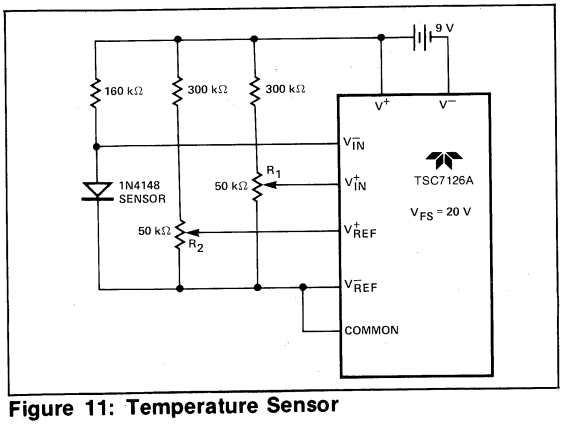


Figure 11: Temperature Sensor

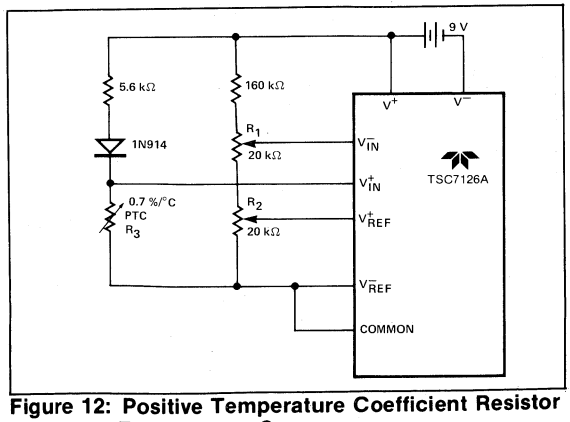


Figure 12: Positive Temperature Coefficient Resistor Temperature Sensor

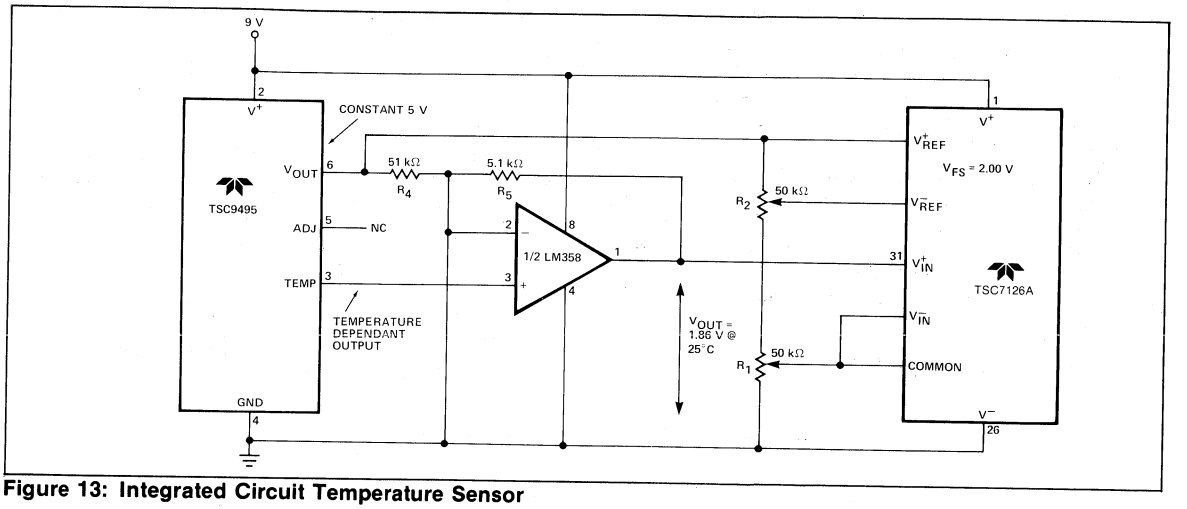
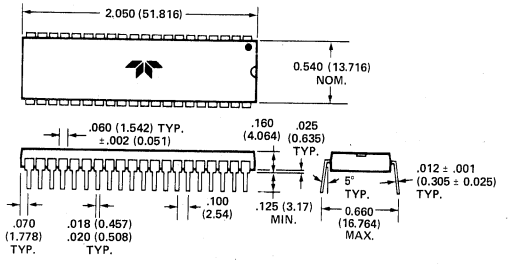


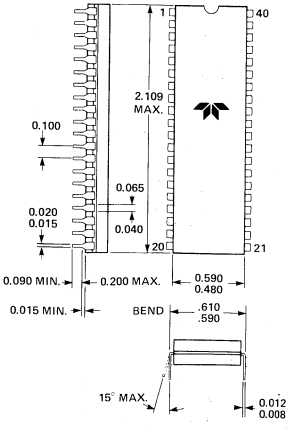
Figure 13: Integrated Circuit Temperature Sensor

Package Information

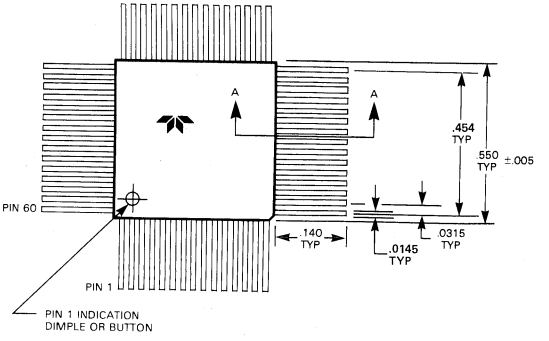
(Package #17)
40-Pin Plastic Dip (PL Package)



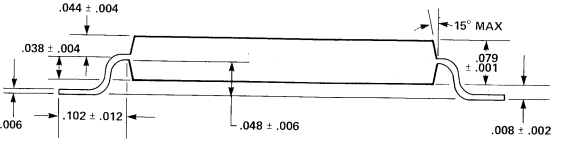
(Package #20)
40-Pin Cerdip



60-Pin Flat Package



"SQ" Package - Unformed Leads
(Package #22)



"BQ" Package - Formed Leads
(Package #21)

TSC7126
3 1/2 Digit A/D Converter
• Low Power Dissipation - 900 μW Max.

General Description

The single chip CMOS TSC7126 incorporates all the active devices for a 3 1/2 digit analog-to-digital converter to directly drive an LCD display. The internal oscillator, voltage reference and display segment/backplane drivers simplify system integration, reduce board space requirements and lower total cost. A low cost, high resolution -0.05% - indicating meter requires only a display, four resistors, four capacitors and a 9 V battery. The flat package option eases the mechanical design of low cost, hand held multimeters and systems.

The TSC7126 dual slope conversion technique rejects interference signals when the integration time is set to a multiple of the interference signal period. This is especially useful in industrial measurement environments where 50, 60 and 400 Hz line frequency signals are present.

With an auto-zero error less than 10 μV, zero drift less than 1 μV/° C, input bias current of 10 pA max and rollover error of less than one count, the TSC7126 brings exceptional value to the portable battery powered field.

In addition, the differential input and reference allows the measurement on load cells, strain gauges and other bridge type transducers. The low power TSC7126 can be used as a plug-in replacement for the TSC7106 by changing only the values of seven passive components.

For applications needing a low drift internal voltage reference refer to the TSC7126A data sheet.

Features

- Long Battery Life ..... 8000 Hours Typical
- Auto-Zero Cycle
- Guaranteed Zero Reading With Zero Input
- Low Noise ..... 15 μV_{p-p}
- High Resolution (0.05%) and Wide Dynamic Range (72 dB)
- Low Input Leakage Current ..... 1 pA Typical
  10 pA Maximum
- Direct LCD Display Drive - No External Components.
- Precision Null Detection With True Polarity at Zero
- High Impedance Differential Input
- Convenient 9 V Battery Operation With Low Power Dissipation ..... 500 μW Typical
  900 μW Maximum
- Internal Clock Circuit
- Drop-In Replacement for ICL7126
- Available in Compact Flat Package
- Industrial Temperature Range Device

Typical Applications

- Thermometry
- Bridge Readouts (Strain Gauges, Load Cells, Null Detectors)
- Digital Meters
  - — Voltage/Current/Ohms/Power
  - — pH
  - — Capacitance/Inductance
  - — Fluid Flow Rate/Viscosity/Level
- Digital Scales
- LVDT Indicators
- Portable Instrumentation
- Power Supply Readouts
- Process Monitors
- Photometers

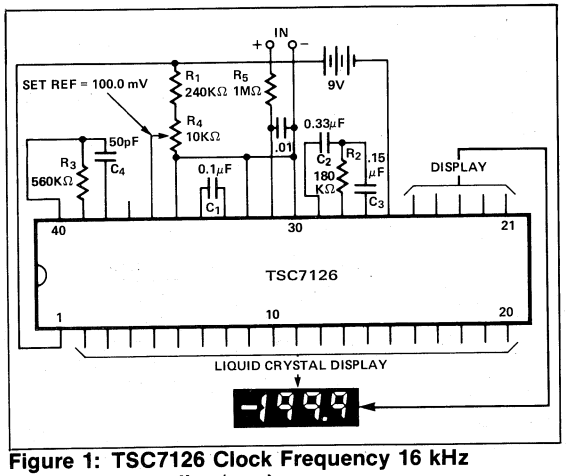


Figure 1: TSC7126 Clock Frequency 16 kHz (1 reading/sec.)

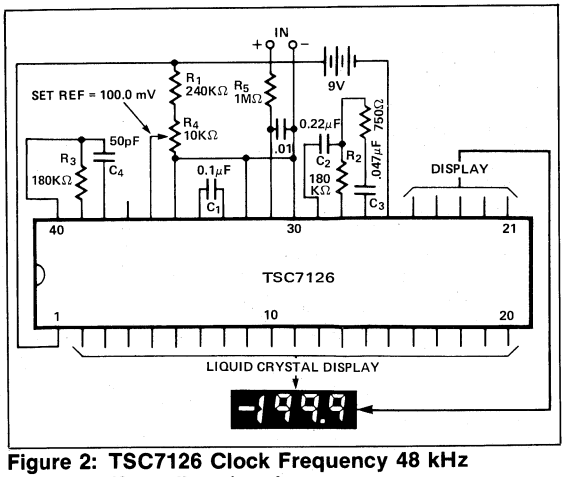


Figure 2: TSC7126 Clock Frequency 48 kHz (3 readings/sec.)

Absolute Maximum Ratings*

Supply voltage (V^+ to V^-) ..... 15 V
Analog Input Voltage (either input) [1] ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... Test to V^+
Power Dissipation [2]
Ceramic Package ..... 1000 mW
Plastic Package ..... 800 mW
Operating Temperature
(C Device) ..... 0°C to +70°C
(I Device) ..... -25°C to +85°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Electrical Characteristics [3]

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0 mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100 mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN} = +V_{IN} \approx$ 200.0 mV	-1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200 mV or Full Scale = 2.000 V	-1	±0.2	+1	Counts
Common Mode Rejection Ratio[4]	V_{CM} = ±1V, V_{IN} = 0V. Full Scale = 200.0 mV	—	50	—	μV/V
Noise (Pk - Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0 mV	—	15	—	μV
Leakage Current @ Input	V_{IN} = 0V	—	1	10	pA
Zero Reading Drift	V_{IN} = 0 0° < T_A < 70°C	—	0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0 mV 0 < T_A < 70°C (Ext. Ref. 0 ppm/°C)	—	1	5	ppm/°C
Supply Current (Does not include Common current)	V_{IN} = 0 (Note 6)	—	50	100	μA
Analog Common Voltage (with respect to positive supply)	250KΩ between Common and positive supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to positive supply)	250KΩ between Common and positive supply	—	80	—	ppm/°C
Pk-Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Power Dissipation Capacitance	vs. Clock Frequency	—	40	—	pF

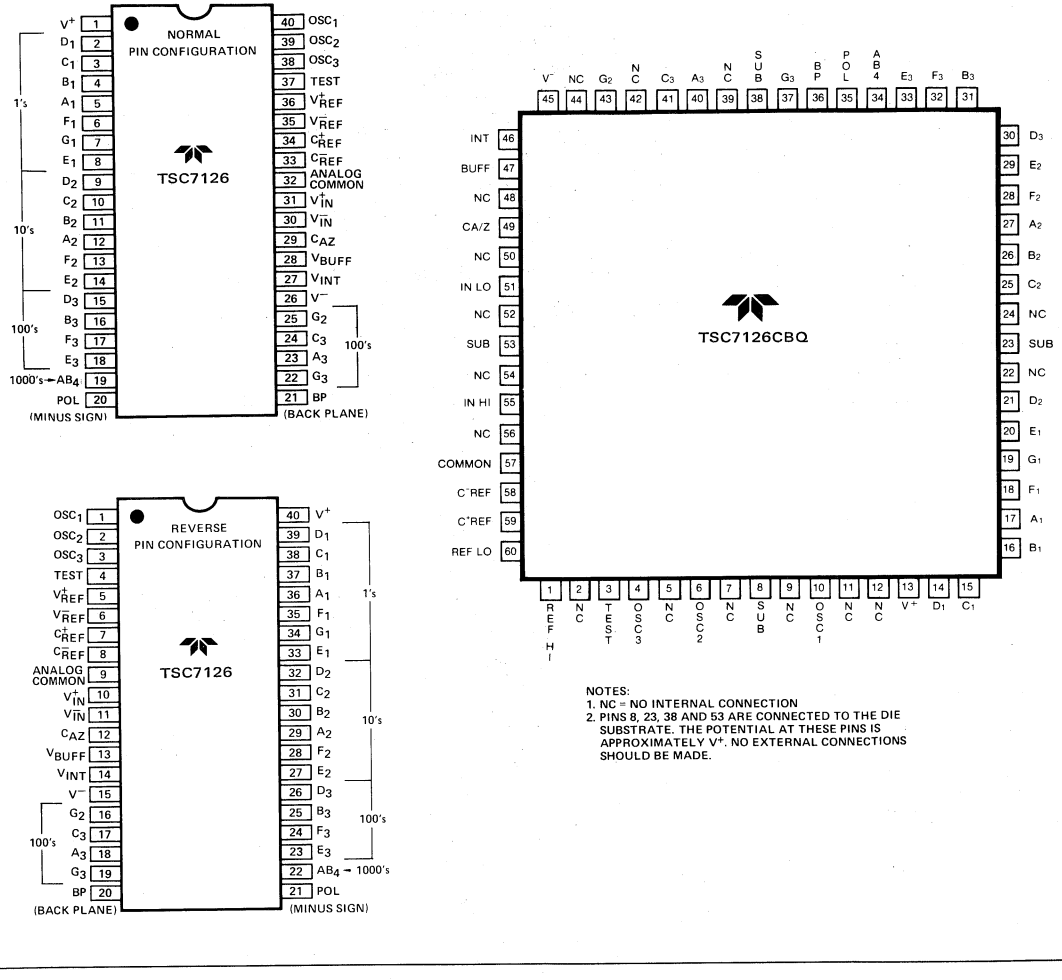
Notes:
1. Input voltages may exceed the supply voltages provided the input current is limited to ±100 μA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Unless otherwise noted, specifications apply at T_A = 25°C. f_{CLOCK} = 16 kHz and are tested in the circuit of Figure 1.
4. Refer to "Differential Input" discussion on page 4.
5. Backplane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50 mV.
6. During auto-zero phase, current is 10-20 μA higher. 48 kHz oscillator, Figure 2, increases current by 8 μa (typ.).

* Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

Ordering Information

Part No.	Package	Pin Layout	Temp. Range
TSC7126CPL	40-Pin Plastic Dip	Normal	0°C to 70°C
TSC7126RCPL	40-Pin Plastic Dip	Reversed	0°C 70°C
TSC7126IJL	40-Pin CerDIP	Normal	-25°C to +85°C
TSC7126CBQ	60-Pin Plastic Flat	Formed Leads	0°C to 70°C
TSC7126CSQ	60-Pin Plastic Flat	Unformed Leads	0°C to 70°C
Devices with 160 Hour, +125°C Burn-In			
TSC7126CPL/BI	40-Pin Plastic Dip	Normal	0°C to 70°C
TSC7126IJL/BI	40-Pin CerDIP	Normal	-25°C to +85°C

Pin Configuration



NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

Pin Description

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
1	(40)	13	V^+	Positive supply voltage.
2	(39)	14	D_1	Activates the D section of the units display.
3	(38)	15	C_1	Activates the C section of the units display.
4	(37)	16	B_1	Activates the B section of the units display.
5	(36)	17	A_1	Activates the A section of the units display.
6	(35)	18	F_1	Activates the F section of the units display.
7	(34)	19	G_1	Activates the G section of the units display.
8	(33)	20	E_1	Activates the E section of the units display.

Pin Description (Cont.)

40-Pin DIP Pin Number Normal	(Reverse)	60-Pin Flat Package Pin Number	Name	Description
9	(32)	21	D_2	Activates the D section of the units display.
10	(31)	25	C_2	Activates the C section of the tens display.
11	(30)	26	B_2	Activates the B section of the tens display.
12	(29)	27	A_2	Activates the A section of the tens display.
13	(28)	28	F_2	Activates the F section of the tens display.
14	(27)	29	E_2	Activates the E section of the tens display.
15	(26)	30	D_3	Activates the D section of the hundreds display.
16	(25)	31	B_3	Activates the B section of the hundreds display.
17	(24)	32	F_3	Activates the F section of the hundreds display.
18	(23)	33	E_3	Activates the E section of the hundreds display.
19	(22)	34	AB_4	Activates both halves of the 1 in the thousands display.
20	(21)	35	POL	Activates the negative polarity display.
21	(20)	36	BP	Backplane drive output.
22	(19)	37	G_3	Activates the G section of the hundreds display.
23	(18)	40	A_3	Activates the A section of the hundreds display.
24	(17)	41	C_3	Activates the C section of the hundreds display.
25	(16)	43	G_2	Activates the G section of the tens display.
26	(15)	45	V^-	Negative power supply voltage.
27	(14)	46	V_{INT}	The integrating capacitor should be selected to give the maximum voltage swing that ensures component tolerance build up will not allow the integrator output to saturate. When analog common is used as a reference and the conversion rate is 3 readings per second, a 0.047 μF capacitor may be used. The capacitor must have a low dielectric constant to prevent roll-over errors. See INTEGRATING CAPACITOR section for additional details.
28	(13)	47	V_{BUFF}	Integration resistor connection. Use a 180 kΩ for a 200 mV full-scale range and a 180 MΩ for 2 V full scale range.
29	(12)	49	C_{AZ}	The size of the auto-zero capacitor influences the system noise. Use a 0.33 μF capacitor for a 200 mV full-scale, and a 0.033 μF capacitor for a 2 volt full-scale. See paragraph on AUTO-ZERO CAPACITOR for more details.
30	(11)	51	V_{IN}^-	The low input is connected to this pin.
31	(10)	55	V_{IN}^+	The high input signal is connected to this pin.
32	(9)	57	Analog Common	This pin is primarily used to set the analog common-mode voltage for battery operation or in systems where the input signal is referenced to the power supply. See paragraph on ANALOG COMMON for more details. It also acts as a reference voltage source.
33	(8)	58	C_{REF}^-	See pin 34.
34	(7)	59	C_{REF}^+	A 0.1 μF capacitor is used in most applications. If a large common mode voltage exists (for example the V_{IN} pin is not at analog common), and a 200 mV scale is used, a 1.0 μF is recommended and will hold the rollover error to 0.5 count.
35	(6)	60	V_{REF}^-	See pin 36.
36	(5)	1	V_{REF}^+	The analog input required to generate a full-scale output (1,999 counts). Place 100 mV between pins 35 and 36 for 199.9 mV full-scale. Place 1.00 volts between pins 35 and 36 for 2 volts full-scale. See paragraph on REFERENCE VOLTAGE.
37	(4)	3	Test	Lamp test. When pulled high (to V^+) all segments will be turned on and the display should read -1888. It may also be used as a negative supply for externally generated decimal points. See paragraph under TEST for additional information.
38	(3)	4	OSC_3	See pin 40.
39	(2)	6	OSC_2	See pin 40.
40	(1)	10	OSC_1	Pins 40, 39, 38 make up the oscillator section. For a 48 kHz clock (3 readings per section) connect pin 40 to the junction of a 180 kΩ resistor and a 50 pF capacitor. The 180 kΩ resistor is tied to pin 39 and the 50 pF capacitor is tied to pin 38.

Detailed Description

ANALOG SECTION

Figure 3 shows the Block Diagram of the Analog Section for the 7126. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate, (DE).

1. Auto-zero phase

Input high and low are disconnected from the pins and internally shorted to analog COMMON. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. The offset referred to the input is less than 10μV.

2. Signal Integrate phase

The auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. De-integrate Phase

The final phase is reference integrate or de-integrate. Input low is internally connected to analog common and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. The digital reading displayed is

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (—) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition. See Component Values Selection.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 1.0 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator

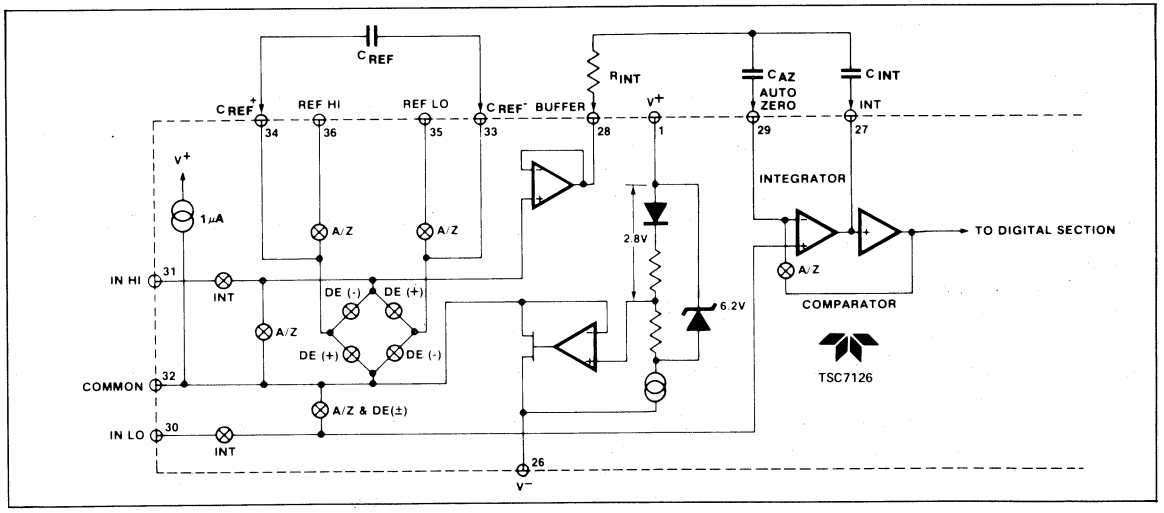


Figure 3: Analog Section of TSC7126.

positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

Analog Common

This pin is included primarily to set the common mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The common pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analog common has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the common voltage will have a low voltage coefficient (0.001%/%), low output impedance (≈15Ω), and a temperature coefficient typically less than 80 ppm/°C.

An external reference may be added to improve temperature stability. The circuit is shown in Figure 4.

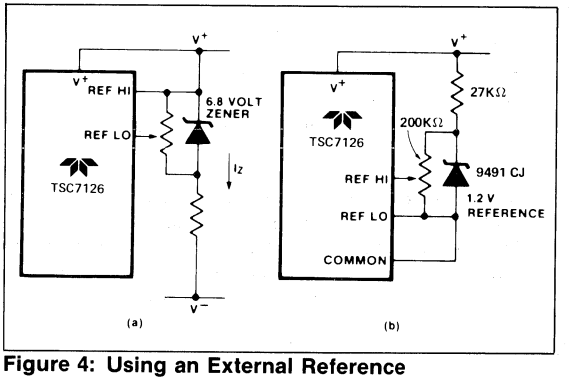


Figure 4: Using an External Reference

Analog common is also used as the IN LO return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC analog COMMON is tied to an N-channel FET that can sink 100 μA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 1 μA of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

Test

The TEST pin serves two functions. It is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. No more than a 1 mA load should be applied. Figures 5 and 6 show such an application.

The second function is a "lamp test". When TEST is pulled high (to V^+) all segments will be turned on and the display should read - 1888. The TEST pin will sink about 10 mA under these conditions

Caution: In the lamp test mode, the segments have a constant d-c voltage (no square-wave) and may burn the LCD display if left in this mode for several minutes.

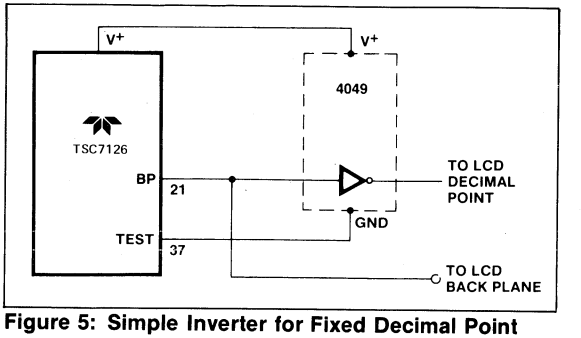


Figure 5: Simple Inverter for Fixed Decimal Point

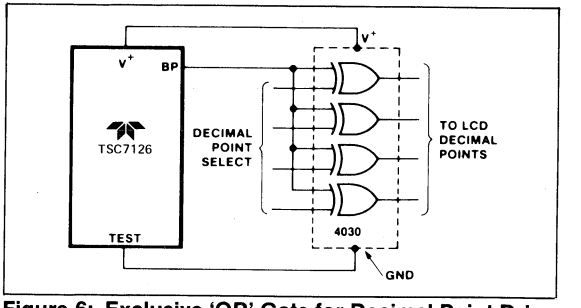


Figure 6: Exclusive 'OR' Gate for Decimal Point Drive

DIGITAL SECTION

Figure 8 shows the digital section for the 7126. An internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the backplane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with

BP when OFF, but out of phase when ON. In all cases, negligible d-c voltage exists across the segments. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

System Timing

Three clocking methods may be used: (Figure 7)

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference integrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48 kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 60 kHz, 48 kHz, 40 kHz, 33-1/3 kHz, etc. should be selected. For 50 Hz rejection, Oscillator frequencies of 66-2/3 kHz, 50 kHz, 40 kHz, etc. would be suitable. Note that 40 kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

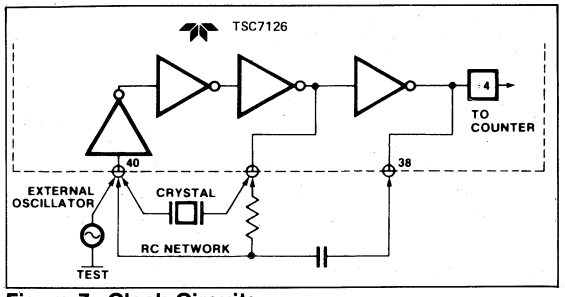


Figure 7: Clock Circuits

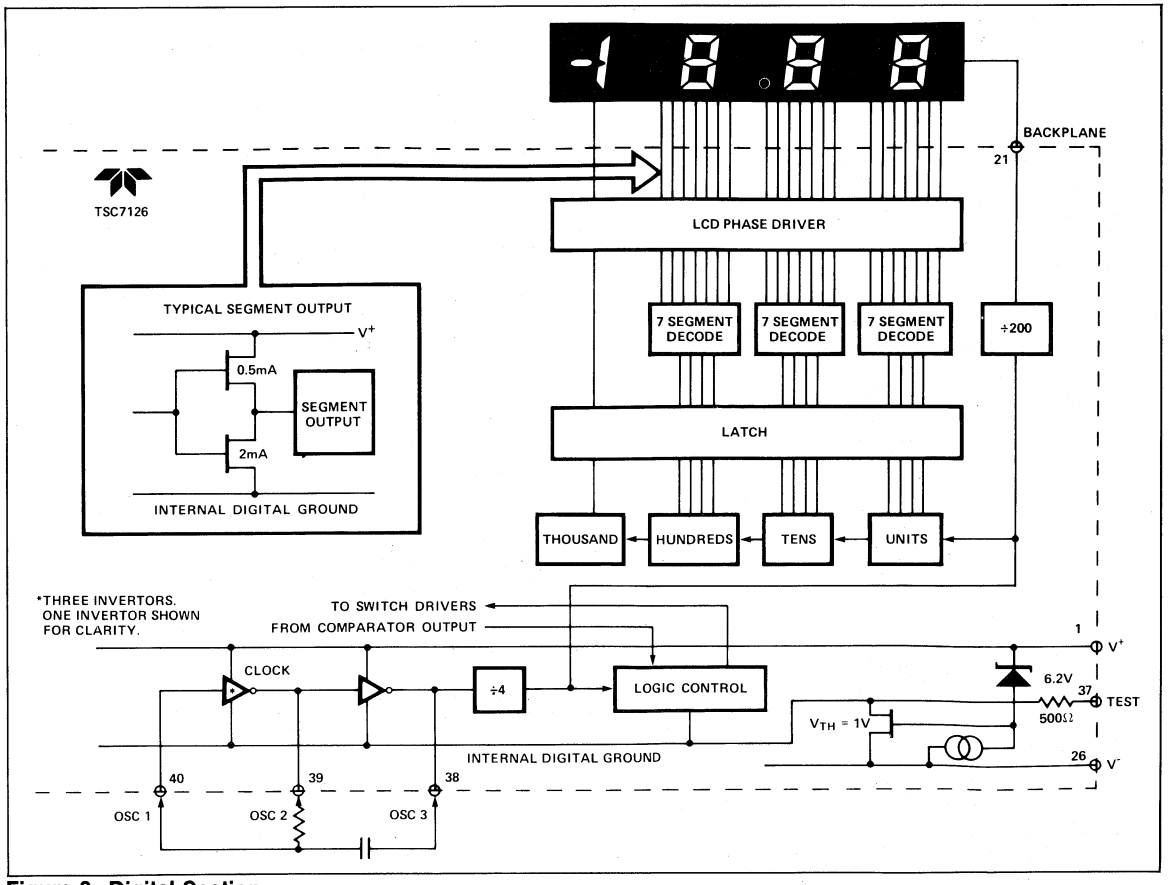


Figure 8: Digital Section

Component Value Selection

1. Auto-zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full scale where noise is very important, a 0.33 μF capacitor is recommended. On the 2 volt scale, a 0.033 μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

2. Reference Capacitor

A 0.1 μF capacitor is acceptable in most applications. However, where a large common mode voltage exists (i.e. the REF LO pin is not at analog COMMON) and a 200 mV scale is used, a larger value is required to prevent roll-over error. Generally 1.0 μF will hold the roll-over error to 0.5 count in this instance.

3. Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). When the analog COMMON is used as a reference, a nominal ±2 volt full scale integrator swing is acceptable). For three readings/second (48 kHz clock) nominal value for C_{INT} is 0.047 μF, for one reading per second (16 kHz) use 0.15 μF.

If different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the output swing.

The integrating capacitor must have low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are recommended for this application.

At three readings/sec., a 750Ω resistor should be placed in series with the integrating capacitor, to compensate for comparator delay.

4. Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6 μA of quiescent current. They can supply ~1 μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full scale, 1.8 MΩ is near optimum and similarly 180 KΩ for a 200.0 mV scale.

5. Oscillator Components

For all ranges of frequency a 50 pF capacitor is recommended and the resistor is selected from the approximate equation $f \sim \frac{45}{RC}$. For 48 kHz clock (3 readings/second), R = 180 KΩ.

6. Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2\ V_{REF}$. Thus, for the 200.0 mV and 2.000 volt scale, V_{REF} should equal 100.0 mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0 mV, the designer should use the input voltage directly and select V_{REF} = 0.341V. A suitable value for integrating resistor would be 330 KΩ. This makes the system slightly quieter and also avoids the necessity of a divider network on the input. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

Typical Applications

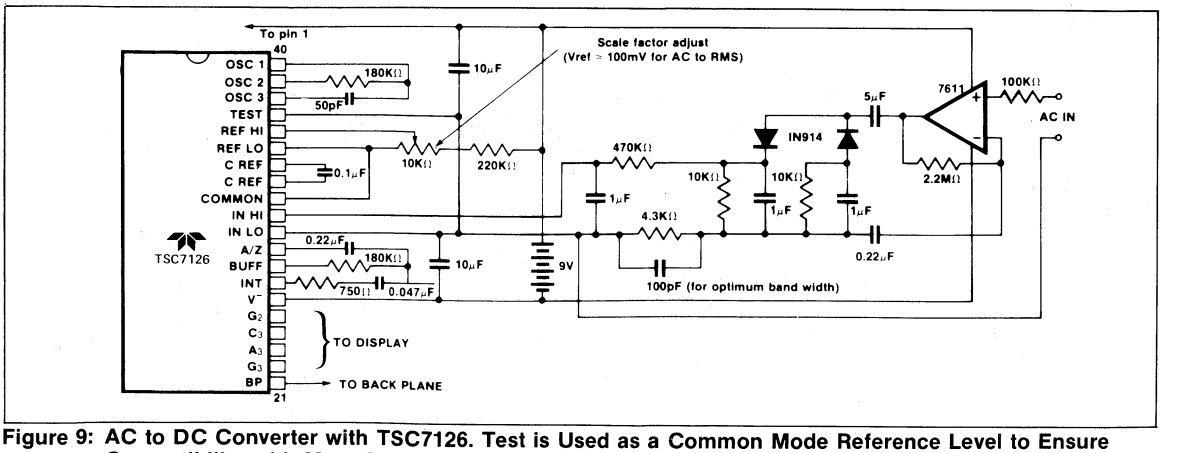


Figure 9: AC to DC Converter with TSC7126. Test is Used as a Common Mode Reference Level to Ensure Compatibility with Most Op-amps.

Typical Applications (Cont.)

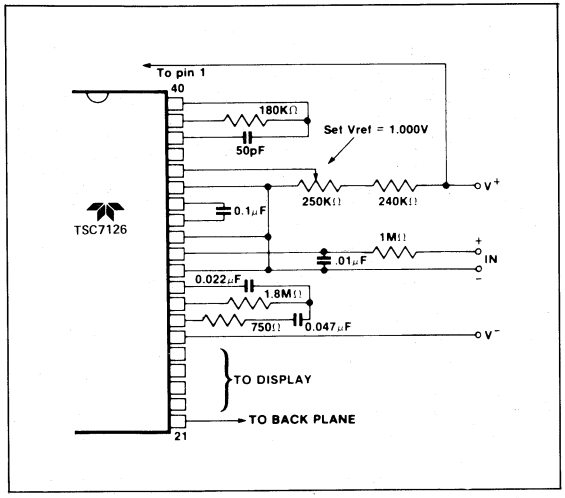


Figure 10: Recommended Values for 2.000 V Full-Scale, Three Readings Per Second.

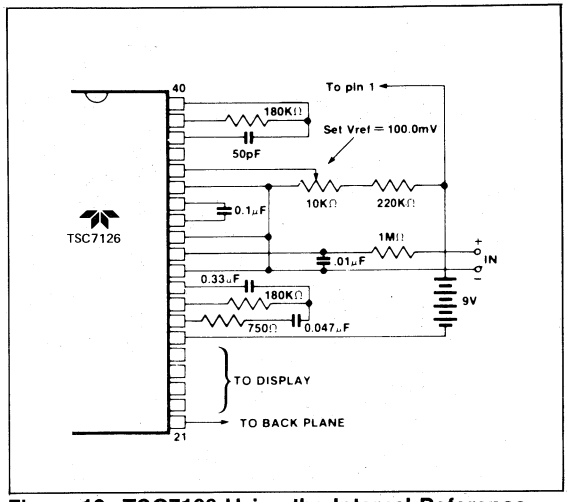


Figure 12: TSC7126 Using the Internal Reference. 200.0 mV Full-Scale, Three Readings Per Second, Floating Supply Voltage (9 V Battery).

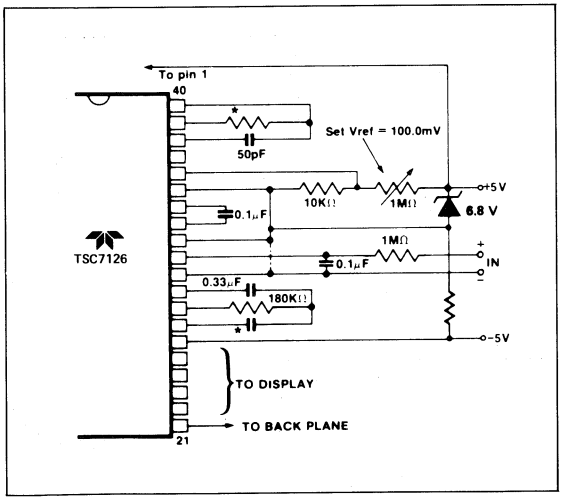


Figure 11: TSC7126 with Zener Diode Reference.

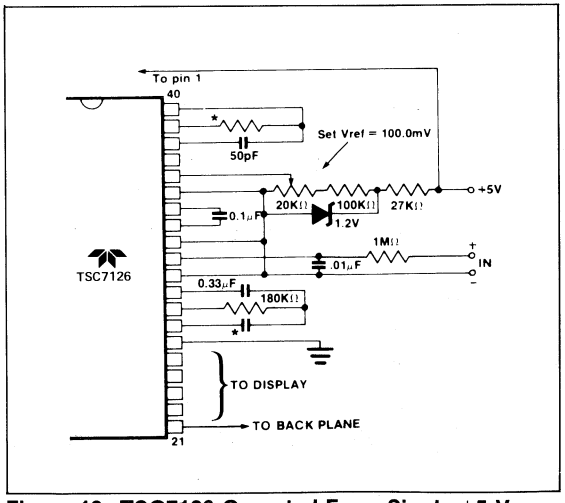


Figure 13: TSC7126 Operated From Single +5 V Supply. An External Reference Must Be Used.

Typical Applications (Cont.)

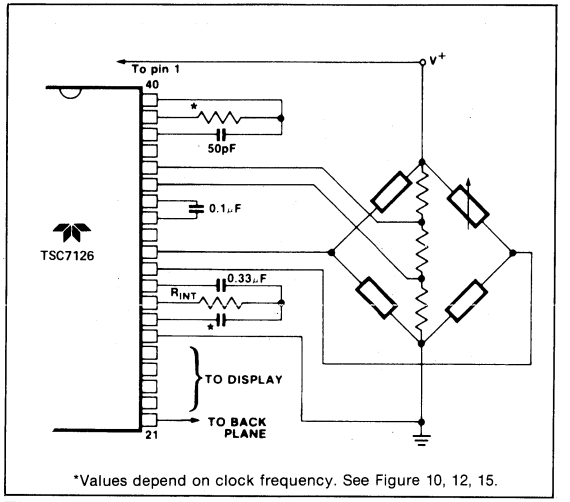


Figure 14: TSC7126 Measuring Ratiometric Values of Quad Load Cell. The Resistor Values Within the Bridge are Determined by the Desired Sensitivity.

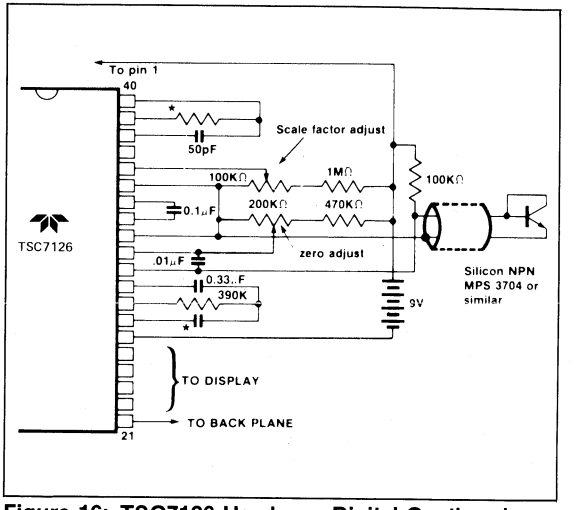


Figure 16: TSC7126 Used as a Digital Centigrade Thermometer. A Silicon Diode-Connected Transistor Has a Temperature Coefficient of About 2 mV/° C.

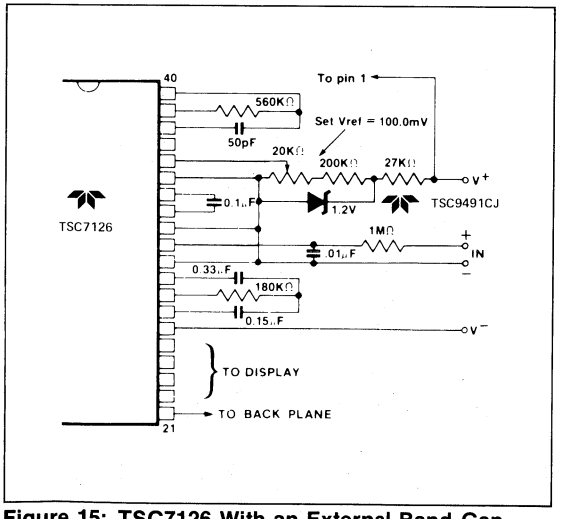


Figure 15: TSC7126 With an External Band-Gap Reference (1.2 V Typ) IN LO Is Tied to Common. Values Shown are for One Reading Per Second.

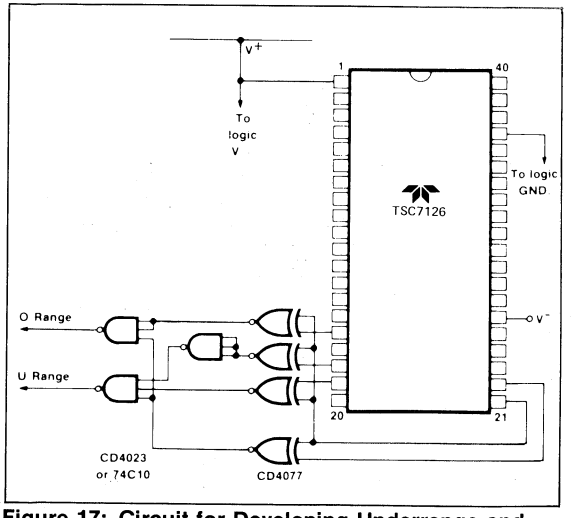


Figure 17: Circuit for Developing Underrange and Overrange Signals from TSC7126 Outputs.

Typical Applications (Cont.)

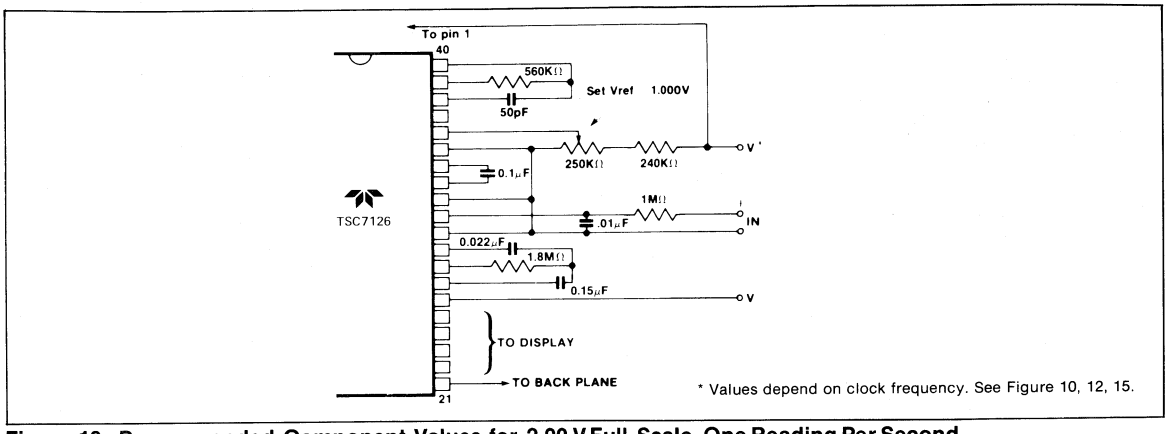
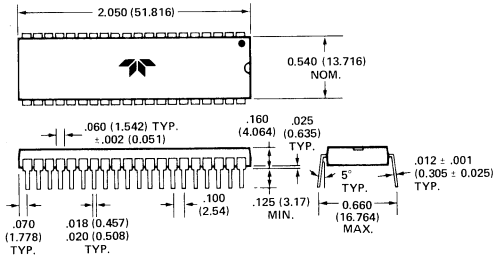


Figure 18: Recommended Component Values for 2.00 V Full-Scale, One Reading Per Second.

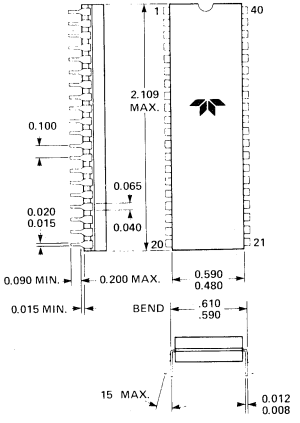
7

Package Information

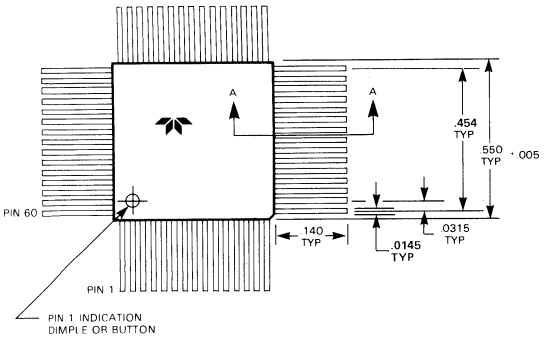
(Package #17)
40-Pin Plastic Dip (PL Package)



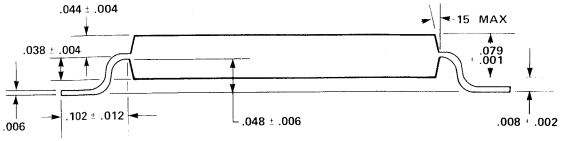
(Package #20)
40-Pin Cerdip



60-Pin Flat Package



"SQ" Package - Unformed Leads
(Package #22)



"BQ" Package - Formed Leads
(Package #21)

TSC7135
4 1/2 Digit Precision Analog-to-Digital Converter

General Description

The TSC7135 4 1/2 digit analog converter offers 50 ppm (1 part in 20,000) resolution with a maximum linearity error of 1 count. An auto-zero cycle reduces the zero error to below 10 μV and zero drift to 0.5 μV/°C. Source impedance error sources are minimized by a 10 pA maximum input current. Rollover error is limited to ± 1 count.

By combining the TSC7135 with a TSC7211A (LCD), TSC7212A (LED) or TSC700A (High LED Segment Current) driver a 4 1/2 digit display DVM or DPM can be constructed. Overrange and underrange signals support automatic range switching and special display blanking/flashing applications.

Micro-processor based measurement systems are supported by the TSC7135 Busy, $\overline{\text{Strobe}}$ and Run/$\overline{\text{HOLD}}$ control signals. Remote data acquisition systems with data transfer via UARTs are also possible. The additional control pins and multiplexed BCD outputs make the TSC7135 the ideal converter for display or μ-processor based measurement systems.

Ordering Information

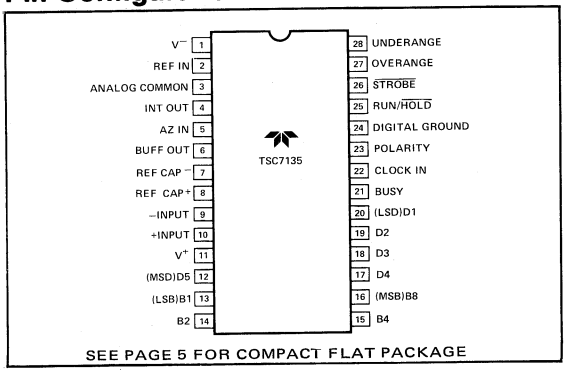
Part No.	Package	Temperature Range
TSC7135CJI	28-Pin CerDIP	0° C to +70° C
TSC7135CPI	28-Pin Plastic	0° C to +70° C
TSC7135CBQ	60-Pin Plastic Flat Package w/ Formed Leads	0° C to +70° C
TSC7135CSQ	60-Pin Plastic Flat Package w/ Unformed Leads	0° C to +70° C

Features

- Low Rollover Error ..... ± 1 Count Maximum
- Guaranteed ± 1 Count Maximum Error
- Guaranteed Zero Reading for 0 V Input
- True Polarity Indication at Zero for Null Detection
- Multiplexed BCD Data Output
- TTL Compatible Outputs
- Differential Input
- Control Signals Permit Interface to UARTS and μ-Processors
- Auto-ranging Supported with Over and Underrange Signals
- Blinking Display Visually Indicates Overrange Condition
- Low Input Current ..... 1 pA
- Low Zero Reading Drift ..... 2 μV/° C
- Interface to TSC7211A, TSC7212A, and TSC700A Display Drivers
- Available in Compact Flat Package

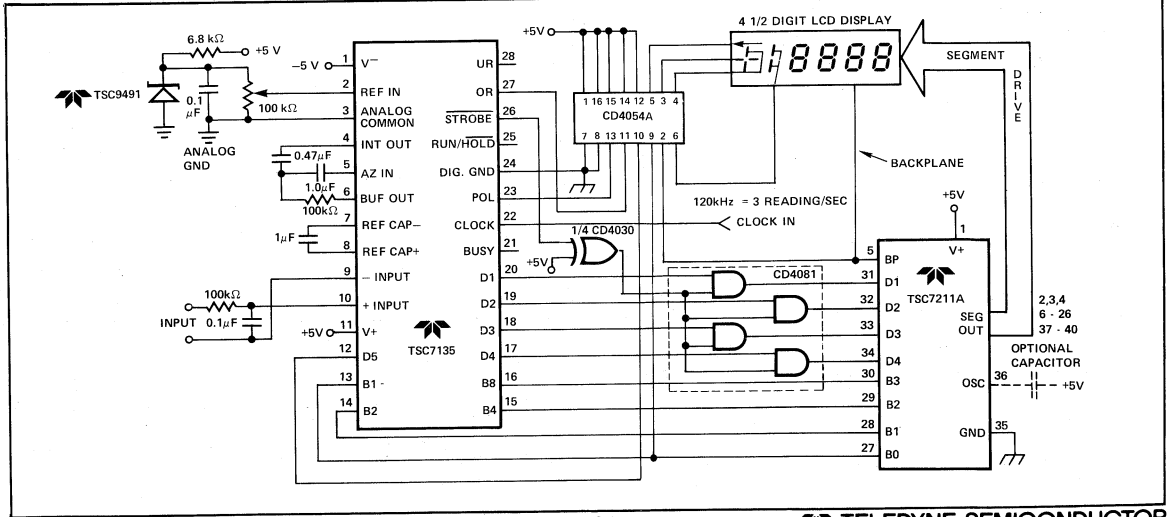
7

Pin Configuration



SEE PAGE 5 FOR COMPACT FLAT PACKAGE

Typical 4 1/2 Digit DVM with LCD Display



Absolute Maximum Ratings (Note 1)

Positive Supply Voltage ..... +6 V
Negative Supply voltage ..... -9 V
Analog Input Voltage (Pin 9 or 10) ..... V^+ to V^- (Note 2)
Reference Input Voltage (Pin 2) ..... V^+ to V^-
Clock Input Voltage ..... 0 V to V^+

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Soldering Lead Temperature (10 Seconds) ..... 300°C
CerDIP(J) Package Power Dissipation ..... 1 W
Plastic(P) Package Power Dissipation ..... 0.8 W

Electrical Specifications: T_A = 25°C, f_{CLOCK} = 120 kHz, V^+ = 5.0 V, V^- = -5 V

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC7135 MIN	TYP	MAX	UNIT
ANALOG SECTION	1		Display Reading with Zero Volt Input	Note 3,4	-0.0000	±0.0000	+0.0000	Display Reading
	2	TC_Z	Zero Reading Temperature Coefficient	V_{IN} = 0 V Note 5	—	0.5	2	μV/°C
	3	TC_{FS}	Full Scale Temperature Coefficient	V_{IN} = 2 V Notes 5,6	—	—	5	ppm/°C
	4	NL	Nonlinearity Error	Note 7	—	0.5	1	count
	5	DNL	Differential Linearity Error	Note 7	—	0.01	—	LSB
	6		Display Reading In Ratiometric Operation	V_{IN} = V_{REF} Note 3	+0.9998	+0.9999	+1.0000	Display Reading
	7	±FSE	± Full Scale Symmetry Error (Rollover Error)	$-V_{IN}$ = $+V_{IN}$ Note 8	—	0.5	1	count
	8	I_{IN}	Input Leakage Current	Note 4	—	1	10	pA
	9	V_N	Noise	Peak-to-Peak Value not exceed 95% of time	—	15	—	μV_{p-p}
DIGITAL SECTION	10	I_{NL}	Input Low Current	V_{IN} = 0 V	—	10	100	μA
	11	I_{NH}	Input High Current	V_{IN} = +5 V	—	0.08	10	μA
	12	V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA	—	0.20	0.40	V
	13	V_{OH}	Output High Voltage (B_1, B_2, B_4, B_8, D_1 - D_5)	I_{OH} = 1 mA	2.4	4.4	5.0	V
	14	V_{OH}	Output High Voltage (Busy, Polarity, Overrange, Underrange, Strobe)	I_{OH} = 10 μA	4.9	4.99	5.0	V
	15	f_{CLK}	Clock Frequency	Note 11	0	2100	1200	kHz
POWER SUPPLY	16	V^+	Positive Supply Voltage		4	5	6	V
	17	V^-	Negative Supply Voltage		-3	-5	-8	V
	18	I^+	Positive Supply Current	f_{CLK} = 0 Hz	—	1.0	3.0	mA
	19	I^-	Negative Supply Current	f_{CLK} = 0 Hz	—	0.7	3.0	mA
	20	Pd	Power Dissipation	f_{CLK} = 0 Hz	—	8.5	30	mW

Notes:

1. Functional operation is not implied.
2. Limit input current to under 100 μA if input voltages exceed supply voltage.
3. Full Scale Voltage = 2.000 V.
4. V_{IN} = 0.0000 V.
5. 0°C ≤ T_A ≤ +70°C.
6. External Reference Temperature Coefficient less than 0.01 ppm/°C.
7. -2 V ≤ V_{IN} ≤ +2 V. Error of reading from best fit straight line.
8. $|V_{IN}|$ = 1.9959.
9. Test Circuit shown in Figure 1.
10. Static Sensitive Device. Unused devices must be stored in conductive material to protect devices form static discharge and static fields.
11. Specification related to clock frequency range over which the TSC7135 correctly performs its various functions. Increased errors result at higher operating frequencies.

Test Circuits

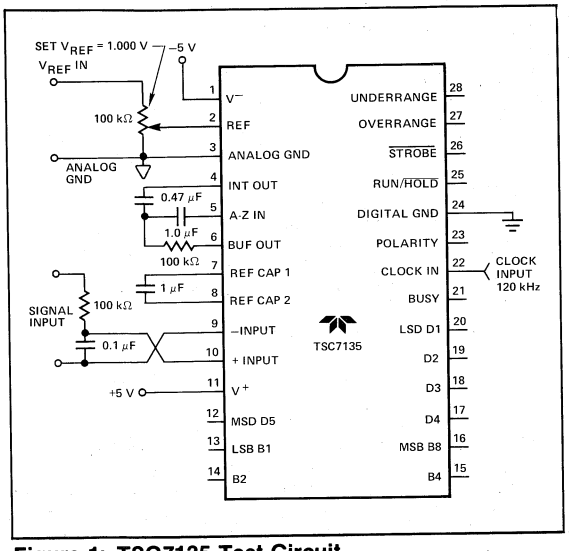


Figure 1: TSC7135 Test Circuit

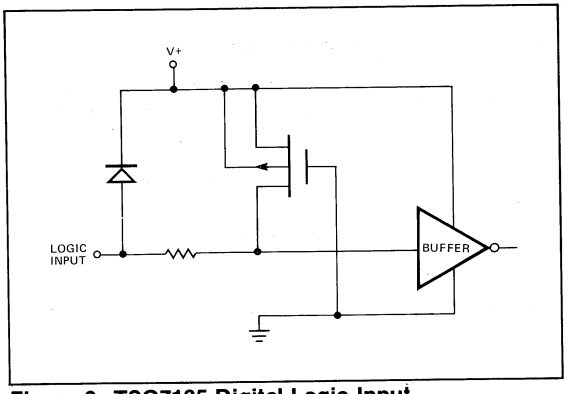


Figure 2: TSC7135 Digital Logic Input

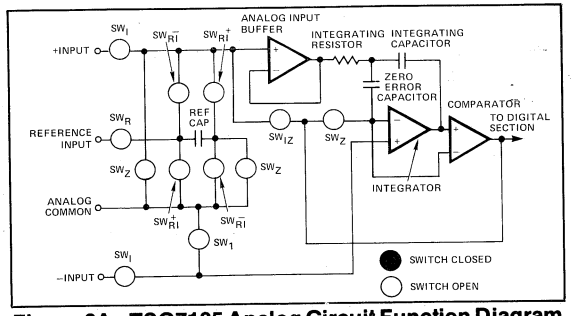


Figure 3A: TSC7135 Analog Circuit Function Diagram

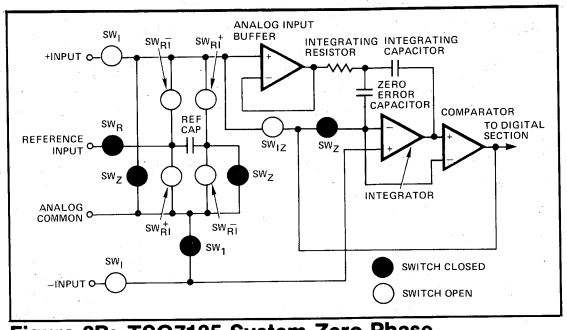


Figure 3B: TSC7135 System Zero Phase

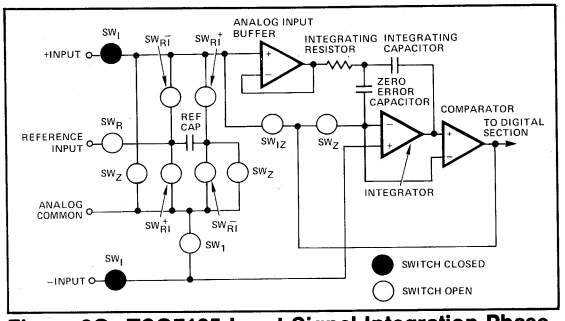


Figure 3C: TSC7135 Input Signal Integration Phase

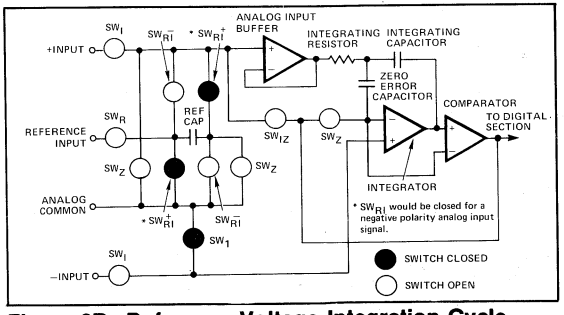


Figure 3D: Reference Voltage Integration Cycle

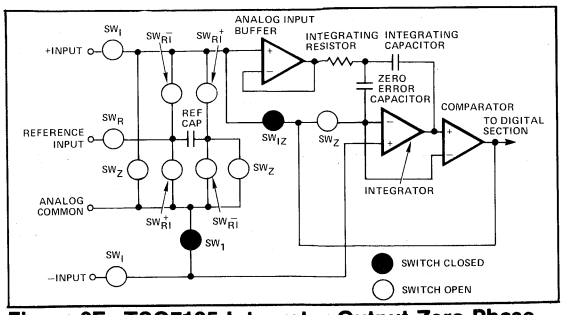


Figure 3E: TSC7135 Integrator Output Zero Phase

7

General Theory of Operation

Dual Slope Conversion Principles

The TSC7135 is a dual slope, integrating analog to digital converter. An understanding of the dual slope conversion technique will aid in following the detailed TSC7135 operation theory.

The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period. Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal.

In a simple dual slope converter a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

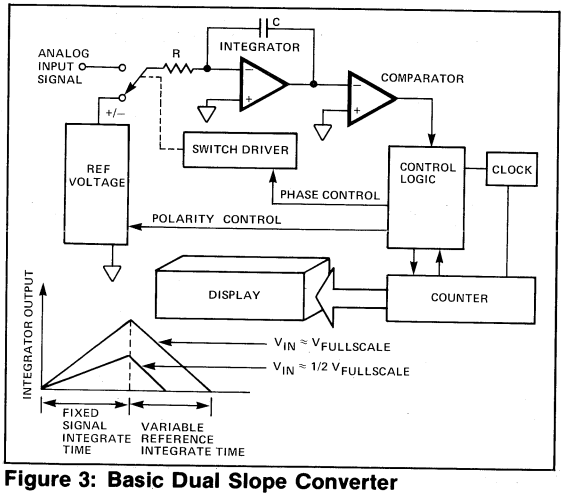


Figure 3: Basic Dual Slope Converter

A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{RC}\int_0^{T_{SI}} V_{IN}(t)\,dt = \frac{V_R\,T_{RI}}{RC}$$

where:

V_R = Reference Voltage

T_{SI} = Signal Integration Time (Fixed)

T_{RI} = Reference Voltage Integration Time (Variable)

For a constant V_{IN}:

$$V_{IN} = V_R\left[\frac{T_{RI}}{T_{SI}}\right]$$

The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments.

TSC7135 Operation Theory

The TSC7135 incorporates a system zero and integrator output voltage zero phase to the normal two phase dual slope measurement cycle. Reduced system errors, fewer calibration steps and a shorter overrange recovery time result.

The TSC7135 measurement cycle contains four phases:

- System Zero
- Analog Input Signal Integration
- Reference Voltage Integration
- Integrator Output Zero

Internal analog gate status is shown in Table 1 for each phase.

Table 1: Internal Analog Gate Status

Conversion Cycle Phase	Internal Analog Gate Status							Reference Schematic
	SW_I	SW^+_{RI}	SW^-_{RI}	SW_Z	SW_R	SW_1	SW_{IZ}	
System Zero				Closed	Closed	Closed		3 A
Input Signal Integration	Closed							3 B
Reference Voltage Integration		Closed*				Closed		3 C
Integrator Output Zero						Closed	Closed	3 D

Note: *Assumes a positive polarity input signal. SW^-_{RI} would be closed for a negative input signal.

System Zero Phase (Figure 3B)

During this phase errors due to buffer, integrator and comparator offset voltages are compensated for by charging C_{AZ} (auto-zero capacitor) with a compensating error voltage. With a zero input voltage the integrator output will remain at zero.

The external input signal is disconnected from the internal circuitry by opening the two SW_I switches. The internal input points connect to analog common. The reference capacitor charges to the reference voltage potential through SW_R. A feedback loop, closed around the integrator and comparator, charges the C_{AZ} capacitor with a voltage to compensate for buffer amplifier, integrator and comparator offset voltages.

Analog Input Signal Integration Phase

(Figure 3C)

The TSC7135 integrates the differential voltage between the + Input and - Input. The differential voltage must be within the device common-mode range; -1 V from either supply rail typically.

The input signal polarity is determined at the end of this phase.

Reference Voltage Integration (Figure 3D)

The previously charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero. The digital reading displayed is:

$$\text{Reading} = 10{,}000 \left[\frac{\text{Differential Input}}{V_{REF}} \right]$$

Integrator Output Zero (Figure 3E)

This phase guarantees the integrator output is at zero volts when the system zero phase is entered and that the true system offset voltages are compensated for. This phase normally lasts 100 to 200 clock cycles. If an overrange condition exists the phase is extended to 6200 clock cycles.

Analog Pin Functional Description

Differential Inputs (+ Input (Pin 10) and -Input (Pin 9))

The TSC7135 operates with differential voltages within the input amplifier common-mode range. The input amplifier common-mode range extends from 0.5 V below the positive supply to 1.0 V above the negative supply. Within this common-mode voltage range an 86 dB common-mode rejection ratio is typical.

The integrator output also follows the common-mode voltage. The integrator output must not be allowed to saturate. A worst case condition exists, for example, when a large positive common-mode voltage with a near full scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4 V full scale swing with some loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

Analog Common (Pin 3)

Analog COMMON is used as the -Input return during auto-zero and de-integrate. If -Input is different from analog COMMON, a common-mode voltage exists in the system. This signal is rejected by the excellent CMRR of the converter. In most applications -Input will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common-mode voltage from the converter. The reference voltage is referenced to analog COMMON.

Reference Voltage (REF IN (Pin 2))

The REF IN reference voltage input must be a positive voltage with respect to analog COMMON. Two reference voltage circuits are shown in Figure 4.

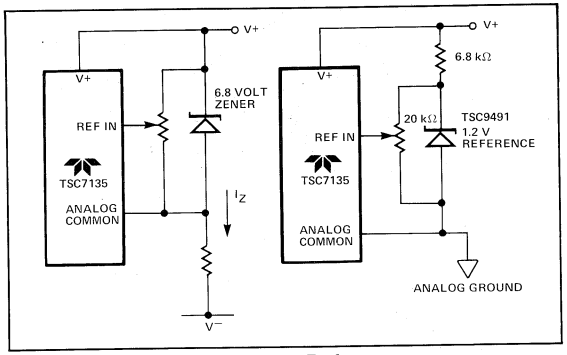
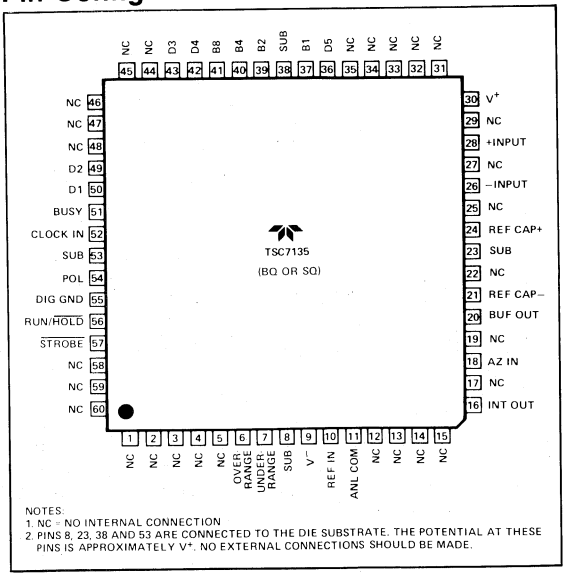


Figure 4: Using an External Reference

The TSC7135 digital section is shown in Figure 5. Timing relationships are shown in Figure 6.

Pin Configuration



NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

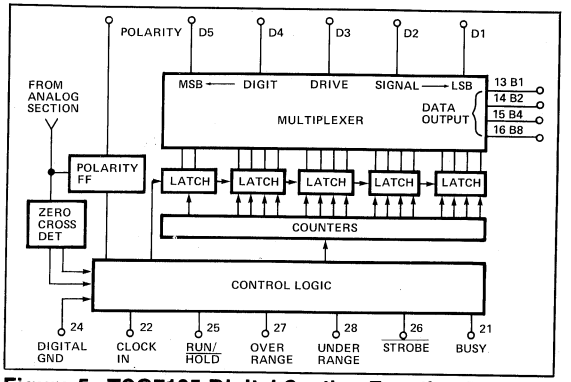


Figure 5: TSC7135 Digital Section Function Diagram

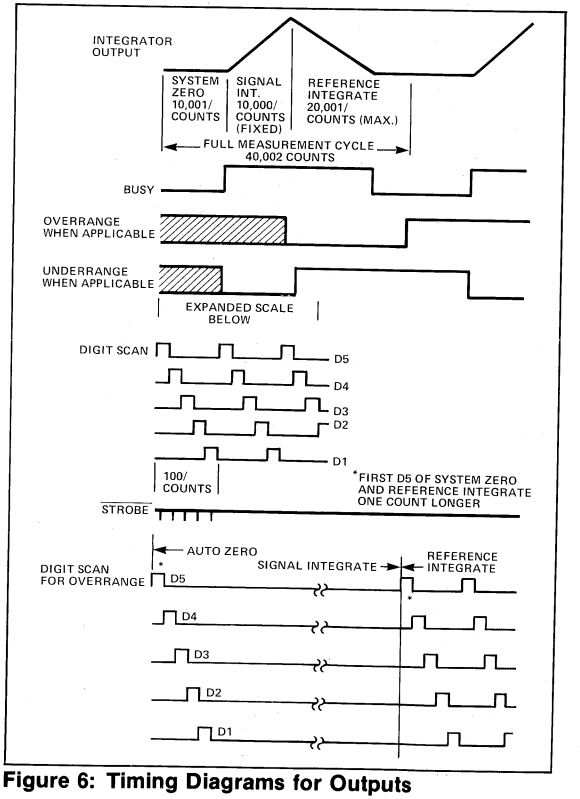


Figure 6: Timing Diagrams for Outputs

TSC7135 Digital Section Functional Description

The major digital subsystems within the TSC7135 are illustrated in Figure 5 with timing relationships shown in Figure 6. The multiplexed BCD output data can be displayed on LCD or LED displays with the TSC700A (LED), TSC7211A (LCD), or TSC7212A (LED) four digit display drivers.

The digital section is best described through a discussion of the control signals and data outputs.

Run/$\overline{\text{Hold}}$ Input (Pin 25)

When left open this pin assumes a logic 1 level. With R/$\overline{\text{H}}$ = 1 the TSC7135 performs conversions continuously with a new measurement cycle beginning every 40,002 clock pulses.

When R/$\overline{\text{H}}$ changes to a logic 0 the measurement cycle in progress will be completed and data held and displayed as long as the logic 0 condition exists.

A positive pulse (>300 ns) at R/$\overline{\text{H}}$ will initiate a new measurement cycle. The measurement cycle in progress when R/$\overline{\text{H}}$ initially assumed the logic "0" state must be completed before the positive pulse can be recognized as a single conversion run command.

The new measurement cycle begins with a 10,001 count auto-zero phase. At the end of this phase the busy signal goes high.

$\overline{\text{Strobe}}$ Output (Pin 26)

During the measurement cycle the $\overline{\text{STROBE}}$ control line is pulsed low five times. The five low pulses occur in the center of the digit drive signals (D_1, D_2, D_3, D_5). (Figure 7)

D_5 (MSD) goes high for 201 counts when the measurement cycles end. In the center of the D_5 pulse, 101 clock pulses after the end of the measurement cycle, the first $\overline{\text{STROBE}}$ occurs for one-half clock pulse. After the D_5 digit strobe, D_4 goes high for 200 clock pulses. The $\overline{\text{STROBE}}$ goes low 100 clock pulses after D_4 goes high. This continues through the D_1 digit drive pulse.

The digit drive signals will continue to permit display scanning. $\overline{\text{STROBE}}$ pulses are not repeated until a new measurement is completed. The digit drive signals will not continue if the previous signal resulted in an overrange condition.

The active low $\overline{\text{STROBE}}$ pulses aid BCD data transfer to UARTs, processors and external latches. See Application Note AN16.

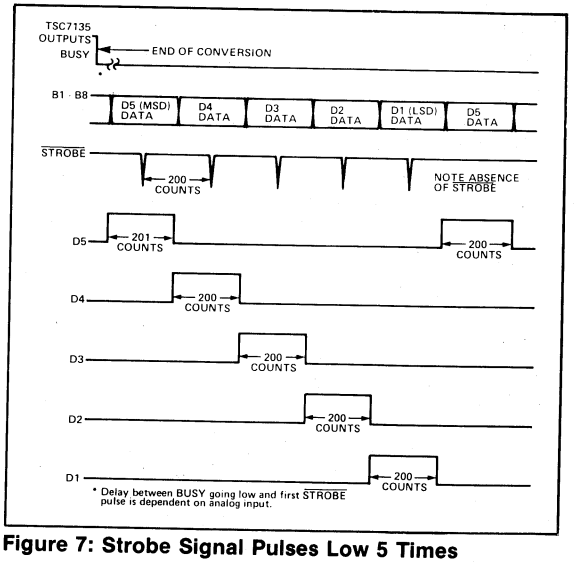


Figure 7: Strobe Signal Pulses Low 5 Times Per Conversion.

Busy Output (Pin 21)

At the beginning of the signal integration phase BUSY goes high and remains high until the first clock pulse after the integrator zero crossing. BUSY returns to the logic "0" state after the measurement cycle ends in a overrange condition. The internal display latches are loaded during the first clock pulse after busy and are latched at the clock pulse end. The busy signal does not go high at the beginning of the measurement cycle which starts with the auto-zero cycle.

Overrange Output (Pin 27)

If the input signal causes the reference voltage integration time to exceed 20,000 clock pulses the overrange output is set to a logic 1. The overrange output register is set when BUSY goes low and is reset at the beginning of the next reference integration phase.

TSC7135 Digital Section Functional Description (Cont.)

Underrange Output (Pin 28)

If the output count is 9% of full scale or less (≤1800 counts) the underrange register bit is set at the end of BUSY. The bit is set low at the next signal integration phase.

Polarity Output (Pin 23)

A positive input is registered by a logic 1 polarity signal. The polarity bit is valid at the beginning of reference integrate and remains valid until determined during the next conversion.

The polarity bit is valid even for a zero reading. Signals less than the converters LSB will have the signal polarity determined correctly. This is useful in null applications.

Digit Drive Outputs (Pins 12, 17, 18, 19 & 20)

Digit drive signals are positive going signals. The scan sequence is D_5 to D_1. All positive pulses are 200 clock pulses wide except D_5 which is 201 clock pulses wide.

All five digits are scanned continuously unless an overrange condition occurs. In an overrange condition all digit drives are held low from the final STROBE pulse until the beginning of the next reference integrate phase. The scanning sequence is then repeated. This provides a blinking visual display indication.

BCD Data Outputs (Pins 13, 14, 15 and 16)

The binary coded decimal bits B_8, B_4, B_2, B_1 are positive true logic signals. The data bits become active simultaneously with the digit drive signals. In an overrange condition all data bits are at a logic "0" state.

Applications Information

Component Value Selection

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. Both the buffer amplifier and the integrator have a class A output stage with 100 μA of quiescent current. A 20 μA drive current gives negligible linearity errors. Values of 5 to 40 μA give good results. The exact value of integrating resistor for a 20 μA current is easily calculated.

$$R_{INT} = \frac{\text{full-scale voltage}}{20\ \mu A}$$

Integrating Capacitor

The product of integrating resistor and capacitor should be selected to give the maximum voltage swing which ensures that the tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). For ±5 volt supplies and analog COMMON tied to supply ground, a ±3.5 to ±4 volt full scale integrator swing is adequate. A 0.10 μF to 0.47 μF is recommended. In general, the value of C_{INT} is given by:

$$C_{INT} = \frac{[10{,}000 \times \text{clock period}] \times I_{INT}}{\text{Integrator output voltage swing}}$$

$$= \frac{(10{,}000)\ (\text{clock period})\ (20\mu A)}{\text{Integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it has low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference. This ratiometric condition should read half scale 0.9999. Any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

Auto-Zero and Reference Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. A large capacitor reduces the noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Smaller or cheaper caps can be used if accurate readings are not required for the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full-scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. For this reason, it is recommended that a high quality reference be used where high-accuracy absolute measurements are being made. Suitable references are:

Part Type	Manufacturer
TSC9491	Teledyne Semiconductor
MC1400U2	Motorola

Conversion Timing

Line Frequency Rejection

A signal integration period at a multiple of the 60 Hz line frequency will maximize 60 Hz "line noise" rejection.

A 100 kHz clock frequency will reject both 50 Hz, 60 Hz and 400 Hz noise. This corresponds to 2.5 readings per second.

Oscillator Frequency	Frequency Rejected
300 kHz, 200 kHz, 150 kHz, 120 kHz, 100 kHz, 40 kHz, 33 1/3 kHz	60 Hz
250 kHz, 166 2/3 kHz, 125 kHz, 100 kHz	50 Hz
100 kHz	50 Hz, 60 Hz, 400 Hz

Conversion Rate vs Clock Frequency

Oscillator Frequency (kHz)	Conversion Rate (Conv/Sec)
100	2.5
120	3
200	5
300	7.5
400	10
800	20
1,200	30

Power Supplies and Grounds

Power Supplies

The TSC7135 is designed to work from ±5 V supplies. The conditions to use a single +5 V supply are:

- The input signal is referenced to the center of the common mode range of the converter.
- The signal is less than ±1.5 volts.

Grounding

Systems should use separate digital and analog ground systems to avoid loss of accuracy.

Displays and Driver Circuits

Teledyne Semiconductor manufactures three display decoder/driver circuits to interface the TSC7135 to LCD or LED displays. Each driver has 28 outputs for driving four seven segment digit displays. The TSC700A features increased LED segment drive current for greater display brightness.

Device	Package	Description
TSC7211AIPL	40 Pin Epoxy	4 Digit LCD Driver/Decoder
TSC7212AIPL	40 Pin Epoxy	4 Digit LED Driver/Decoder
TSC700AIJL	40 Pin CerDIP	4 Digit LED Driver/Decoder with high LED Segment Current ($I_{SEG} \geq 11$ mA)

Several sources exist for LCD and LED displays:

Manufacturer	Address	Display Type
Hewlett Packard Components	640 Page Mill Rd Palo Alto, CA 94304	LED
Litronix, Inc.	19000 Homestead Rd. Cupertino, CA 94010	LED
And	770 Airport Blvd. Burlingame, CA 94010	LCD and LED
Epson America, Inc.	3415 Kanhi Kawa St. Torrence, CA 90505	LCD

High Speed Operation

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. The comparator in this circuit follows the integrator ramp with a 3 μs delay, and at a clock frequency of 160 kHz (6 μs period) half of the first reference integrate clock period is lost in delay. This means that the meter reading will change from 0 to 1 with a 50 μV input, 1 to 2 with 150 μV, 2 to 3 at 250 μV, etc. This transition at mid-point is considered desirable by most users; however, if the clock frequency is increased appreciably above 160 kHz, the instrument will flash "1" on noise peaks even when the input is shorted.

For many-dedicated applications where the input signal is always of one polarity, the delay of the comparator need not be a limitation. Since the non-linearity and noise do not increase substantially with frequency, clock rates of up to ~1 MHz may be used. For a fixed clock frequency, the extra count or counts caused by comparator delay will be a constant and can be subtracted out digitally.

The clock frequency may be extended above 160 kHz without this error, however, by using a low value resistor in series with the integrating capacitor. The effect of the resistor is to introduce a small pedestal voltage on to the integrator output at the beginning of the reference integrate phase. By careful selection of the ratio between this resistor and the integrating resistor (a few tens of ohms in the recommended circuit), the comparator delay can be compensated and the maximum clock frequency extended by approximately a factor of 3. At higher frequencies, ringing and second order breaks will cause significant non-linearities in the first few counts of the instrument.

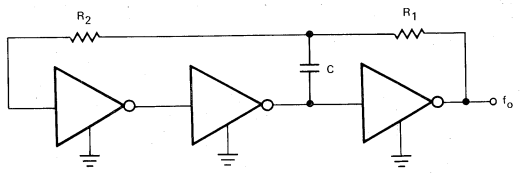
The minimum clock frequency is established by leakage on the auto-zero and reference caps. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

The clock used should be free from significant phase or frequency jitter. Several suitable low-cost oscillators are shown in the Applications section. The multiplexed output means that if the display takes significant current from the logic supply, the clock should have good PSRR.

Zero-Crossing Flip-Flop

The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. False zero-crossings caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by up to one count in every instance, and if a correction were not made, the display would always be one count too high. Therefore, the counter is disabled for one clock pulse at the beginning of the reference integrate (de-integrate) phase. This one-count delay compensates for the delay of the zero-crossing flip-flop, and allows the correct number to be latched into the display. Similarly, a one-count delay at the beginning of auto-zero gives an overload display of 0000 instead of 0001. No delay occurs during signal integrate, so that true ratiometric readings result.

Application Circuits



Gates are 74C04

1. $f_O \approx \frac{1}{2\,C[0.41\,R_P + 0.70\,R_1]}$, $R_P = \frac{R_1\,R_2}{R_1 + R_2}$

a. If $R_1 = R_2 = R_1$, $f \cong 0.55/RC$

b. If $R_2 >> R_1$, $f \cong 0.45/R_1C$

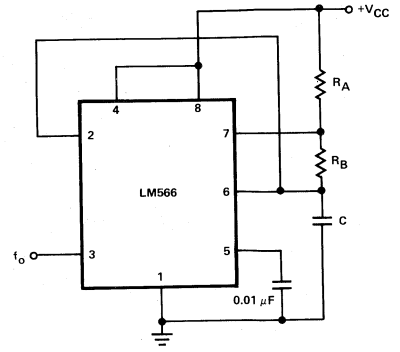
c. If $R_2 << R_1$, $f \cong 0.72/R_1C$

a. f = 120 kHz, C = 420 pF
$R_1 = R_2 \approx 10.9\ k\,\Omega$

b. f = 120 kHz, C = 420 pF, R_2 = 50 k Ω
R_1 = 8.93 k Ω

c. f = 120 kHz, C = 220 pF, R_2 = 5 k Ω
R_1 = 27.3 k Ω

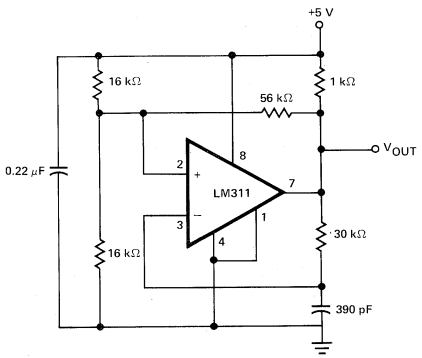
Figure A: R/C Oscillator



$$f = \frac{1.44}{(R_A + 2\,R_B)\,C}\ ,\quad \text{duty cycle} = \frac{R_B}{R_A + 2\,R_B}$$

a. f = 120 kHz, C = **1200 pF, $R_A + 2R_B$ = 10 kΩ**

Figure B: "555" Timer Oscillator



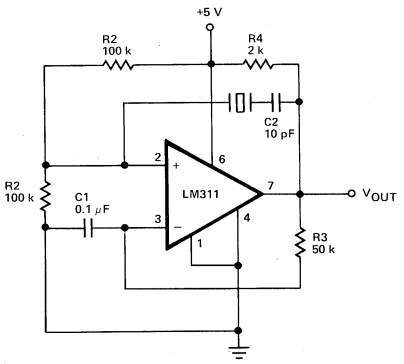
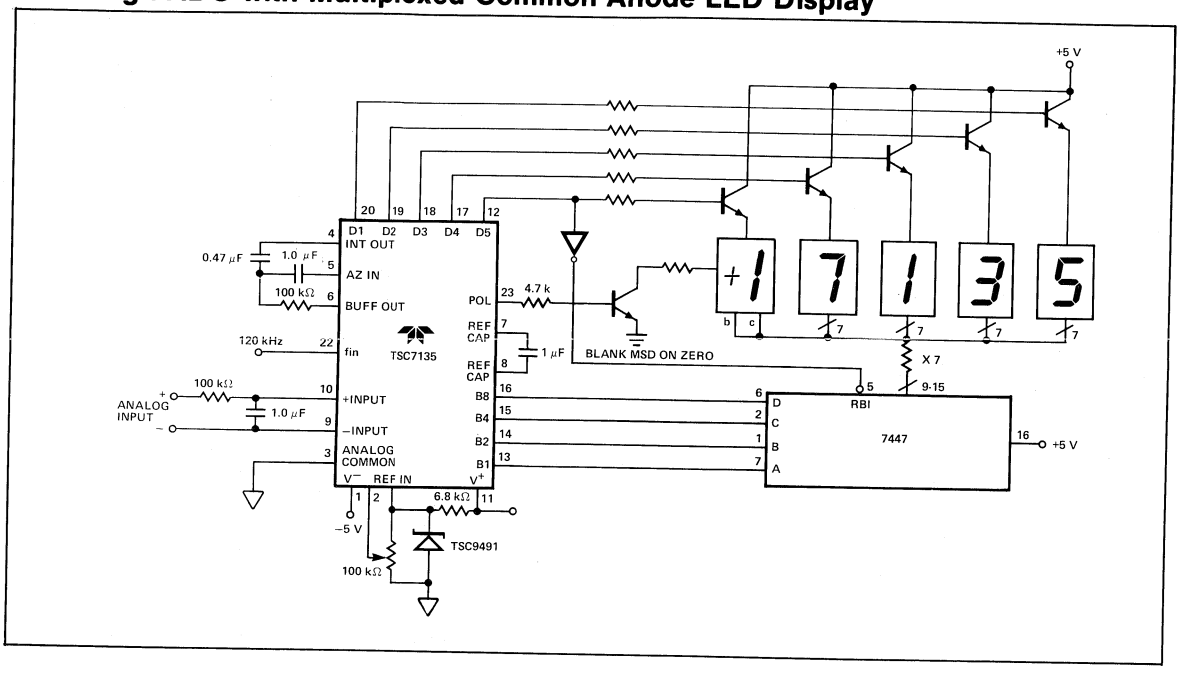
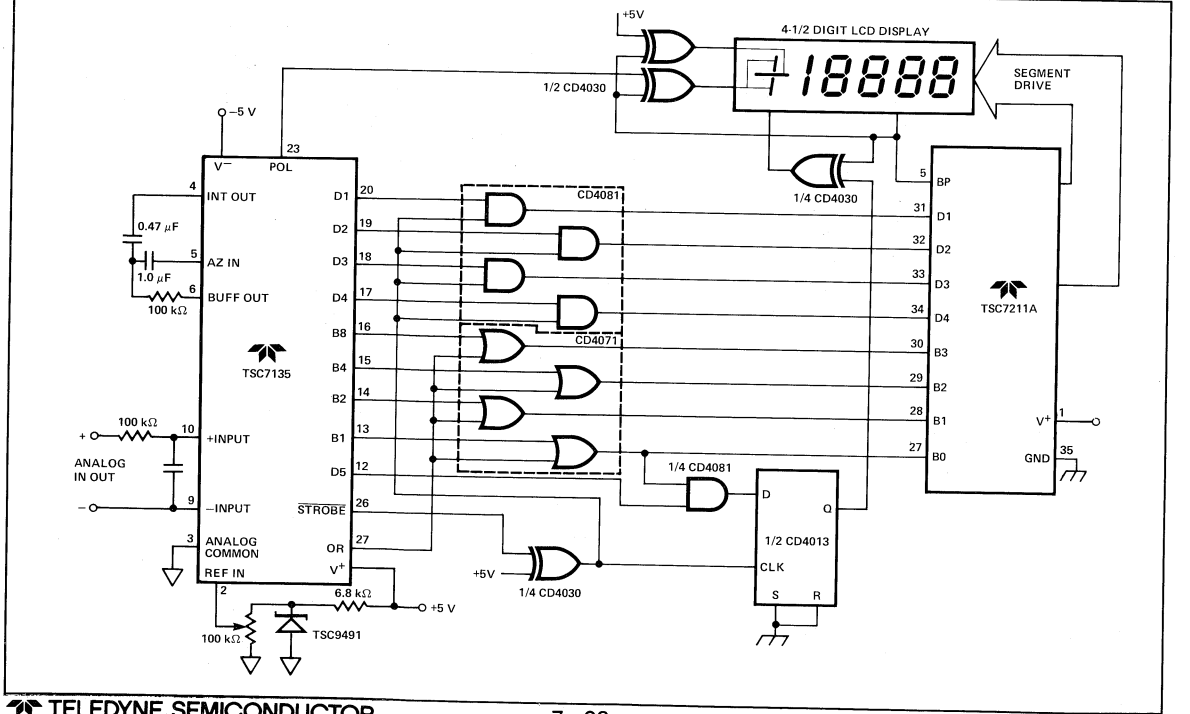


Figure C: Comparator Clock Circuit

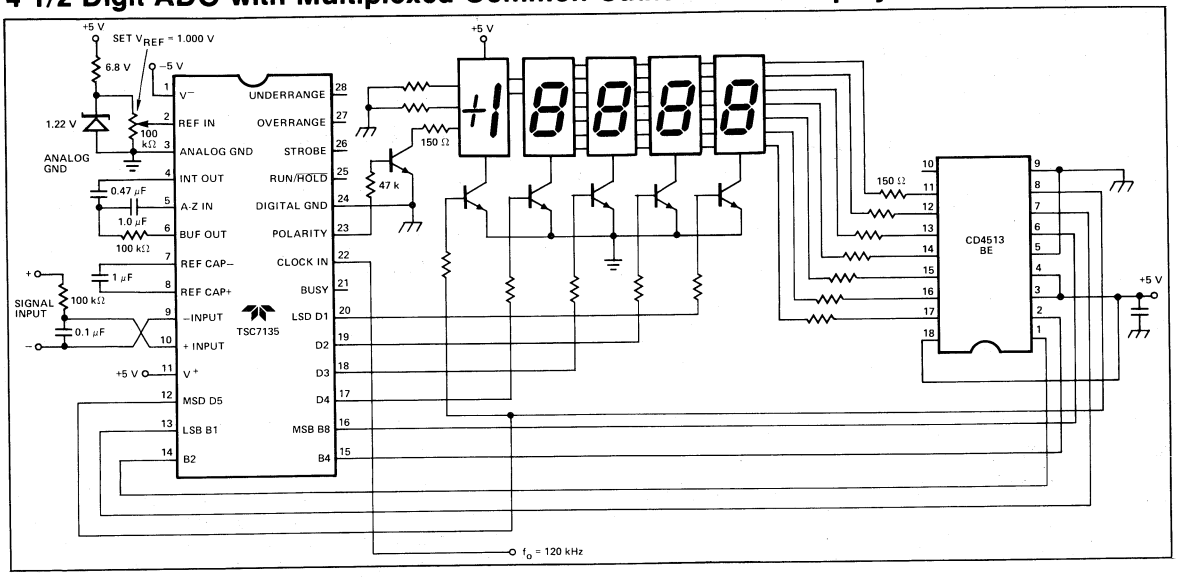
4 1/2 Digit ADC with Multiplexed Common Anode LED Display



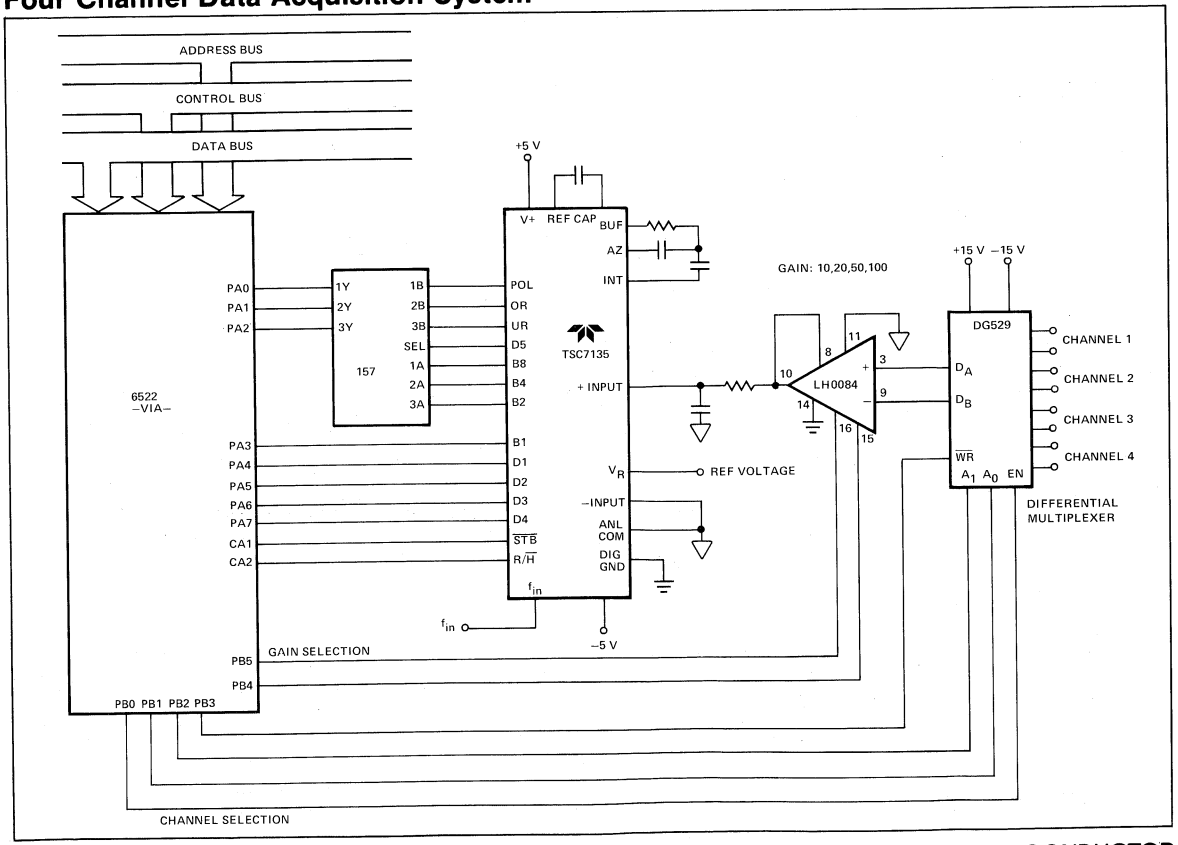
4 1/2 Digit ADC Interfaced to LCD Display with Digit Blanking on Overrange



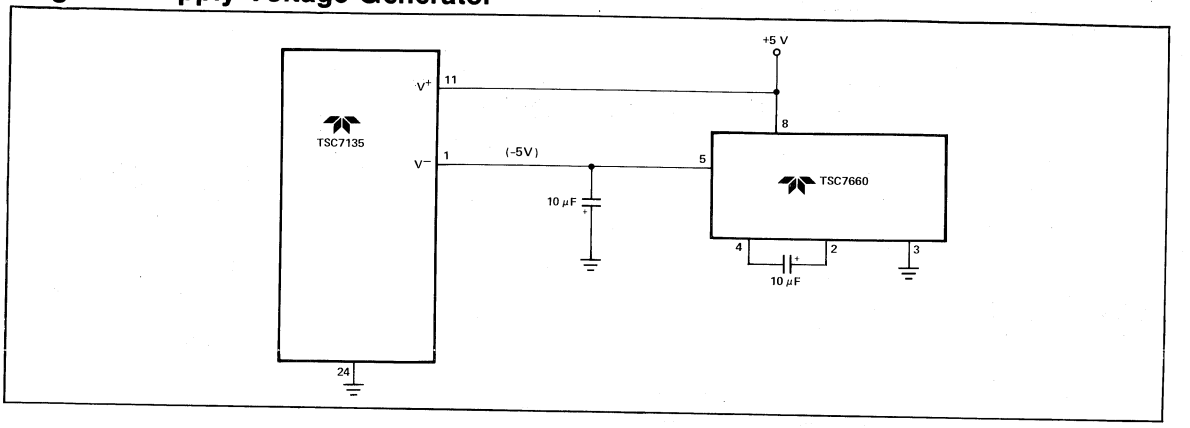
4 1/2 Digit ADC with Multiplexed Common Cathode LED Display



Four Channel Data Acquisition System



Negative Supply Voltage Generator

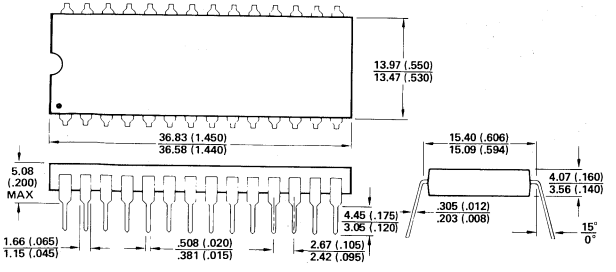


Output Voltage vs Output Current

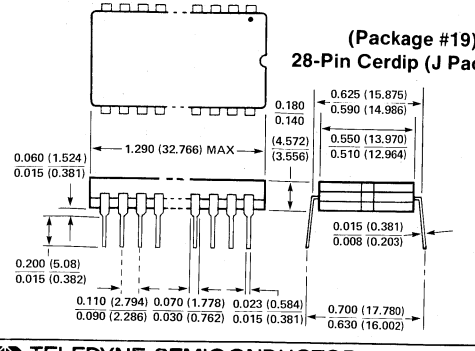
A negative voltage can be generated from the positive supply by using a hex inverter as a free running oscillator to drive a voltage doubler. The five inverters are paralleled to provide a low output impedance. Since the 4049 is a standard 4000 CMOS part, the circuit can be operated from 3 to 15 volts. The 10 μF capacitors were used in order to minimize output ripple at low V+ voltages. When higher input voltages (V+) are available the 10 μF capacitors can be lowered to 1 or 0.1 μF depending on the output loading. If this circuit generates more voltage than is needed, one half of the diodes and capacitors can be eliminated to reduce cost. The output voltage will then be one-half of that shown in the graph and is available on the negative side of the 10 μF capacitor connected to ground.

Package Outlines

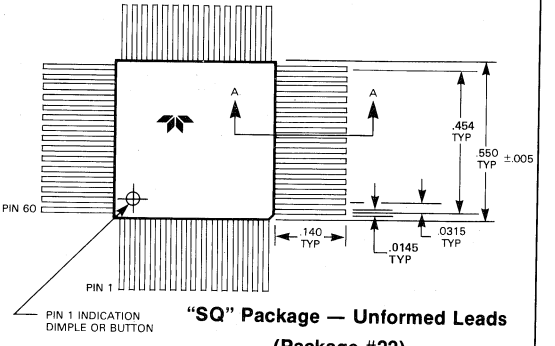
(Package #15)
28-Pin Plastic Dip (J Package)



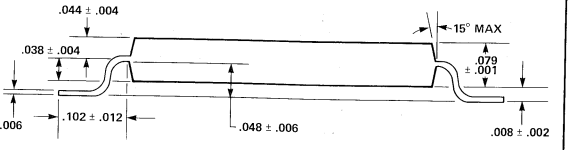
(Package #19)
28-Pin Cerdip (J Package)



60-Pin Flat Package



"SQ" Package — Unformed Leads
(Package #22)



"BQ" Package — Formed Leads
(Package #21)

TELEDYNE SEMICONDUCTOR

TSC8750
3 1/2 Digit ADC w/Parallel BCD Output
• 10 mS Conversion Time
• Latched Outputs

General Description

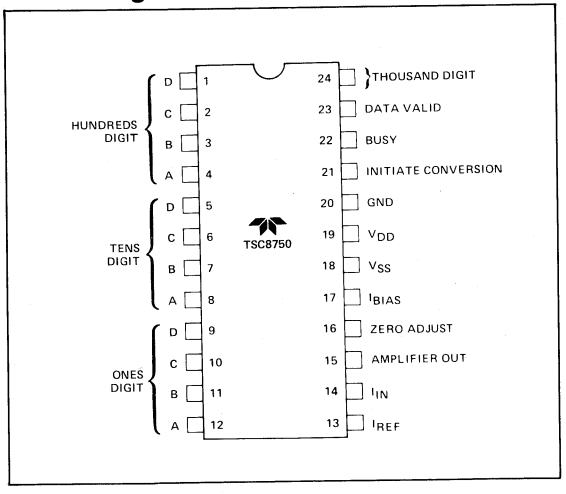
The Teledyne Semiconductor TSC8750 is a 3 1/2 digit monolithic CMOS analog-to-digital converter. Fully self-contained in a single 24-pin dual in-line package, the converter requires only passive support components, voltage or current reference and power supplies.

Conversion is performed by an incremental charge balancing technique which has inherently high accuracy, linearity and noise immunity. An amplifier integrates the sum of the unknown analog current and pulses of a reference current. The number of pulses (charge increments) needed to maintain the amplifier summing junction near zero are counted. At the end of conversion the total count is latched into the digital outputs in a 3 1/2 digit parallel BCD digital format.

Ordering Information

Part No.	Package	Temperature Range
TSC8750CJ	24-Pin Plastic Dip	0° C to +70° C
TSC8750CN	24-Pin Ceramic	-40° C to +85° C
TSC8750BN	24-Pin Ceramic	-55° C to +125° C
Devices with MIL-STD-883 Processing		
TSC8750BN/883	24-Pin Ceramic	-55° C to +125° C

Pin Configuration



Features

- High Accuracy — 3 1/2 Digit Resolution With < ±0.025% Error
- Military Temperature Range Devices
- Monotonic Performance — No Missing Codes
- Monolithic CMOS Construction Gives Low Power Dissipation — 20 mW Typical
- Contains All Required Active Elements — Needs only Passive Support Components, Reference Voltage and Dual Power Supply
- High Stability Over Full Temperature Range
  - — Gain Temperature Coefficient Typically <25 ppm/° C
  - — Zero Drift Typically <30 μV/° C
  - — Differential Non-Linearity Drift Typically <2.5 ppm/° C
- Latched Parallel BCD Outputs
- LPTTL and CMOS Compatible Outputs and Control Inputs
- Strobed or Free Running Conversion
- Infinite Input Range — Any Positive Voltage Can Be Applied Via a Scaling Resistor

Absolute Maximum Ratings

Storage Temperature ..... -65° C to + 150° C
Operating Temperature
BN ..... -55° C to + 125° C
CN ..... -40° C to + 85° C
CJ ..... 0° to + 70° C
V_{DD} -V_{SS} ..... 18 V
I_{IN} ..... ±10 mA
I_{REF} ..... ±10 mA
Digital Input Voltage ..... -0.3 to V_{DD} +0.3 V
Operating V_{DD} and V_{SS} Range ..... 3.5 V to 7 V
Package Dissipation ..... 500 mW
Lead Temperature ..... 300° C
(Soldering, 10 seconds)

HANDLING PRECAUTIONS
CMOS devices must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static tubes or other conductive material. Use proper anti-static handling procedures. Do not connect in circuits under "power on" conditions, as high transients may cause permanent damage.

Electrical Characteristics Unless otherwise specified, $V_{DD} = +5$ V, $V_{SS} = -5$ V, $V_{GND} = 0$, $V_{REF} = -6.4$ V, $R_{BIAS} = 100$ kΩ, test circuit shown. $T_A = 25°$ C unless Full Temperature Range is specified. (-55° C to +125° C for BN, -40° C to +85° C for CN package, 0° to 70° C for CJ package.)

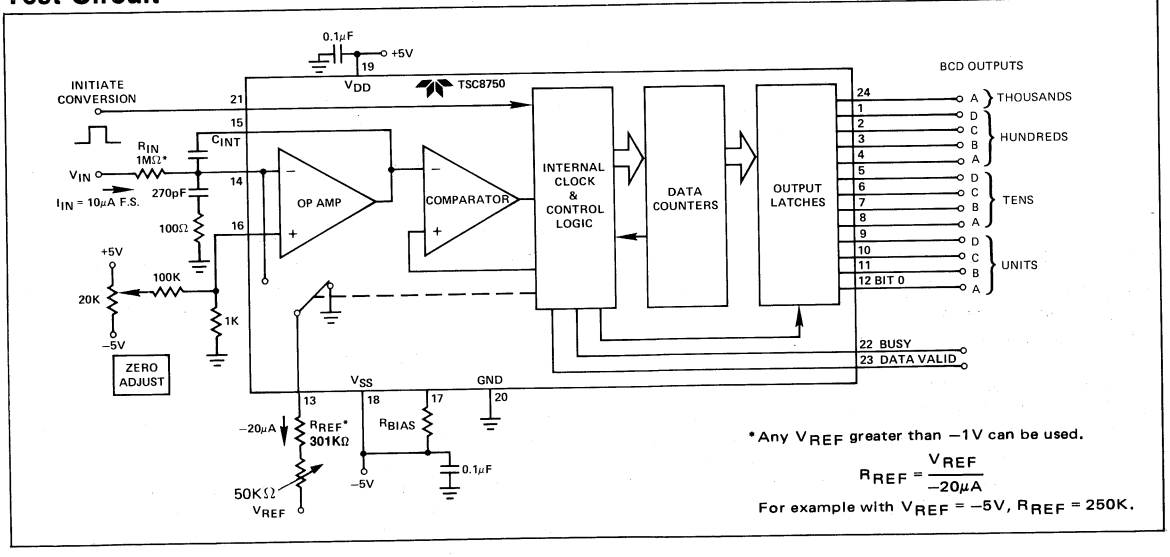
PARAMETER	DEFINITION	CONDITIONS	MIN	TYP	CJ/CL MAX	BL MAX	UNITS
Accuracy							
Resolution Accuracy	BCD Word Length Of Digital Output		3 1/2 (1999 Counts)	—	—	—	Digits
Relative Accuracy	Output Deviation From Straight Line Between Normalized Zero and Full-Scale Input		—	—	0.025	0.025	%
Differential Non-Linearity	Deviation From 1 LSB Between Transition Points		—	—	—	0.025	0.025%
Differential Non-Linearity Temperature Drift	Variation in Differential Non-Linearity Due To Temperature Change	Full Temperature Range	—	±2.5	±5	±5	ppm/° C
Gain Variance	Variation From Exact (Compensate By Trimming R_{IN} or R_{REF})		—	±2	±5	±5	% of Nominal
Gain Temperature Drift	Variation In A Due To Temperature Change	Full Temperature Range	—	±25	±75	±80	ppm/° C
Zero Offset	Correction at Zero Adjust to Give Zero Output When Input Is Zero	$I_{IN} = 0$	—	±10	±50	±50	mV
Zero Temperature Drift	Variation in Zero Offest Due to Temperature Change	Full Temperature Range	—	±3	±5	±8	ppm/° C
Analog Inputs							
I_{IN} Full-Scale	Full-Scale Analog Input Current To Achieve Specified Accuracy		—	10	—	—	μA
I_{REF} (Note 1)	Reference Current Input To Achieve Specified Accuracy		—	-20	—	—	μA
Digital Inputs							
$V_{IN}^{(1)}$	Logical "1" Input Threshold For Initiate Conversion Input	Full Temperature Range	3.5	—	—	—	V
$V_{IN}^{(0)}$	Logical "0" Input Threshold For Initiate Conversion Input	Full Temperature Range	—	—	1.5	1.5	V
Digital Outputs							
$V_{OUT}^{(1)}$	Logical "1" Output Voltage For Digits Out, Busy, and Data Valid Outputs	Full Temp. Range $I_{OUT} = -10$ μA $I_{OUT} = -500$ μA	4.5	—	—	—	V
$V_{OUT}^{(0)}$	Logical "0" Output Voltage For Digits Out, Busy, and Data Valid Outputs	Full Temp. Range $V_{DD} = 4.75$ V $I_{OUT} = 500$ μA	—	—	0.4	0.4	V
Dynamic							
Conversion Time	Time Required to Perform One Complete A/D Conversion	Full Temp. Range	—	10	12	12	ms
Conversion Rate in Free-Run Mode		$V_{INT\ CONV} = +5$ V	84	100	—	—	Conv'ns per Second
Minimum Pulse Width for Initiate Conversion		Full Temp. Range	500	—	—	—	ns

Electrical Characteristics Unless otherwise specified, V_{DD} = +5 V, V_{SS} = -5 V, V_{GND} = 0, V_{REF} = -6.4 V, R_{BIAS} = 100 kΩ, test circuit shown. T_A = 25° C unless Full Temperature Range is specified. (-55° C to +125° C for BN, -40° C to +85° C for CN package, 0° to 70° C for CJ package.)

PARAMETER	DEFINITION	CONDITIONS	MIN	TYP	CJ/CL MAX	BL MAX	UNITS
Supply Current							
I_{DD} Quiescent	Current Required From Positive Supply During Operation	Full Temp. Range	—	1.4	2.5	3.5	mA
(N Package)		$V_{INT\ CONV}$ = OV	—	1.4	5.0		mA
(J Package)							
I_{SS} Quiescent	Current Required From Negative Supply During Operation	Full Temp. Range	—	-1.6	-2.5	-3.5	mA
(N Package)		$V_{INIT\ CONV}$ = OV	—	-1.6	-5.0		mA
(J Package)							
Supply Sensitivity	Change in Full-Scale Gain vs Supply Voltage Change	V_{DD} ± 1V, V_{SS} ±1 V	—	±0.5	±1.0	±1.0	%/V
$\|V_{DD}\| = \|V_{SS}\|$ = 5 V ± 1 V	Change in Full-Scale Gain vs Supply Voltage Change for Tracking Supplies		±0.05	±0.1	±0.1	±0.1	%/V

NOTE:
I_{IN} and I_{REF} pins connect to the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors. See Test Circuit.

Test Circuit



Circuit Description

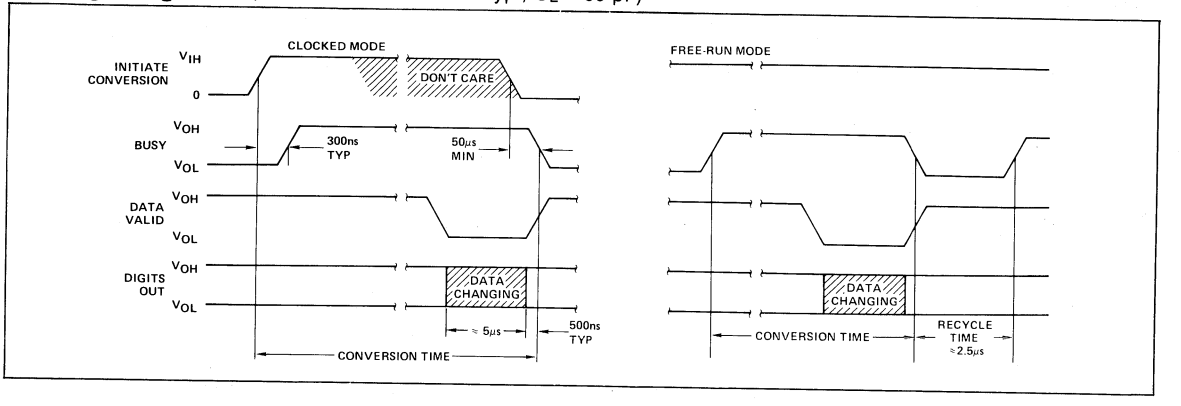
During conversion the sum of a continuous current I_{IN} and pulses of a reference current I_{REF} is integrated for a fixed number of clock periods. I_{IN} is proportional to the analog input voltage; I_{REF} is switched in for exactly one clock period just frequently enough to maintain the summing input of the integrator near zero. Thus, the charge from the continuous I_{IN} current is balanced against the pulses of I_{REF} current. The total number of I_{REF} pulses needed during the conversion period to maintain the charge balance is counted, and the result (in BCD) is latched into the outputs at the end of conversion.

The converter contains two counters and a clock in addition to an operational amplifier, comparator, latching output buffers and housekeeping logic. One counter is a clock counter which (after a reset pulse) starts counting clock pulses; when the required count is reached, the clock counter generates a pulse to start the end-of-conversion routine.

The other counter is a data counter, which is reset synchronously with the clock counter and counts the number of times the I_{REF} current is switched into the summing input of the amplifier during the period defined by the clock counter.

When the Initiate Conversion input is strobed with a positive signal, the busy line latches high and a 10 μs (times given are approximate) start up cycle begins. The integrating capacitor is discharged and both counters are reset during this start up period. Conversion begins at the end of the reset pulse and ends with a pulse generated either by the clock counter or by an overflow condition in the data counter. This pulse disables further inputs into both counters and triggers a 10 μs shutdown cycle. During the shutdown cycle Data Valid goes low for 5 μs. This binary sequence is shown in the timing diagrams. Busy is true high, and when the circuit is busy, Initiate conversion has no effect and may be high or low. Data Valid is also true high. The data from a conversion remain valid for as long as power is applied to the circuit or until Data Valid falls at the end of a subsequent conversion, at which time the output data are updated to reflect the latest conversion.

Timing Diagrams (Rise, fall times = 200 ns typ., C_L = 50 pF)



Pin Functions

Initiate Conversion Input

Accepts CMOS and most 5 V logic inputs. Applying a logic "1" to the Initiate Conversion pin initiates the A/D conversion cycle. Once conversion has been initiated, the cycle cannot be interrupted, and the Initiate Conversion pin is disabled until conversion is complete. Two modes of operation are permitted, clocked or free-running. For clocked operation the Initiate Conversion input is held at logic "0" for standby and taken to logic "1" when a conversion is desired. For free-running operation the Initiate Conversion pin is connected to V_{DD} or similar permanent logic "1" voltage.

Busy Output

A digital status output which is compatible with CMOS logic and low power TTL (can sink and source 500 μA). A logic "1" output on the Busy pin indicates a conversion cycle is in process. A logic "1" to logic "0" transition indicates that conversion is complete and the result has been latched at the Digits Out pins. A logic "0" to logic "1" transition indicates a new conversion cycle has been initiated. If the device is operating in the free-running mode, the Busy output will remain low for approximately 2.5 μs, marking the completion and initiation of consecutive conversion cycles.

Data Valid Output

A digital status which is compatible with CMOS logic and low power TTL (can sink and source 50 μA). A logic "1" output at the Data Valid pin indicates that the Digits Out pins are latched with the result of the last conversion cycle. The Data Valid output goes to logic "0" approximately 5 μs before the completion of a conversion cycle. During this 5 μs interval new data is being transferred to the Digits Out pins, and the Digits Out are not valid.

Digits Out

(ones, tens, hundreds and thousand)

The BCD digit outputs which are the result of the A/D conversion. These outputs are CMOS logic and low power TTL compatible.

Applications Information

Input/Output Relationships

The analog input voltage (V_{IN}) is related to the output by the transfer equation:

$$\text{Digital Counts} = \frac{V_{IN} \cdot A \cdot R_{REF}}{R_{IN} \cdot V_{REF}}$$

$$A = 4128$$

where Digital Counts is the value of the BCD output word presented at Digits Out pins in response to V_{IN}.

The digital output code format is as follows:

Analog Input	Digital Output
$V_{IN} \leq$ Full-Scale	1100110011001
= Full-Scale -1 LSB	1100110011001
= 1 LSB	0 . . . 000 . . . 1
≤ 0	0 . . . 000 . . . 0

External Component Selection

Obtaining a high accuraccy conversion system depends on the voltage regulation of V_{REF} and the thermal stability of R_{IN} and R_{REF}. The exact dependence is given by the transfer function. System accuracy also depends, to a lesser degree, on the voltage regulation of V_{DD} and V_{SS}. The supply connections V_{DD} and V_{SS} should have bypass capacitors of value 0.1 μF or larger right at the device pins.

R_{IN}, R_{EF}

Values of these components are chosen to give a full-scale input current of approximately 10 μA and a reference current of approximately -20 μA.

$$R_{IN} \cong \frac{V_{IN}\ \text{Full-Scale}}{10\ \mu A} \qquad R_{REF} \cong \frac{V_{REF}}{-20\ \mu A}$$

Examples:

$$R_{IN} \cong \frac{10\ V}{10\ \mu A} = 1\ M\Omega \qquad R_{REF} \cong \frac{-6.4\ V}{-20\ \mu A} = 320\ k\Omega$$

Note that these values are approximations, and the exact relationships are defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed using the optional gain adjust circuit to obtain full-scale output at V_{IN} Full-Scale (see adjustment procedure). Metal film resistors with 1% tolerance or better are recommended for high accuracy applications because of their thermal stability and low noise generation.

R_{BIAS}

Specifications for the TSC8750 are based on $R_{BIAS} = 100\ k\Omega$ $\pm 10\%$ unless otherwise noted. However, there are instances when the designer may want to change this resistor in order to affect the conversion time and the supply current. By decreasing R_{BIAS} the A/D will convert much faster and the supply current will be higher. (For example: When R_{BIAS} is 20 k the conversion time is reduced by 1/3, and the supply current will increase from 2 mA to 7 mA.) Likewise, if the R_{BIAS} is increased the conversion time will be longer and the supply current will be much lower. (For example: When R_{BIAS} = 1 mΩ the conversion time will be six times longer, and the supply current is now reduced to .5 mA). For details of this relationship refer to AN-9 typical performance curves.

R_{DAMP}

Exact value not critical but should have a nominal value of 100 Ω $\pm 10\%$. Locate close to pin 14.

C_{DAMP}

Exact value not critical but should have a nominal value of 270 pF $\pm 20\%$. Locate close to pin 14.

C_{INT}

Exact value not critical but should have a nominal value of 68 pF $\pm 10\%$. Low leakage types are recommended, although mica or ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 14, 15.

V_{REF}

A negative reference voltage must be supplied. This may be obtained from a constant current source circuit or from the negative supply.

V_{DD}, V_{SS}

Power supplies of ± 5 V are recommended, with 0.05% line and load regulation and 0.1 μF decoupling capacitors.

Adjustment Procedure

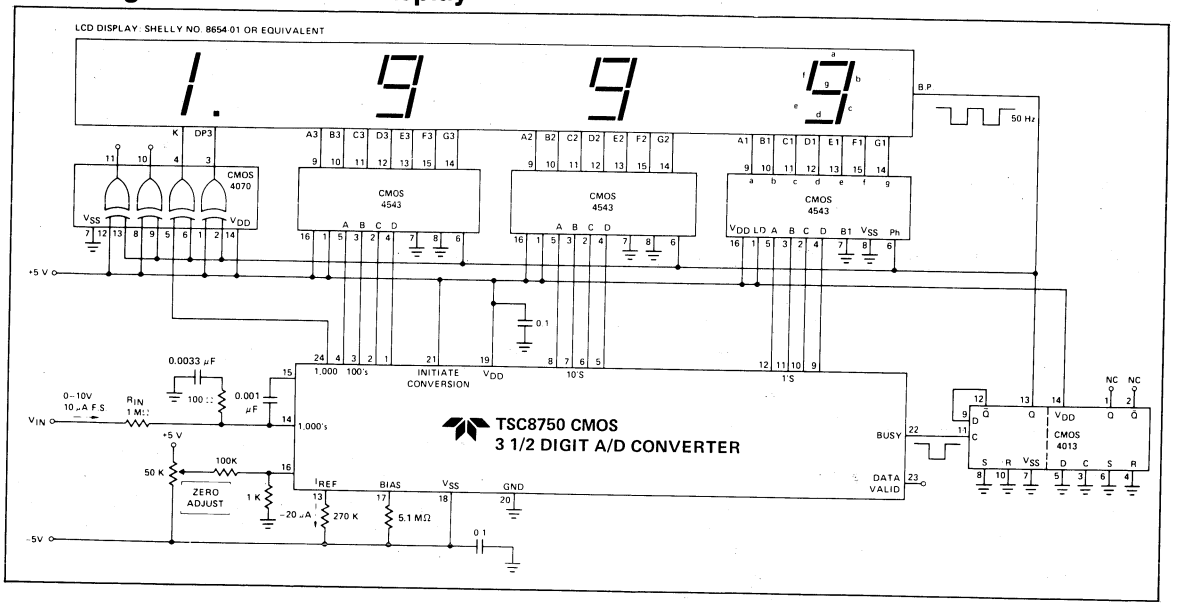
The test circuit diagram shows optional circuits for trimming the zero location and full-scale gain. Because the digital outputs remain constant outside of the normal operating range (i.e. below zero and above full-scale), it is recommended that transition points be used in setting the zero and full-scale values. Recommended procedure is as follows:

- Set the initiate conversion control high to provide free-run operation and verify that converter is operating.
- Set V_{IN} to +1/2 LSB and trim the zero adjust circuit to obtain a 000 . . . 000 . . . to 000 . . . 001 transition. This will correctly locate the zero end.
- For full-scale adjustment, set V_{IN} to the full-scale value less 1 1/2 LSB and trim the gain adjust circuit for a 1100110011000 to 1100110011001 transition.

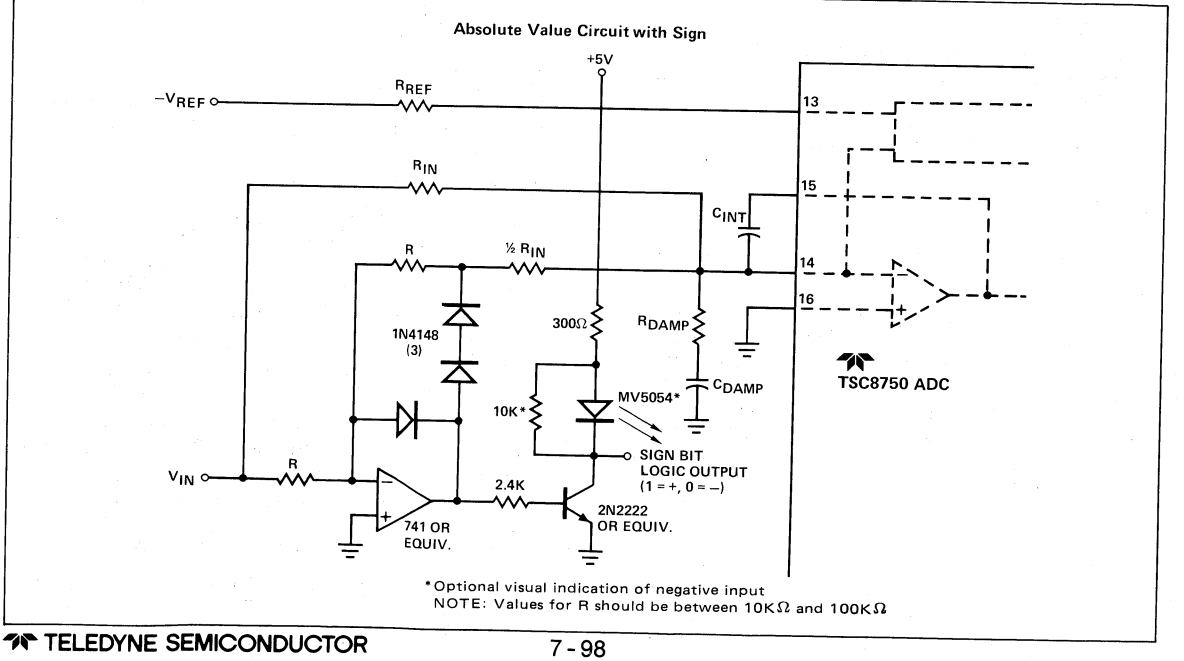
If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

Application/Design Circuits

3 1/2 Digit A/D with LCD Display



Bipolar Operation (+ and - inputs)

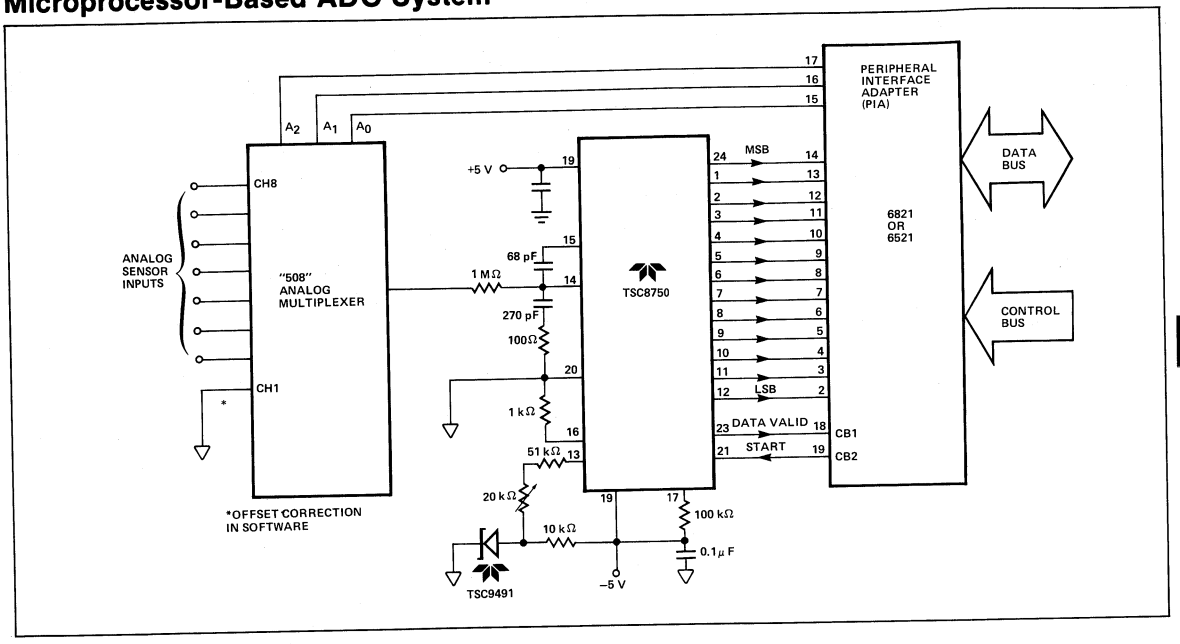


3 1/2 Digit ADC w/Parallel BCD Output

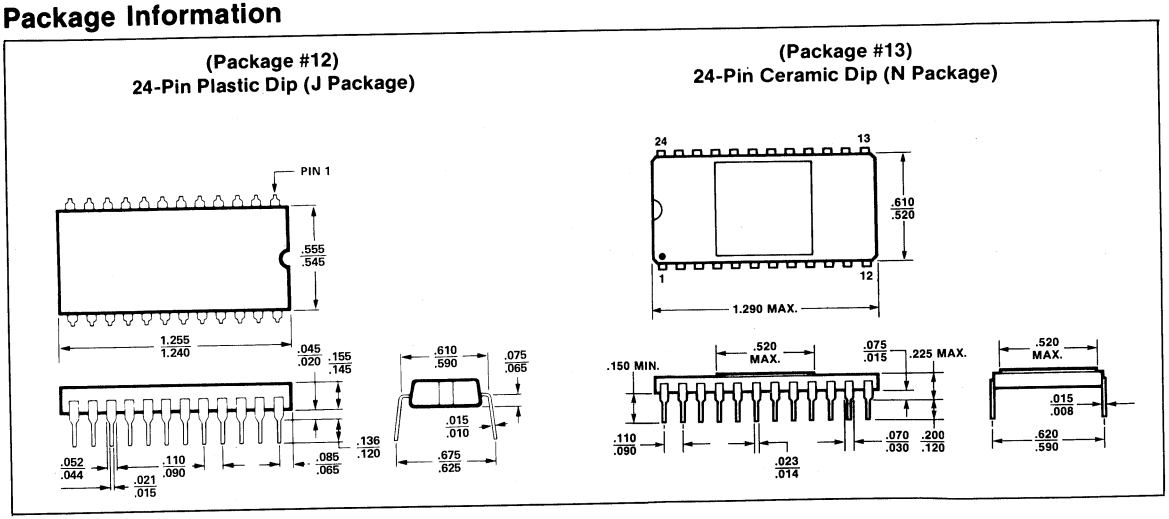
- 10 mS Conversion Time
- Latched Outputs

TSC8750

Microprocessor-Based ADC System



Package Information



TSC14433A
3 1/2 Digit ADC
• ±1 Count Rollover Error
• Low Power

General Description

The TSC14433A is a monolithic CMOS 3 1/2 digit A/D converter which features improved performance over the industry standard TSC14433. Rollover, which is the measurement of an idencital positive and negative signal is guaranteed to have the same reading within one count. The output drive current is increased and is fully compatible to drive TTL loads and conforms to standard B-Series CMOS. The power consumption at 4 mW is approximately one-half of the TSC14433. The TSC14433A combines both analog and digital circuits on a single IC, thus minimizing the number of external components. This dual slope A/D converter provides automatic polarity and zero correction with the addition of two external resistors and two capacitors. The full-scale voltage range of this ratiometric IC extends from 199.9 millivolts to 1.999 volts. The TSC14433A can operate over a wide range of power supply voltages including batteries and standard 5 volt supplies.

HANDLING PRECAUTIONS: These devices are CMOS and must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static handling procedures. Do not connect in circuits under "power on" conditions, as high transients may cause permanent damage.

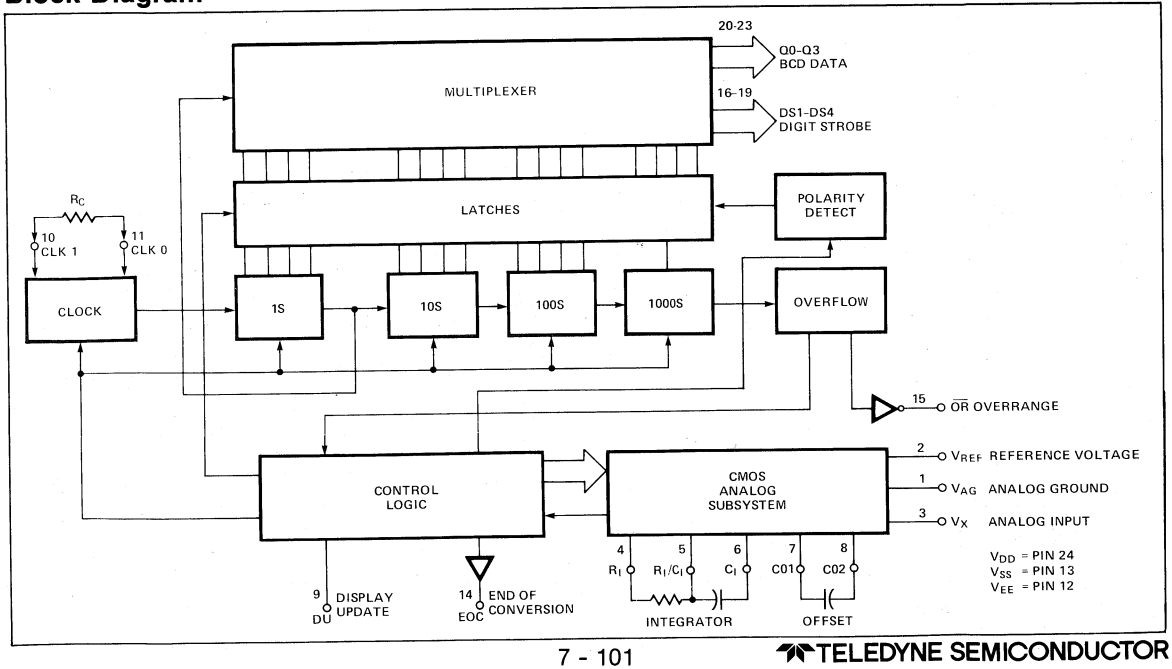
Features

- Rollover: ± 1 Count
- Standard B-Series CMOS Outputs — Drives One Standard TTL Load
- Low Power Consumption: 4 mW Typical @ ±5.0 V
- Overrange and Underrange Signals Available
- Operates in Auto Ranging Circuits
- Accuracy: ±0.05% of Reading ±1 Count
- Two Voltage Ranges: 1.999 V and 199.9 mV
- Up to 25 Conversions Per Second
- Z_{IN} > 1000 M Ohm
- Auto-Polarity and Auto-Zero
- Single Positive Voltage Reference
- Uses On-chip System Clock or External Clock
- Wide Supply Range: e.g., ±4.5 V to ±8.0 V
- Operates With LED and LCD Displays
- Low External Component Count

Applications

- Portable Instruments
- Multimeters
- Digital Voltmeters
- Digital Panel Meters
- Digital Scales
- Digital Thermometers
- Remote A/D Sensing Systems
- MPU Systems

Block Diagram



Absolute Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
DC Supply Voltage	V_{DD} to V_{EE}	-0.5 to +18 Vdc	Vdc
Voltage, Any Pin, Referenced V_{EE}	V	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain Per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C

Recommended Operating Conditions

(V_{SS} = 0 or V_{EE})

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage —			
V_{DD} to Analog Ground	V_{DD}	+5.0 to +8.0	Vdc
V_{EE} to Analog Ground	V_{EE}	-2.8 to -8.0	
Clock Frequency	f_{CLK}	32 to 400	kHz
Zero Offset Correction Capacitor	C_O	0.1 ±20%	μF

Note: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{EE} \le (V_{IN}$ or $V_{OUT}) \le V_{DD}$.

Electrical Characteristics:

(C_I = 0.1 μF mylar, R_I = 470 kΩ @ V_{REF} = 2.000 V, R_I = 27 kΩ @ V_{REF} = 200.0 mV. C_O = 0.1 μF, R_C = 300 kΩ; all voltages referenced to Analog Ground, pin 1.)

CHARACTERISTIC	SYMBOL	V_{DD} Vdc	V_{EE} Vdc	-40°C MIN	-40°C MAX	25°C MIN	25°C TYP	25°C MAX	85°C MIN	85°C MAX	UNIT
Rollover Error (Difference in reading for equal positive and negative reading near Full-Scale) $-V_{IN} = +V_{IN}$: 200 mV Full-Scale	—			—	—	-1	—	+1	—	—	Cnts
Output Current — Pins 14 to 23 (V_{SS} = 0V)											
(V_{OH} = 4.6 V) Source	I_{OH}	5.0	-5.0	-0.25	—	-0.2	-0.36	—	-0.16	—	mA
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	-5.0	1.6	—	1.6	3.2	—	1.6	—	mA
(V_{SS} = -5.0 V)											
(V_{OH} = 4.5 V) Source	I_{OH}	5.0	-5.0	-0.62	—	-0.5	-0.9	—	-0.35	—	mA
(V_{OL} = -4.5 V) Sink	I_{OL}	5.0	-5.0	1.6	—	1.6	5.50	—	1.6	—	mA
Linearity Output Reading (Note 1)	—										
(V_{REF} = 2.000 V)		5.0	-5.0	—	—	-0.05	+0.05	+0.05	—	—	%rdg
(V_{REF} = 200.0 mV)		5.0	-5.0	—	—	-1 count		+1 count	—	—	
Stability Output Reading (Note 2)	—										
(V_X = 1.990 V, V_{REF} = 2.000 V)		5.0	-5.0	—	—	—	—	2	—	—	LSD
(V_X = 199.0 mV, V_{REF} = 200.0 mV)		5.0	-5.0	—	—	—	—	3	—	—	LSD
Zero Output Reading (V_X = 0 V, V_{REF} = 2.000 V)	—	5.0	-5.0	—	—	—	0	0	—	—	LSD
Bias Current —											
Analog Input	—	5.0	-5.0	—	—	—	± 20	± 100	—	—	pA
Reference Input		5.0	-5.0	—	—	—	± 20	± 100	—	—	pA
Analog Ground		5.0	-5.0	—	—	—	± 20	± 500	—	—	pA
Common-Mode Rejection (V_X = 1.4 V, V_{REF} = 2.000 V, f_{OC} = 32 kHz)		5.0	-5.0	—	—	—	65	—	—	—	dB
Output Voltage — Pins 14 to 23											
(V_{SS} = 0 V) "0" Level	V_{OL}	5.0	-5.0	—	0.05	—	0	0.05	—	0.05	V
"1" Level	V_{OH}	5.0	-5.0	4.95	—	4.95	5.0	—	4.95	—	V
(V_{SS} = -5.0 V) "0" Level	V_{OL}	5.0	-5.0	—	-4.95	—	-5.0	-4.95	—	-4.95	V
"1" Level	V_{OH}	5.0	-5.0	4.95	—	4.95	5.0	—	4.95	—	V
Clock Frequency (R_C = 300 kΩ)	f_{CLK}	5.0	-5.0	—	—	—	66	—	—	—	kHz
Input Current — DU	I_{DU}	5.0	-5.0	—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Quiescent Current	I_Q	5.0	-5.0	—	3.7	—	0.4	2.0	—	1.6	mA
(V_{DD} to V_{EE}, I_{SS} = 0)		8.0	-8.0	—	7.4	—	1.4	4.0	—	3.2	mA
Supply Rejection (V_{DD} to V_{EE}, I_{SS} = 0, V_{REF} = 2.000 V)	—	5.0	-5.0	—	—	—	0.5	—	—	—	mV/V

Note:

1. Accuracy — The accuracy of the meter at full-scale is the accuracy of the setting of the reference voltage. Zero is recalculated during each conversion cycle. The meaningful specification is linearity. In other words, the deviation from correct reading for all inputs other than positive full-scale and zero is defined as the linearity specification.
2. Three LSD stability for 200 mV scale is defined as the range that the LSD will occupy 95% of the time.
3. Pin numbers refer to 24-Pin DIP.

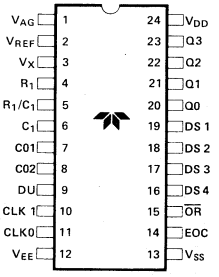
Pin Description

PIN NO. 60-Pin FP	PIN NO. 24-Pin DIP	SYMBOL	DESCRIPTION
7	1	V_{AG}	This is the Analog Ground. It has a high input impedance. This pin determines the reference level for the unknown input voltage (V_X) and the reference voltage (V_{REF}).
10	2	V_{REF}	Reference voltage. Full-scale output is equal to the voltage applied to V_{REF}. Therefore, full-scale voltage of 1.999 V requires 2.000 V reference and 199.9 mV full-scale requires a 200 mV reference. V_{REF} functions as system reset, also. When switched to V_{EE} the system is reset to the beginning of the conversion cycle.
12	3	V_X	The Unknown Input Voltage (V_X) is measured as a ratio of the reference voltage (V_{REF}) in a ratio-metric A/D conversion.
19 22 24	4 5 6	R_1 R_1/C_1 C_1	These pins are for external components used for the integration function in the dual slope conversion. Typical values are 0.1 μF (mylar) capacitor for C_1. R_1 = 470 kΩ (resistor) for 2.0 V full-scale. R_1 = 27 kΩ (resistor) for 200 mV full-scale. Clock frequency of 66 kHz gives 250 ms conversion time. See equation below for calculation of integrator component values.
25 26	7 8	$C0_1$ $C0_2$	These pins are used for connecting the offset correction capacitor. The recommended value is 0.1 μF.
27	9	DU	Display Update input pin. When DU is connected to the EOC output every conversion is displayed. New data will be strobed into the output latches during the conversion cycle if a positive edge is received on DU prior to the ramp-down cycle. When this pin is driven from an external source, the voltage should be referenced to V_{SS}.
34 36	10 11	CLK_1 CLK_0	Clock input pins. The TSC14433 has its own oscillator system clock. Connecting a single resistor between CLK_1 and CLK_0 sets the clock frequency. A crystal or LC circuit may be inserted in lieu of a resistor for improved stability. CLK_1, the clock input, can be driven from an external clock source, which need only have standard CMOS output drive. This pin is referenced to V_{EE} for external clock inputs. A 300 kΩ resistor yields a clock frequency of about 66 kHz. (See typical characteristic curves). (See Figure 9 for alternate circuits).
37	12	V_{EE}	Negative Power Supply. Connection pin for the most negative supply. Please note the current for the output drive circuit is returned through V_{SS}. Typical supply current is 0.8 mA.
39	13	V_{SS}	Negative Power Supply for Output Circuitry. This pin sets the low voltage level for the output pins (BCD, Digit Selects, EOC, OR). When connected to analog ground, the output voltage is from analog ground to V_{DD}. If connected to V_{EE}, the output swing is from V_{EE} to V_{DD}. The recommended operating range for V_{SS} is between V_{DD} -3.0 volts and V_{EE}.
40	14	EOC	End of Conversion output generates a pulse at the end of each conversion cycle. This generated pulse width is equal to one half the period of the system clock.
41	15	OR	Overrange pin. Normally this pin is set high. When V_X exceeds V_{REF} the OR pin is low.
49 51 52 54	16 17 18 19	DS_4 DS_3 DS_2 DS_1	Digit Select pins. The digit select output goes high when the respective digit is selected. The MSD (1/2 digit) turns on immediately after an EOC pulse. The remaining digits turn on in sequence from MSD to LSD. To ensure that the BCD data has settled, an inter-digit blanking time of two clock periods is included. Clock frequency divided by 80 equals multiplex rate. For example a system clock of 66 kHz gives a multiplex rate of 0.8 kHz.
5 4 57 55	20 21 22 23	Q_3 Q_2 Q_1 Q_0	See Figure 12 for Digit Select Timing Diagram. BCD Data Output pins. Multiplexed BCD outputs contain 3 full digits of information during digit select DS2, 3, 4. During DS1, the 1/2 digit, overrange, underrange and polarity information is available. Refer to Truth Table.
6	24	V_{DD}	Positive Power Supply. This is the most positive power supply pin.

Ordering Information

Part No.	Package	Temperature Range
TSC14433ACJ	24-Pin Plastic Dip	-40° C to +85° C
TSC14433ACL	24-Pin CerDIP	-40° C to +85° C
TSC14433ACBQ	60-Pin Plastic Flat Package: Formed Leads	-40° C to +85° C
TSC14433ACSQ	60-Pin Plastic Flat Package: Unformed Leads	-40° C to +85° C
Devices with 160 Hour, +125° C Burn-In		
TSC14433ACJ/BI	24-Pin Plastic Dip	-40° C to +85° C
TSC14433ACL/BI	24-Pin CerDIP	-40° C to +85° C

Pin Configuration

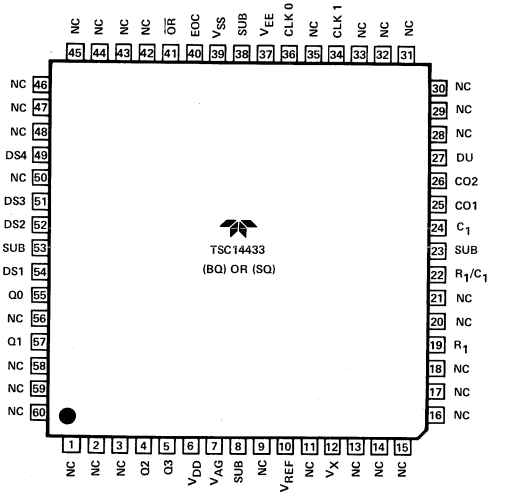


$$R_1 = \frac{V_X(max)}{C_1} \times \frac{T}{\Delta V}$$

$$\Delta V = V_{DD} - V_X \text{ (max)} - 0.5$$

$$T = 4000 \times \frac{1}{f_{CLK}}$$

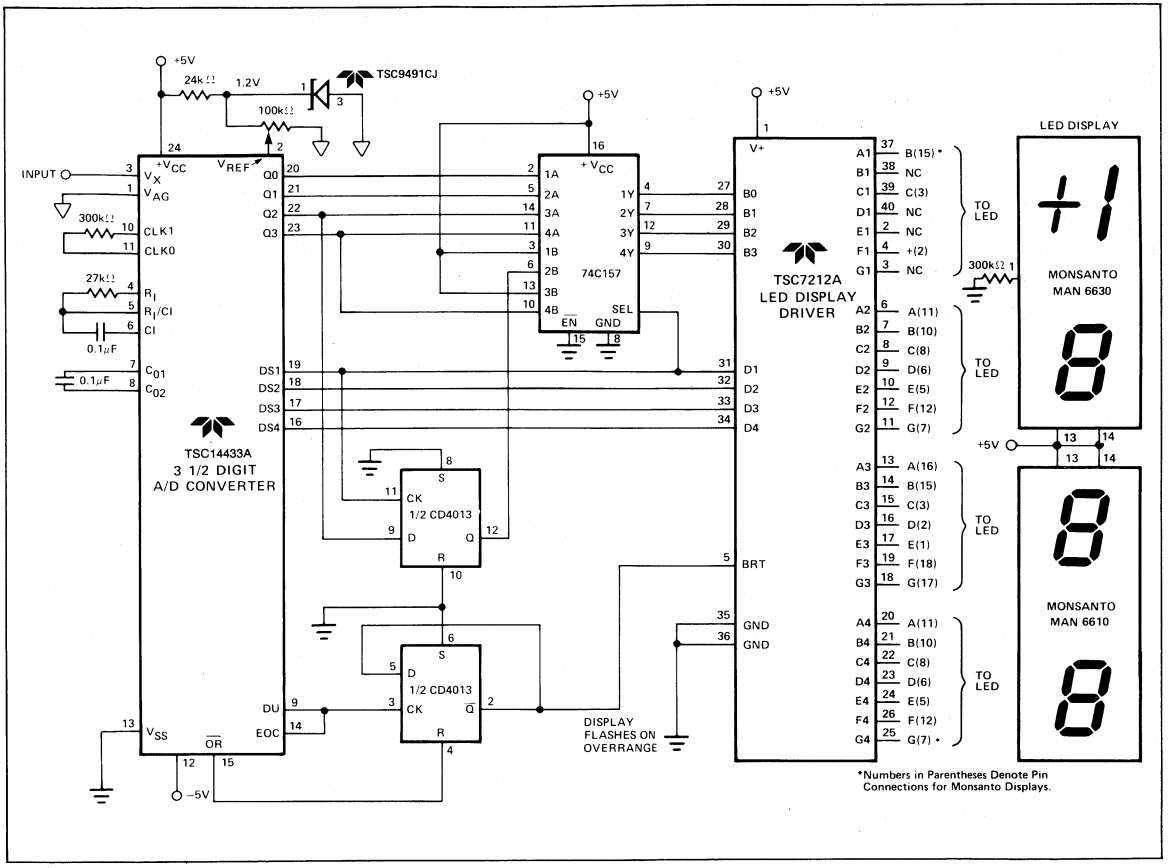
Where
R_1 is in kΩ
V_{DD} is the voltage at pin 24 referenced to V_{AG}
V_X is the voltage at pin 3 referenced to V_{AG}
f_{CLK} is the clock frequency at pin 10 in kHz



NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V^+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

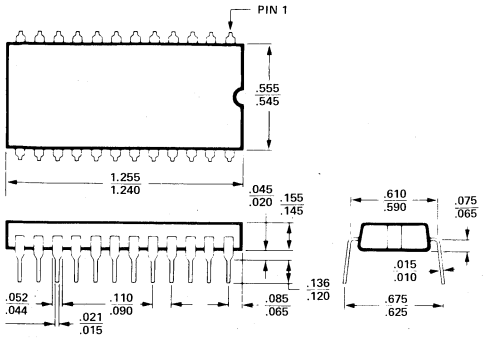
Typical Applications

TSC7212A Interface to TSC14433A 3 1/2 Digit ADC.

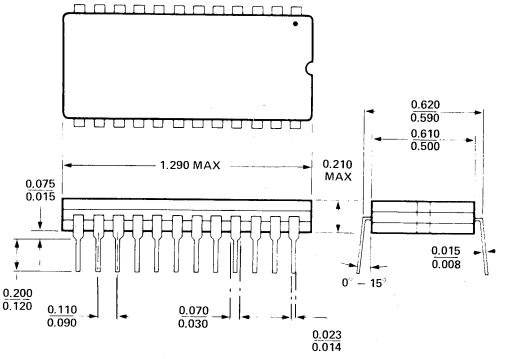


Package Information

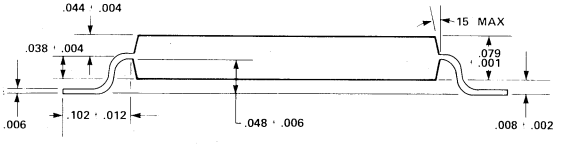
24-Pin Plastic Dip (J)
(Package #12)



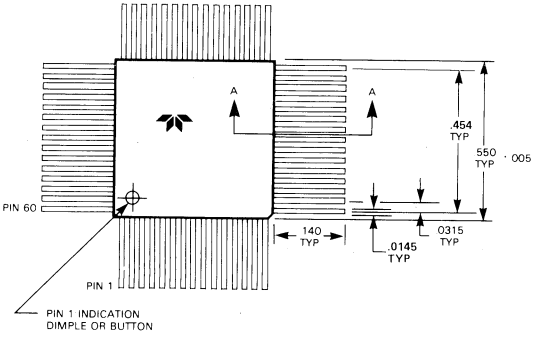
24-Pin CerDIP (L)
(Package #14)



60-Pin Flat Package
(Package #21)



60-Pin Flat Package
(Package #22)



TELEDYNE SEMICONDUCTOR

TSC14433B
3 1/2 Digit ADC
• Low Cost
• Multiplexed BCD Data
• ±4 Count Rollover Error

General Description

The TSC14433B is a monolithic CMOS 3 1/2 digit A/D converter. This low cost electrical version is ideal in systems where optimum rollover performance is not required. The TSC14433B combines both analog and digital circuits on a single IC, thus minimizing the number of external components. This dual slope A/D converter provides automatic polarity and zero correction with the addition of two external resistors and two capacitors. The full scale voltage range of this ratiometric IC extends from 199.9 millivolts to 1.999 volts. The TSC14433B can operate over a wide range of power supply voltages including batteries and standard 5 volt supplies.

HANDLING PRECAUTIONS: These devices are CMOS and must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static handling procedures. Do not connect in circuits under "power on" conditions, as high transients may cause permanent damage.

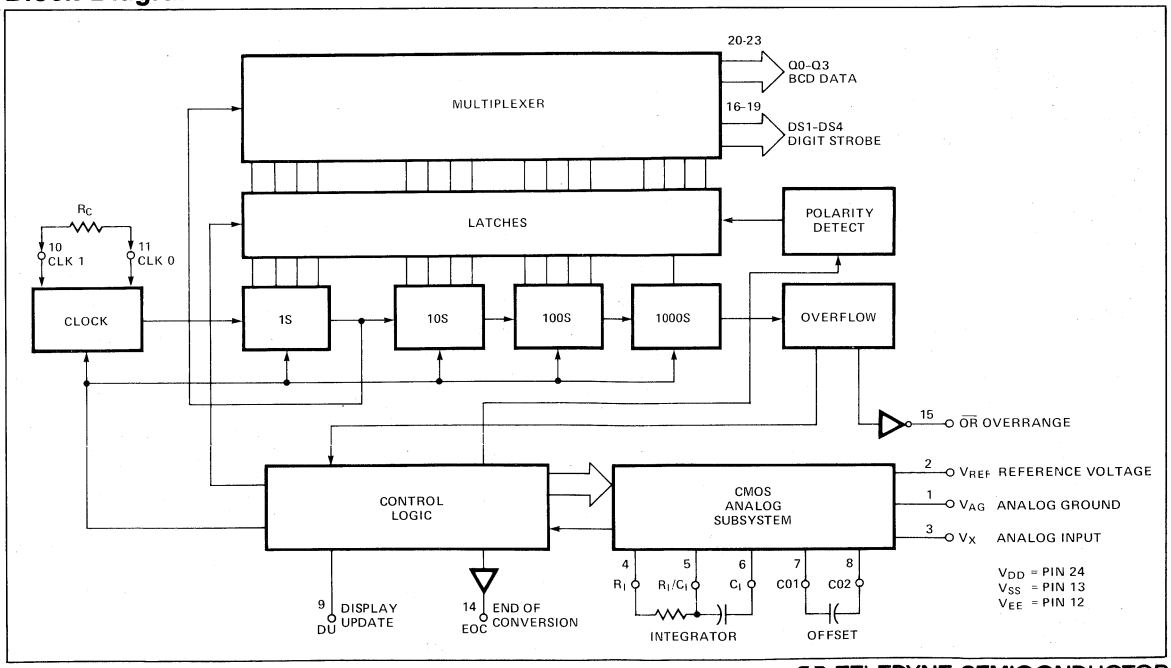
Features

- Low Cost
- Available in Compact Flat Package
- Rollover: ± 4 Count
- Low Power Consumption: 4 mW Typical @ ± 5.0 V
- Overrange and Underrange Signals Available
- Operates in Auto Ranging Circuits
- Accuracy: ± 0.05% of Reading ± 1 Count
- Two Voltage Ranges: 1.999 V and 199.9 mV
- Up to 25 Conversions Per Second
- Z_{IN} > 1000 M Ohm
- Auto-Polarity and Auto-Zero
- Uses On-chip System Clock or External Clock
- Wide Supply Range: e.g., ± 4.5 V to ± 8.0 V
- Operates With LED, LCD, Vacuum Fluorescent Displays

Applications

- Portable Instruments
- Multimeters
- Digital Voltmeters
- Digital Panel Meters
- Digital Scales
- Digital Thermometers
- Remote A/D Sensing Systems
- MPU Systems

Block Diagram



TSC14433B

3 1/2 Digit CMOS
- Low Cost
- Multiplexed BCD Data
- ±4 Count Rollover Error

Absolute Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
DC Supply Voltage	V_{DD} to V_{EE}	-0.5 to +18 Vdc	Vdc
Voltage, Any Pin, Referenced V_{EE}	V	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain Per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C

Recommended Operating Conditions

(V_{SS} = 0 or V_{EE})

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage — V_{DD} to Analog Ground	V_{DD}	+5.0 to +8.0	Vdc
V_{EE} to Analog Ground	V_{EE}	-2.8 to -8.0	
Clock Frequency	f_{CLK}	32 to 400	kHz
Zero Offset Correction Capacitor	C_O	0.1 ±20%	µF

Note: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{EE} \le (V_{IN}$ or $V_{OUT}) \le V_{DD}$.

Electrical Characteristics:

(C_I = 0.1 µF mylar, R_I = 470 kΩ @ V_{REF} = 2.000 V, R_I = 27 kΩ @ V_{REF} = 200.0 mV. C_O = 0.1 µF, R_C = 300 kΩ; all voltages referenced to Analog Ground, pin 1.)

		V_{DD}	V_{EE}	-40°C		25°C			85°C		
CHARACTERISTIC	SYMBOL	Vdc	Vdc	MIN	MAX	MIN	TYP	MAX	MIN	MAX	UNIT
Rollover Error (Difference in reading for equal positive and negative reading near Full-Scale) $-V_{IN} = +V_{IN}$: 200 mV Full-Scale	—			—	—	-4	—	+4	—	—	counts
Output Current — Pins 14 to 23 (V_{SS} = 0V)											
(V_{OH} = 4.6 V) Source	I_{OH}	5.0	-5.0	-0.25	—	-0.2	-0.36	—	-0.16	—	mA
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	-5.0	0.64	—	0.51	0.88	—	0.36	—	mA
(V_{SS} = -5.0 V)											
(V_{OH} = 4.5 V) Source	I_{OH}	5.0	-5.0	-0.52	—	-0.5	-0.9	—	-0.35	—	mA
(V_{OL} = -4.5 V) Sink	I_{OL}	5.0	-5.0	1.3	—	1.3	2.25	—	0.9	—	mA
Linearity Output Reading (Note 1)											
(V_{REF} = 2.000 V)	—	5.0	-5.0	—	—	-0.05-		+0.05+	—	—	%rdg
(V_{REF} = 200.0 mV)		5.0	-5.0	—	—	1 cnt	±0.05	1 cnt	—	—	%rdg
Stability Output Reading (Note 2)											
(V_X = 1.990 V, V_{REF} = 2.000 V)		5.0	-5.0	—	—	—	—	2	—	—	LSD
(V_X = 199.0 mV, V_{REF} = 200.0 mV)	—	5.0	-5.0	—	—	—	—	3	—	—	LSD
Zero Output Reading (V_X = 0 V, V_{REF} = 2.000 V)	—	5.0	-5.0	—	—	—	0	0	—	—	LSD
Bias Current —											
Analog Input	—	5.0	-5.0	—	—	—	± 20	± 100	—	—	pA
Reference Input		5.0	-5.0	—	—	—	± 20	± 100	—	—	pA
Analog Ground		5.0	-5.0	—	—	—	± 20	± 500	—	—	pA
Common-Mode Rejection (V_X = 1.4 V, V_{REF} = 2.000 V, f_{OC} = 32 kHz)		5.0	-5.0	—	—	—	65	—	—	—	dB
Output Voltage — Pins 14 to 23											
(V_{SS} = 0 V) "0" Level	V_{OL}	5.0	-5.0	—	0.05	—	0	0.05	—	0.05	V
"1" Level	V_{OH}	5.0	-5.0	4.95	—	4.95	5.0	—	4.95	—	V
(V_{SS} = -5.0 V) "0" Level	V_{OL}	5.0	-5.0	—	-4.95	—	-5.0	-4.95	—	-4.95	V
"1" Level	V_{OH}	5.0	-5.0	4.95	—	4.95	5.0	—	4.95	—	V
Clock Frequency (R_C = 300 kΩ)	f_{CLK}	5.0	-5.0	—	—	—	66	—	—	—	kHz
Input Current — DU	I_{DU}	5.0	-5.0	—	±0.3	—	±0.00001	±0.3	—	±1.0	µA
Quiescent Current (V_{DD} to V_{EE}, I_{SS} = 0)	I_Q	5.0	-5.0	—	3.7	—	0.4	2.0	—	1.6	mA
		8.0	-8.0	—	7.4	—	1.4	4.0	—	3.2	mA
Supply Rejection (V_{DD} to V_{EE}, I_{SS} = 0, V_{REF} = 2.000 V)	—	5.0	-5.0	—	—	—	0.5	—	—	—	mV/V

Note:
1. Accuracy — The accuracy of the meter at full-scale is the accuracy of the setting of the reference voltage. Zero is recalculated during each conversion cycle. The meaningful specification is linearity. In other words, the deviation from correct reading for all inputs other than positive full-scale and zero is defined as the linearity specification.
2. Three LSD stability for 200 mV scale is defined as the range that the LSD will occupy 95% of the time.

Pin Description

PIN NO. 60-Pin FP	PIN NO. 24-Pin DIP	SYMBOL	DESCRIPTION
7	1	V_{AG}	This is the Analog Ground. It has a high input impedance. This pin determines the reference level for the unknown input voltage (V_X) and the reference voltage (V_{REF}).
10	2	V_{REF}	Reference voltage. Full-scale output is equal to the voltage applied to V_{REF}. Therefore, full-scale voltage of 1.999 V requires 2.000 V reference and 199.9 mV full-scale requires a 200 mV reference. V_{REF} functions as system reset, also. When switched to V_{EE} the system is reset to the beginning of the conversion cycle.
12	3	V_X	The Unknown Input Voltage (V_X) is measured as a ratio of the reference voltage (V_{REF}) in a ratio-metric A/D conversion.
19 22 24	4 5 6	R_1 R_1/C_1 C_1	These pins are for external components used for the integration function in the dual slope conversion. Typical values are 0.1 μF (mylar) capacitor for C_1. R_1 = 470 kΩ (resistor) for 2.0 V full-scale. R_1 = 27 kΩ (resistor) for 200 mV full-scale. Clock frequency of 66 kHz gives 250 ms conversion time. See equation below for calculation of integrator component values.
25 26	7 8	C_{01} C_{02}	These pins are used for connecting the offset correction capacitor. The recommended value is 0.1 μF.
27	9	DU	Display Update input pin. When DU is connected to the EOC output every conversion is displayed. New data will be strobed into the output latches during the conversion cycle if a positive edge is received on DU prior to the ramp-down cycle. When this pin is driven from an external source, the voltage should be referenced to V_{SS}.
34 36	10 11	CLK_1 CLK_0	Clock input pins. The TSC14433 has its own oscillator system clock. Connecting a single resistor between CLK_1 and CLK_0 sets the clock frequency. A crystal or LC circuit may be inserted in lieu of a resistor for improved stability. CLK_1, the clock input, can be driven from an external clock source, which need only have standard CMOS output drive. This pin is referenced to V_{EE} for external clock inputs. A 300 kΩ resistor yields a clock frequency of about 66 kHz. (See typical characteristic curves). (See Figure 9 for alternate circuits).
37	12	V_{EE}	Negative Power Supply. Connection pin for the most negative supply. Please note the current for the output drive circuit is returned through V_{SS}. Typical supply current is 0.8 mA.
39	13	V_{SS}	Negative Power Supply for Output Circuitry. This pin sets the low voltage level for the output pins (BCD, Digit Selects, EOC, OR). When connected to analog ground, the output voltage is from analog ground to V_{DD}. If connected to V_{EE}, the output swing is from V_{EE} to V_{DD}. The recommended operating range for V_{SS} is between V_{DD} -3.0 volts and V_{EE}.
40	14	EOC	End of Conversion output generates a pulse at the end of each conversion cycle. This generated pulse width is equal to one half the period of the system clock.
41	15	OR	Overrange pin. Normally this pin is set high. When V_X exceeds V_{REF} the OR pin is low.
49 51 52 54	16 17 18 19	DS_4 DS_3 DS_2 DS_1	Digit Select pins. The digit select output goes high when the respective digit is selected. The MSD (1/2 digit) turns on immediately after an EOC pulse. The remaining digits turn on in sequence from MSD to LSD. To ensure that the BCD data has settled, an inter-digit blanking time of two clock periods is included. Clock frequency divided by 80 equals multiplex rate. For example a system clock of 66 kHz gives a multiplex rate of 0.8 kHz.
5 4 57 55	20 21 22 23	Q_3 Q_2 Q_1 Q_0	See Figure 12 for Digit Select Timing Diagram. BCD Data Output pins. Multiplexed BCD outputs contain 3 full digits of information during digit select DS2, 3, 4. During DS1, the 1/2 digit, overrange, underrange and polarity information is available. Refer to Truth Table.
6	24	V_{DD}	Positive Power Supply. This is the most positive power supply pin.

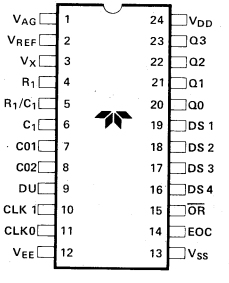
3 1/2 Digit CMOS

- Low Cost
- Multiplexed BCD Data
- ±4 Count Rollover Error

Ordering Information

Part No.	Package	Temperature Range
TSC14433BCL	24-pin CerDIP	-40 to +85°C
TSC14433BCJ	24-pin Plastic Dip	-40 to +85°C
TSC14433BCBQ	60-Pin Plastic Flat Package: Formed Leads	-40 to +85°C
TSC14433BCSQ	60-Pin Plastic Flat Package: Unformed Leads	-40 to +85°C

Pin Configuration

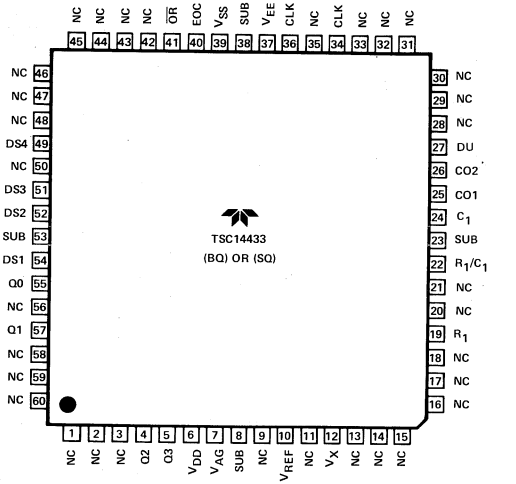


$$R_1 = \frac{V_x(max)}{C_1} \times \frac{T}{\Delta V}$$

$$\Delta V = V_{DD} - V_X\ (max) - 0.5$$

$$T = 4000 \times \frac{1}{f_{CLK}}$$

Where
R_1 is in kΩ
V_{DD} is the voltage at pin 24 referenced to V_{AG}
V_X is the voltage at pin 3 referenced to V_{AG}
f_{CLK} is the clock frequency at pin 10 in kHz



NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V^+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

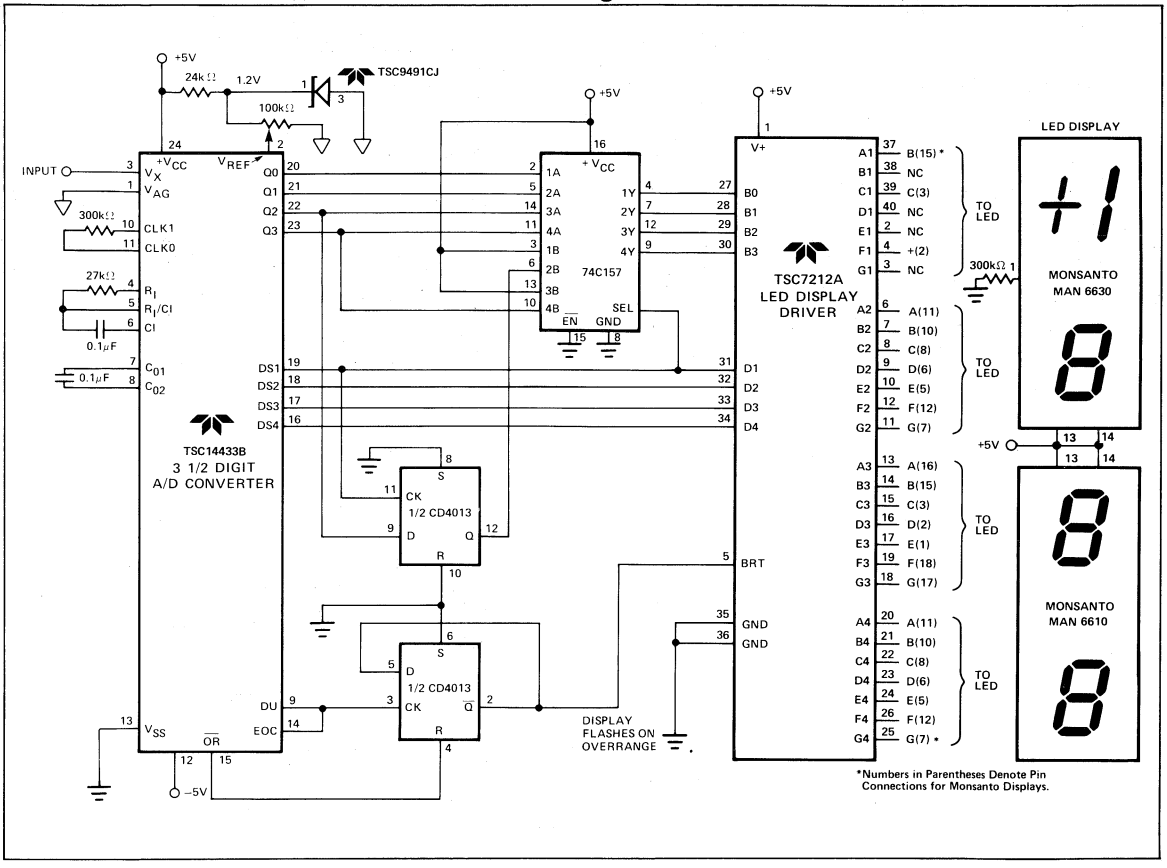
3 1/2 Digit CMOS

- Low Cost
- Multiplexed BCD Data
- ±4 Count Rollover Error

TSC14433B

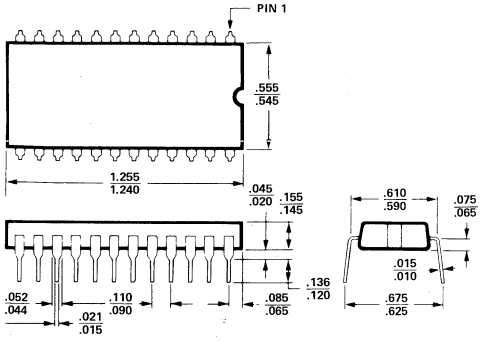
Typical Applications

TSC7212A Interface to TSC14433B 3 1/2 Digit ADC.

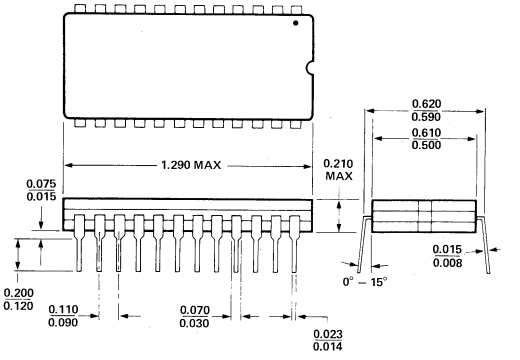


Package Information

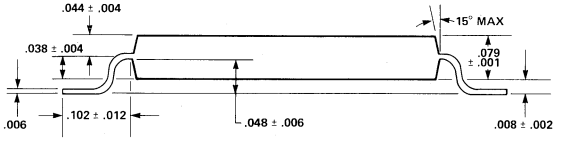
24-Pin Plastic Dip (J)
(Package #12)



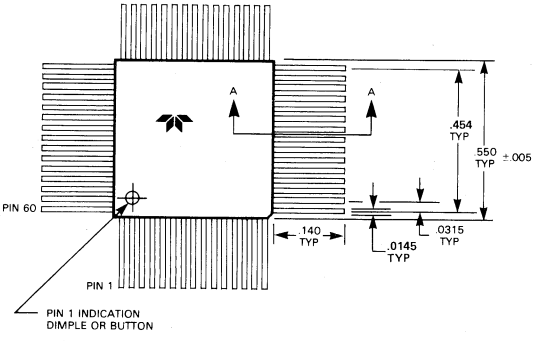
24-Pin CerDIP (L)
(Package #14)



60-Pin Flat Package
(Package #21)



60-Pin Flat Package
(Package #22)



TSC14433
3 1/2 Digit ADC
• Multiplexed BCD Data
• Low Power

General Description

The TSC14433 is a low power, high-performance, monolithic CMOS 3 1/2 digit A/D converter. The TSC14433 combines both analog and digital circuits on a single IC, thus minimizing the number of external components. This dual slope A/D converter provides automatic polarity and zero correction with the addition of two external resistors and two capacitors. The full-scale voltage range of this ratiometric IC extends from 199.9 millivolts to 1.999 volts. The TSC14433B can operate over a wide range of power supply voltages including batteries and standard 5 volt supplies.

The high impedance MOS analog inputs are well suited for applications using current, resistance or voltmeters. The output drive is compatible with low power Schottky TTL loads and conforms to standard B-series CMOS.

HANDLING PRECAUTIONS: These devices are CMOS and must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static handling procedures. Do not connect in circuits under "power on" conditions, as high transients may cause permanent damage.

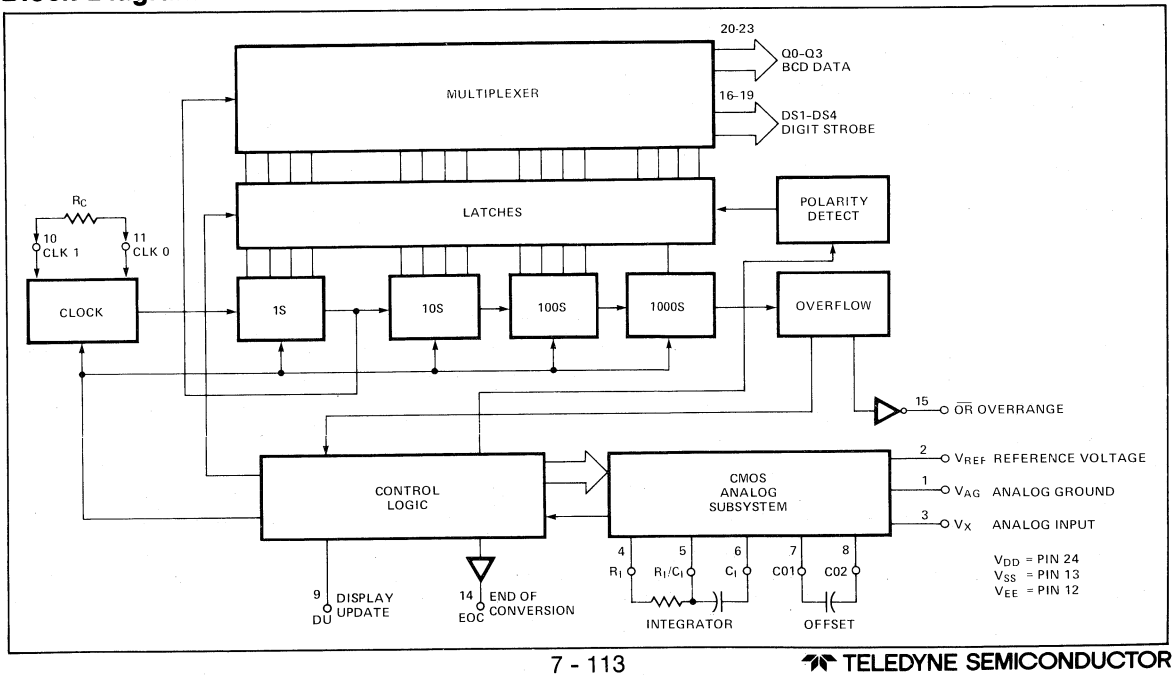
Features

- Accuracy: ±0.05% of Reading ±1 Count
- Two Voltage Ranges: 1.999 V and 199.9 mV
- Up to 25 Conversions Per Second
- Z_{IN} > 1000 M Ohm
- Single Positive Voltage Reference
- Standard B-Series CMOS Outputs — Drives One Low Power Schottky load
- Uses On-chip System Clock, or External Clock
- Low Power Consumption: 8.0 mW Typical @ ±5.0 V
- Wide Supply Range: e.g., ±4.5 V to ±8.0 V
- Overrange and Underrange Signals Available
- Operates in Auto Ranging Circuits
- Operates With LED and LCD Displays
- Low External Component Count
- Available in Compact Flat Package

Applications

- Portable Instruments
- Multimeters
- Digital Voltmeters
- Digital Panel Meters
- Digital Scales
- Digital Thermometers
- Remote A/D Sensing Systems
- MPU Systems

Block Diagram



Absolute Maximum Ratings

RATING	SYMBOL	VALUE	UNIT
DC Supply Voltage	V_{DD} to V_{EE}	-0.5 to +18	Vdc
Voltage, Any Pin, Referenced to V_{EE}	V	-0.5 to V_{DD} +0.5	Vdc
DC Current Drain Per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C

Recommended Operating Conditions

(V_{SS} = 0 or V_{EE})

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage —			
V_{DD} to Analog Ground	V_{DD}	+5.0 to +8.0	Vdc
V_{EE} to Analog Ground	V_{EE}	-2.8 to -8.0	
Clock Frequency	f_{CLK}	32 to 400	kHz
Zero Offset Correction Capacitor	C_O	0.1 ±20%	μF

Note: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{EE} \le (V_{IN}$ or $V_{OUT}) \le V_{DD}$.

Electrical Characteristics:

(C_I = 0.1 μF mylar, R_I = 470 kΩ @ V_{REF} = 2.000 V, R_I = 27 kΩ @ V_{REF} = 200.0 mV, C_O = 0.1 μF, R_C = 300 kΩ; all voltages referenced to Analog Ground, pin 1.)

CHARACTERISTIC	SYMBOL	V_{DD} Vdc	V_{EE} Vdc	-40°C MIN	-40°C MAX	25°C MIN	25°C TYP	25°C MAX	85°C MIN	85°C MAX	UNIT
Linearity Output Reading (Note 1)	—										
(V_{REF} = 2.000 V)		5.0	-5.0	—	—	-0.05	+0.05	+0.05	—	—	%rdg
(V_{REF} = 200.0 mV)		5.0	-5.0	—	—	-1 count		+1 count	—	—	
Stability Output Reading (Note 2)	—										
(V_X = 1.990 V, V_{REF} = 2.000 V)		5.0	-5.0	—	—	—	—	2	—	—	LSD
(V_X = 199.0 mV, V_{REF} = 200.0 mV)		5.0	-5.0	—	—	—	—	3	—	—	LSD
Zero Output Reading (V_X = 0 V, V_{REF} = 2.000 V)	—	5.0	-5.0	—	—	—	0	0	—	—	LSD
Bias Current —											
Analog Input	—	5.0	-5.0	—	—	—	± 20	± 100	—	—	pA
Reference Input		5.0	-5.0	—	—	—	± 20	± 100	—	—	pA
Analog Ground		5.0	-5.0	—	—	—	± 20	± 500	—	—	pA
Common-Mode Rejection (V_X = 1.4 V, V_{REF} = 2.000 V, f_{OC} = 32 kHz)		5.0	-5.0	—	—	—	65	—	—	—	dB
Output Voltage — Pins 14 to 23											
(V_{SS} = 0 V) "0" Level	V_{OL}	5.0	-5.0	—	0.05	—	0	0.05	—	0.05	V
"1" Level	V_{OH}	5.0	-5.0	4.95	—	4.95	5.0	—	4.95	—	V
(V_{SS} = -5.0 V) "0" Level	V_{OL}	5.0	-5.0	—	-4.95	—	-5.0	-4.95	—	-4.95	V
"1" Level	V_{OH}	5.0	-5.0	4.95	—	4.95	5.0	—	4.95	—	V
Output Current — Pins 14 to 23 (V_{SS} = 0V)											
(V_{OH} = 4.6 V) Source	I_{OH}	5.0	-5.0	-0.25	—	-0.2	-0.36	—	-0.14	—	mA
(V_{OL} = 0.4 V) Sink	I_{OL}	5.0	-5.0	0.64	—	0.51	0.88	—	0.36	—	mA
(V_{SS} = -5.0 V)											
(V_{OH} = 4.5 V) Source	I_{OH}	5.0	-5.0	-0.62	—	-0.5	-0.9	—	-0.35	—	mA
(V_{OL} = -4.5 V) Sink	I_O	5.0	-5.0	1.6	—	1.3	2.25	—	0.9	—	mA
Clock Frequency (R_C = 300 kΩ)	f_{CLK}	5.0	-5.0	—	—	—	66	—	—	—	kHz
Input Current — DU	I_{DU}	5.0	-5.0	—	±0.3	—	±0.00001	±0.3	—	±1.0	μA
Quiescent Current	I_Q	5.0	-5.0	—	3.7	—	0.9	2.0	—	1.6	mA
(V_{DD} to V_{EE}, I_{SS} = 0)		8.0	-8.0	—	7.4	—	1.8	4.0	—	3.2	mA
Supply Rejection (V_{DD} to V_{EE}, I_{SS} = 0, V_{REF} = 2.000 V)	—	5.0	-5.0	—	—	—	0.5	—	—	—	mV/V

Note:

1. Accuracy — The accuracy of the meter at full-scale is the accuracy of the setting of the reference voltage. Zero is recalculated during each conversion cycle. The meaningful specification is linearity. In other words, the deviation from correct reading for all inputs other than positive full-scale and zero is defined as the linearity specification.
2. Three LSD stability for 200 mV scale is defined as the range that the LSD will occupy 95% of the time.
3. Pin numbers refer to 24-pin DIP.

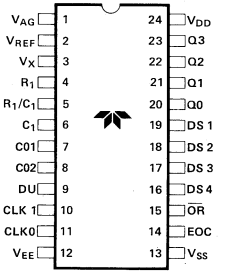
Pin Description

PIN NO. 60-Pin FP	PIN NO. 24-Pin DIP	SYMBOL	DESCRIPTION
7	1	V_{AG}	This is the Analog Ground. It has a high input impedance. This pin determines the reference level for the unknown input voltage (V_X) and the reference voltage (V_{REF}).
10	2	V_{REF}	Reference voltage. Full-scale output is equal to the voltage applied to V_{REF}. Therefore, full-scale voltage of 1.999 V requires 2.000 V reference and 199.9 mV full-scale requires a 200 mV reference. V_{REF} functions as system reset, also. When switched to V_{EE} the system is reset to the beginning of the conversion cycle.
12	3	V_X	The Unknown Input Voltage (V_X) is measured as a ratio of the reference voltage (V_{REF}) in a ratio-metric A/D conversion.
19 22 24	4 5 6	R_1 R_1/C_1 C_1	These pins are for external components used for the integration function in the dual slope conversion. Typical values are 0.1 μF (mylar) capacitor for C_1. R_1 = 470 kΩ (resistor) for 2.0 V full-scale. R_1 = 27 kΩ (resistor) for 200 mV full-scale. Clock frequency of 66 kHz gives 250 ms conversion time. See equation below for calculation of integrator component values.
25 26	7 8	CO_1 CO_2	These pins are used for connecting the offset correction capacitor. The recommended value is 0.1 μF.
27	9	DU	Display Update input pin. When DU is connected to the EOC output every conversion is displayed. New data will be strobed into the output latches during the conversion cycle if a positive edge is received on DU prior to the ramp-down cycle. When this pin is driven from an external source, the voltage should be referenced to V_{SS}.
34 36	10 11	CLK_1 CLK_0	Clock input pins. The TSC14433 has its own oscillator system clock. Connecting a single resistor between CLK_1 and CLK_0 sets the clock frequency. A crystal or LC circuit may be inserted in lieu of a resistor for improved stability. CLK_1, the clock input, can be driven from an external clock source, which need only have standard CMOS output drive. This pin is referenced to V_{EE} for external clock inputs. A 300 kΩ resistor yields a clock frequency of about 66 kHz. (See typical characteristic curves). (See Figure 9 for alternate circuits).
37	12	V_{EE}	Negative Power Supply. Connection pin for the most negative supply. Please note the current for the output drive circuit is returned through V_{SS}. Typical supply current is 0.8 mA.
39	13	V_{SS}	Negative Power Supply for Output Circuitry. This pin sets the low voltage level for the output pins (BCD, Digit Selects, EOC, OR). When connected to analog ground, the output voltage is from analog ground to V_{DD}. If connected to V_{EE}, the output swing is from V_{EE} to V_{DD}. The recommended operating range for V_{SS} is between V_{DD} -3.0 volts and V_{EE}.
40	14	EOC	End of Conversion output generates a pulse at the end of each conversion cycle. This generated pulse width is equal to one half the period of the system clock.
41	15	OR	Overrange pin. Normally this pin is set high. When V_X exceeds V_{REF} the OR pin is low.
49 51 52 54	16 17 18 19	DS_4 DS_3 DS_2 DS_1	Digit Select pins. The digit select output goes high when the respective digit is selected. The MSD (1/2 digit) turns on immediately after an EOC pulse. The remaining digits turn on in sequence from MSD to LSD. To ensure that the BCD data has settled, an inter-digit blanking time of two clock periods is included. Clock frequency divided by 80 equals multiplex rate. For example a system clock of 66 kHz gives a multiplex rate of 0.8 kHz.
5 4 57 55	20 21 22 23	Q_3 Q_2 Q_1 Q_0	See Figure 12 for Digit Select Timing Diagram. BCD Data Output pins. Multiplexed BCD outputs contain 3 full digits of information during digit select DS2, 3, 4. During DS1, the 1/2 digit, overrange, underrange and polarity information is available. Refer to Truth Table.
6	24	V_{DD}	Positive Power Supply. This is the most positive power supply pin.

Ordering Information

Part No.	Package	Temperature Range
TSC14433CJ	24-pin Plastic Dip	-40° C to +85° C
TSC14433CL	24-pin CerDIP	-40° C to +85° C
TSC14433CBQ	60-Pin Plastic Flat Package: Formed Leads	-40° C to +85° C
TSC14433CSQ	60-Pin Plastic Flat Package: Unformed Leads	-40° C to +85° C
Devices with 160, Hour, +125° C Burn-In		
TSC14433CJ/BI	24-Pin Plastic Dip	-40° C to +85° C
TSC14433CL/BI	24-Pin CerDIP	-40° C to +85° C

Pin Configuration

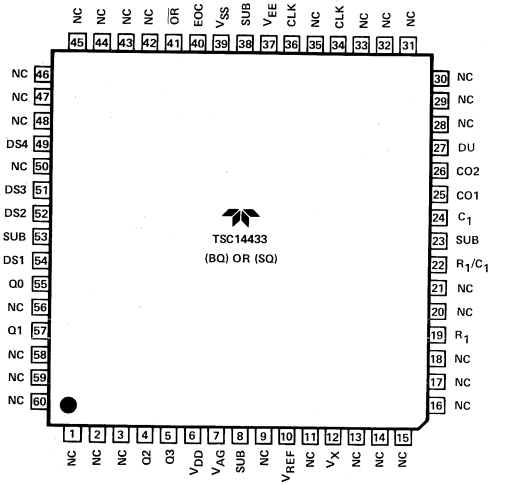


$$R_1 = \frac{V_X(max)}{C_1} \times \frac{T}{\Delta V}$$

$$\Delta V = V_{DD} - V_X\ (max) - 0.5$$

$$T = 4000 \times \frac{1}{f_{CLK}}$$

Where
R_1 is in kΩ
V_{DD} is the voltage at pin 24 referenced to V_{AG}
V_X is the voltage at pin 3 referenced to V_{AG}
f_{CLK} is the clock frequency at pin 10 in kHz



NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V^+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

Typical Characteristics

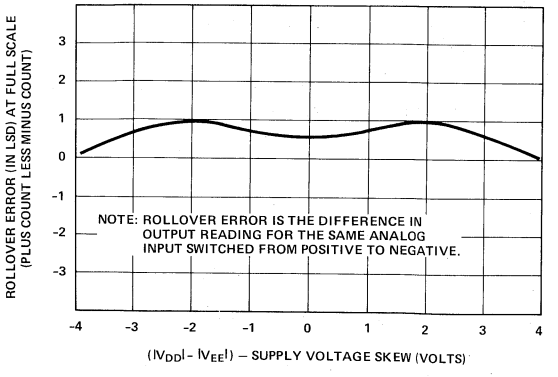


Figure 1: Typical Rollover Error vs. Power Supply Skew.

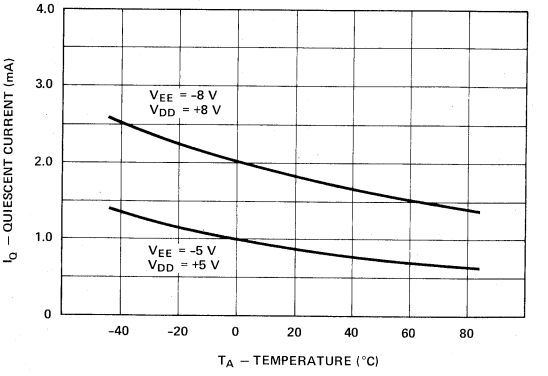


Figure 2: Typical Quiescent Power Supply Current vs. Temperature.

Typical Characteristics (Cont.)

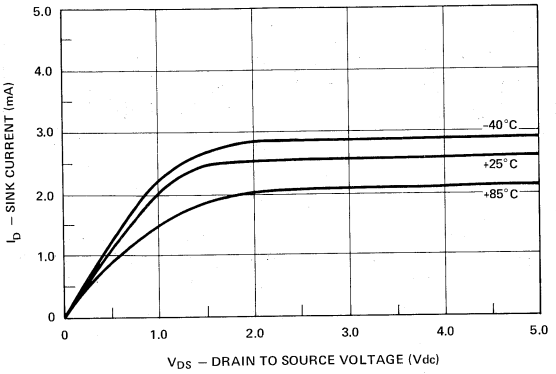


Figure 3: Typical N-Channel Sink Current at $V_{DD}-V_{SS}$ = 5 Volts.

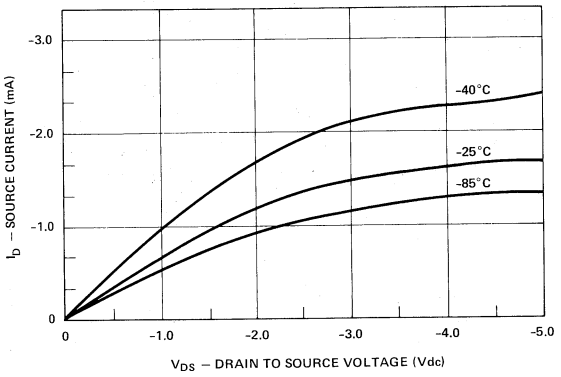


Figure 4: Typical P-Channel Source Current at $V_{DD}-V_{SS}$ = 5 Volts.

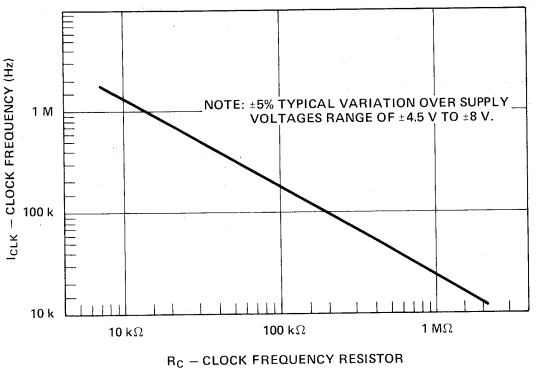


Figure 5: Typical Clock Frequency vs. Resistor (R_C).

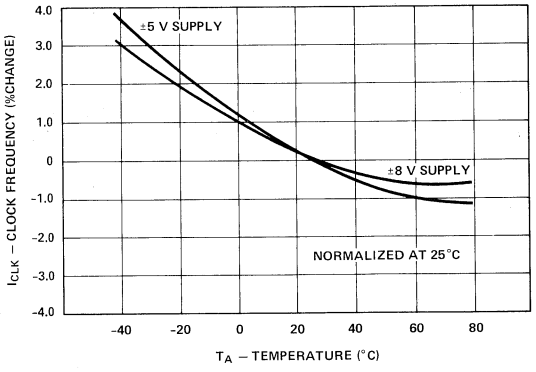


Figure 6: Typical % Change of Clock Frequency vs. Temperature.

CONVERSION RATE =	$\frac{\text{CLOCK FREQUENCY}}{16{,}400}$ ±1.5%
MULTIPLEX RATE =	$\frac{\text{CLOCK FREQUENCY}}{80}$

Circuit Description

The TSC14433 CMOS IC becomes a modified dual slope A/D with a minimum of external components. This IC has the customary CMOS digital logic circuitry as well as the CMOS analog circuitry. It provides the user with digital functions (Such as counters, latches, multiplexers) and analog functions (such as operational amplifiers and comparators) on a single chip.

Features of this sytem include auto-zero, high input impedances and autopolarity. Low power consumption and a wide range of power supply voltages are also advantages of this CMOS device. The system's auto-zero function compensates for the offset voltage of the internal amplifiers and comparators. In this "ratiometric system," the output reading is the ratio of the unknown voltage to the reference voltage where a ratio of 1 equal to the maximum count of 1999. It takes approximately 16,000 clock periods to complete one conversion cycle. Each conversion cycle may be divided into six segements. Figure 7 shows the conversion cycle in 6 segments for both positive and negative inputs.

Segment 1 — The offset capacitor (C_O), which compensates

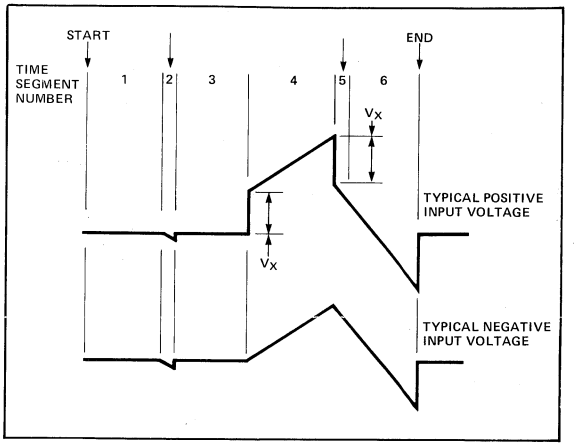


Figure 7: Integrator Waveforms at Pin 6.

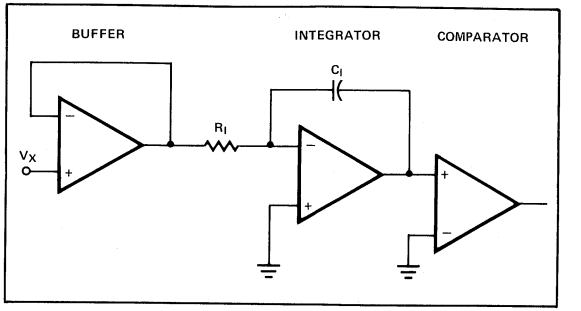


Figure 8: Equivalent Circuit Diagrams of the Analog Section During Segment 4 of the Timing Cycle.

for the input offset voltages of the buffer and integrator amplifiers, is charged during this period. However, the integrator capacitor is shorted. This segment requires 4000 clock periods.

During Segment 2 — The integrator output decreases to the comparator threshold voltage. At this time a number of counts equivalent to the input offset voltage of the comparator is stored in the offset latches for later use in the auto-zero process. The time for this segment is variable, and less than 800 clock periods.

Segment 3 — This segment of the conversion cycle is the same as Segment 1.

Segment 4 — Segment 7 is an up-going ramp cycle with the unknown input voltage (V_X) as the input to the integrator. Figure 8 shows the equivalent configuration of the analog section of the TSC14433. The actual configuration of the analog section is dependent upon the polarity of the input voltage during the previous conversion cycle.

Segment 5 — this segment is a down-going ramp period with the reference voltage as the input to the integrator. Segment 5 of the conversion cycle has a time equal to the number of counts stored in the offset storage latches during Segment 2. As a result, the system zeros automatically.

Segment 6 — This is an extension of Segment 5. The time period for this portion is 4000 clock periods. The results of the A/D conversion cycle are determined in this portion of the conversion cycle.

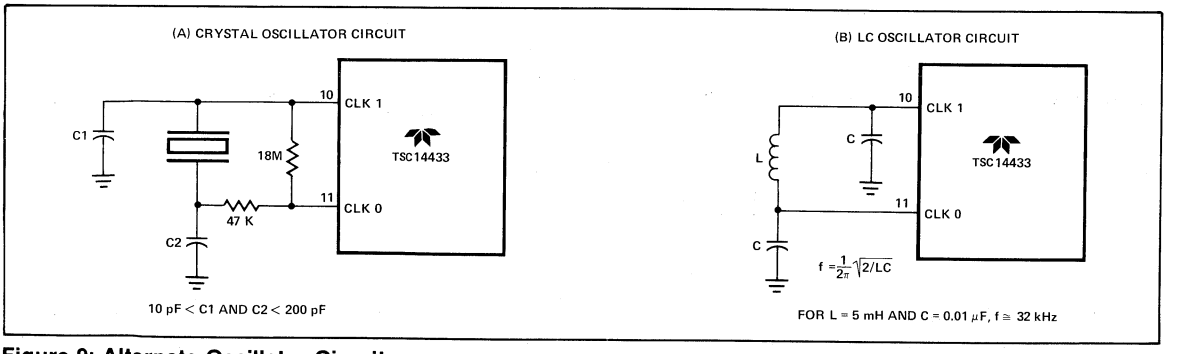


Figure 9: Alternate Oscillator Circuits.

Applications Information

Figure 10 is an example of a 3 1/2 digit voltmeter using the TSC14433 with common-anode displays. This system require a 2.5 V reference. Full-scale may be adjusted to 1.999 V or 199.9 mV. Input overrange is indicated by flashing a display.

This display uses LEDs with common anode digit lines. Power supply for this system is shown as a dual ±5 V supply; however, the TSC14433 will operate over a wide voltage range (see recommended operating conditions, page 3).

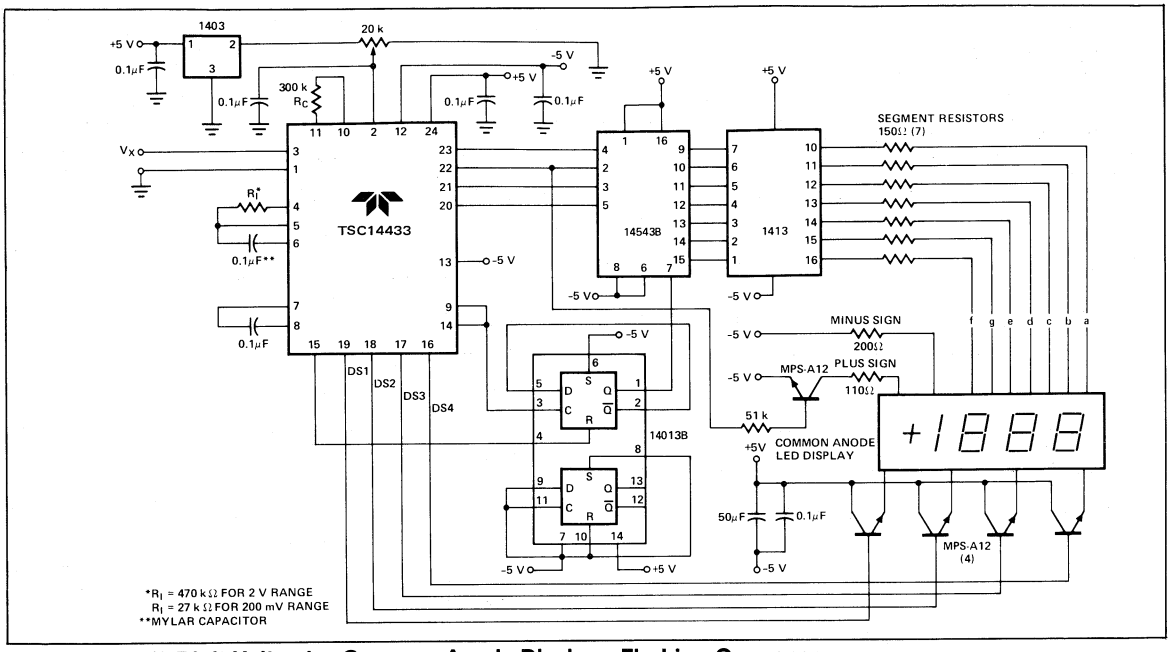


Figure 10: 3 1/2 Digit Voltmeter-Common Anode Displays, Flashing Overrange

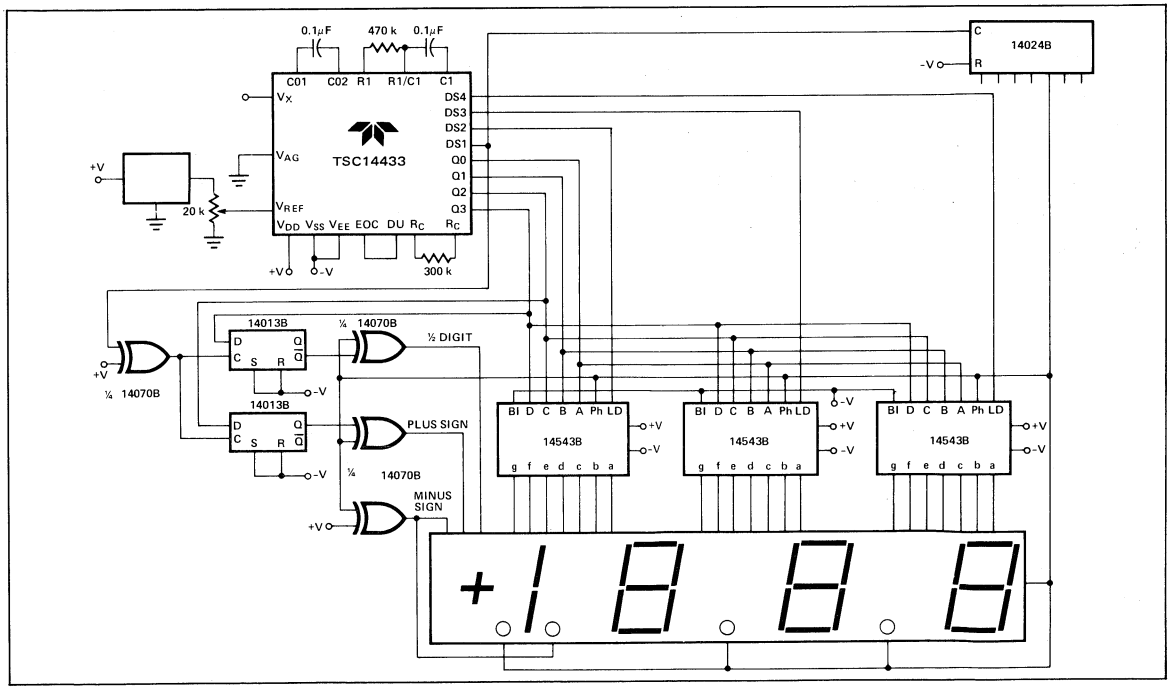


Figure 11: 3 1/2 Digit Voltmeter with LCD Display.

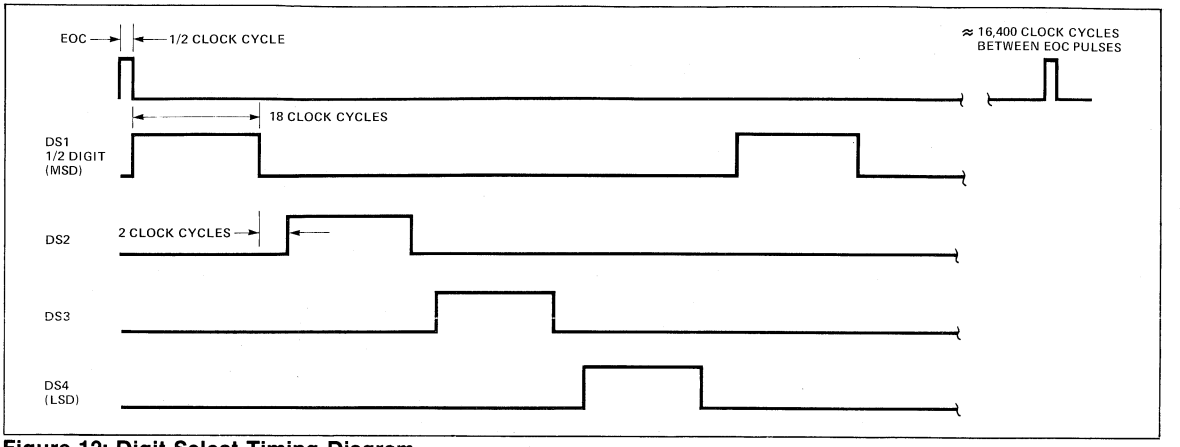


Figure 12: Digit Select Timing Diagram

The circuit in Figure 11 shows a 3 1/2 digit LCD voltmeter. The 14024B provides the low frequency square wave signal drive to the LCD backplane. Dual power supplies are shown here, however, one supply may be used when V_{SS} is connected to V_{EE}. In this case V_{AG} must be at least 2.8 V above V_{EE}.

When only segment b and c of the decoder are connected to the 1/2 digit of the display, 4, 0, 7 and 3 appear as 1.

The overrange indication (Q3 = 0 and Q0 = 1) occurs when the count is greater than 1999, e.g., 1.999 V for a reference of 2.000 V. The underrange indication, useful for autoranging circuits, occurs when the count is less than 180, e.g., 0.180 V for a reference of 2.000 V.

CAUTION: If the most significant digit is connected to a display other than a "1" only; such as a full digit display, segments other than b and c must be disconnected. The BCD to seven segment decoder must blank on BCD inputs 1010 to 1111.

TRUTH TABLE

CODED CONDITION OF MSD	Q3	Q2	Q1	Q0	BCD TO 7 SEGMENT DECODING
+0	1	1	1	0	Blank
—0	1	0	1	0	Blank
+0 UR	1	1	1	1	Blank
—0 UR	1	0	1	1	Blank
+1	0	1	0	0	4 → 1 Hook Up
—1	0	0	0	0	0 → 1 only seg b
+1 OR	0	1	1	1	7 → 1 and c to
—1 OR	0	0	1	1	3 → 1 MSD

Notes for Truth Table
Q3 — 1/2 digit, low for "1", high for "0"
Q2 — Polarity: "1" = positive, "0" = negative
Q0 — Out of range condition exists if Q0 = 1. When used in conjunction with Q3 the type of out of range condition is indicated, i.e., Q3 = 0 ➧ OR or Q3 = 1 ➧ UR.

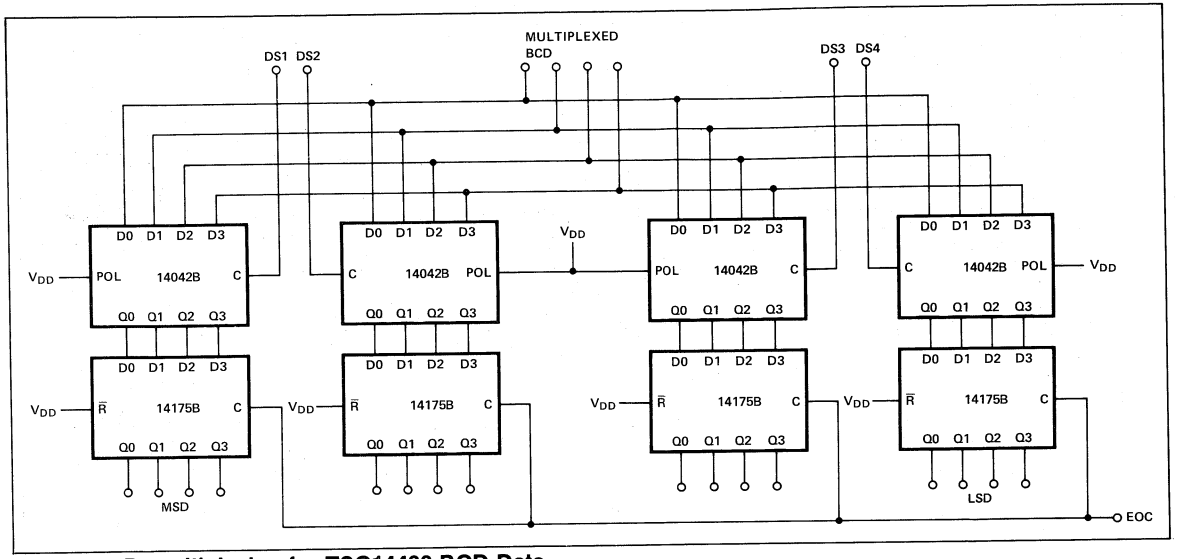


Figure 13: Demultiplexing for TSC14433 BCD Data.

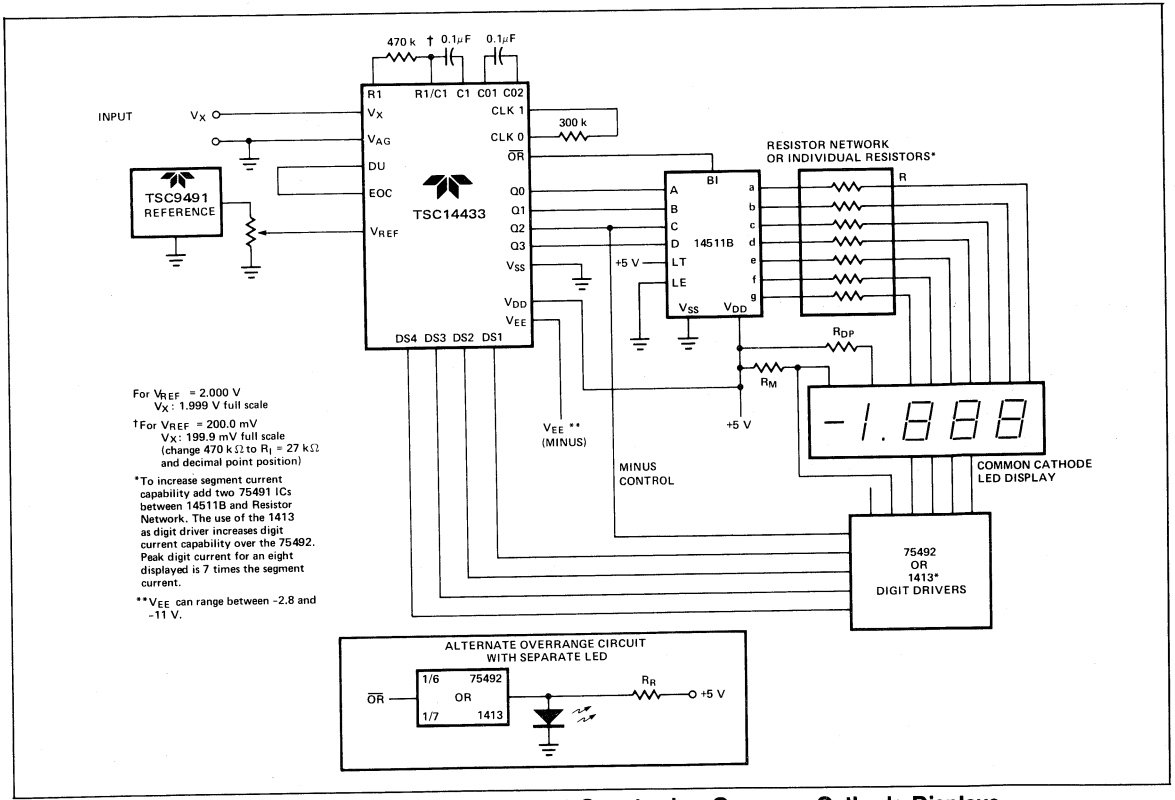


Figure 14: 3 1/2 Digit Voltmeter with Low Component Count using Common Cathode Displays.

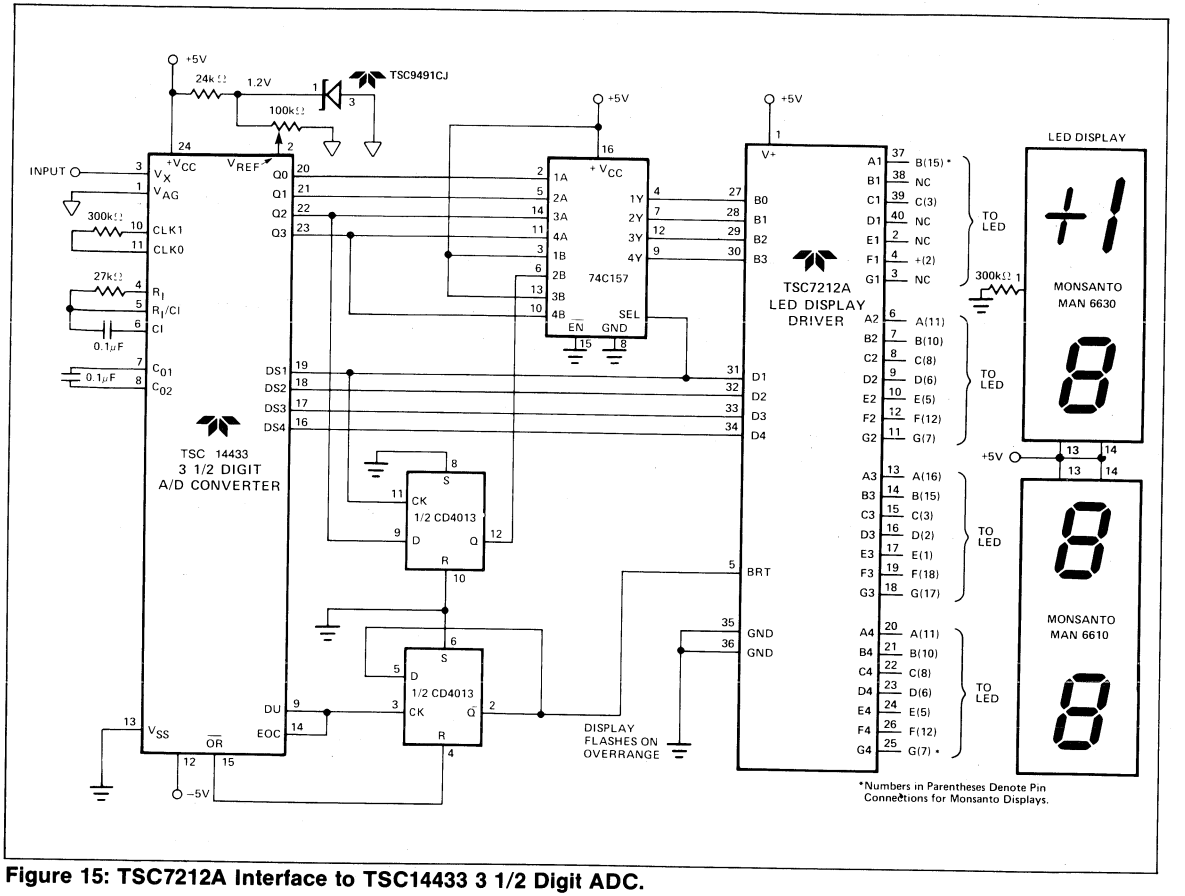
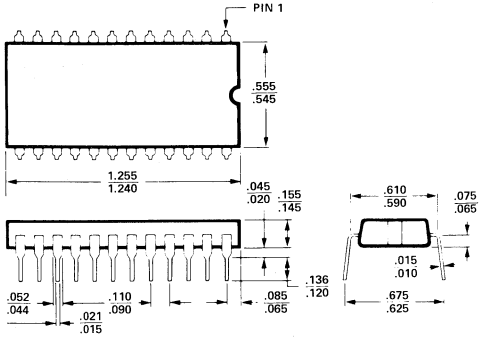


Figure 15: TSC7212A Interface to TSC14433 3 1/2 Digit ADC.

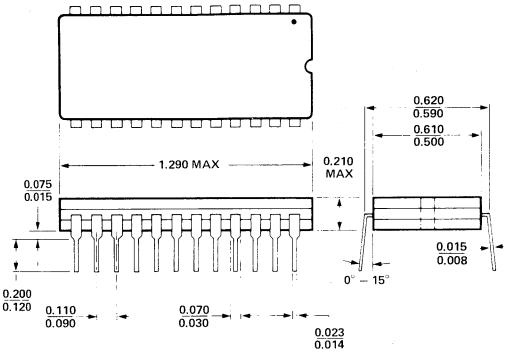
Figure 14 is an example of a 3 1/2 digit LED voltmeter with a minimum of external components (only 11 additional components). In this circuit the 14511B provides the segment drive and the 75492 or 1413 provides sink for digit current. Display is blanked during the overrange condition.

Package Information

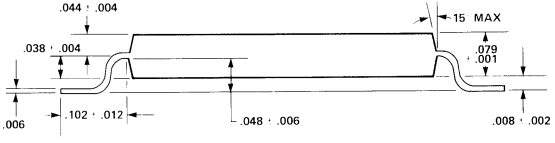
24-Pin Plastic Dip (J)
(Package #12)



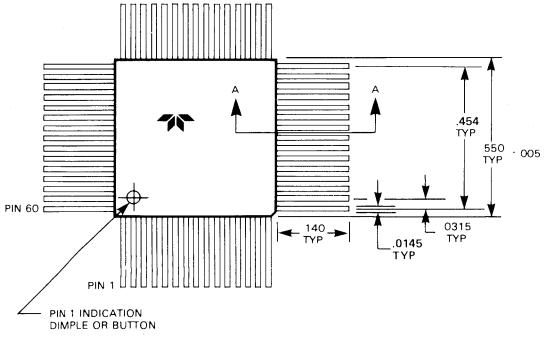
24-Pin CerDIP (L)
(Package #14)



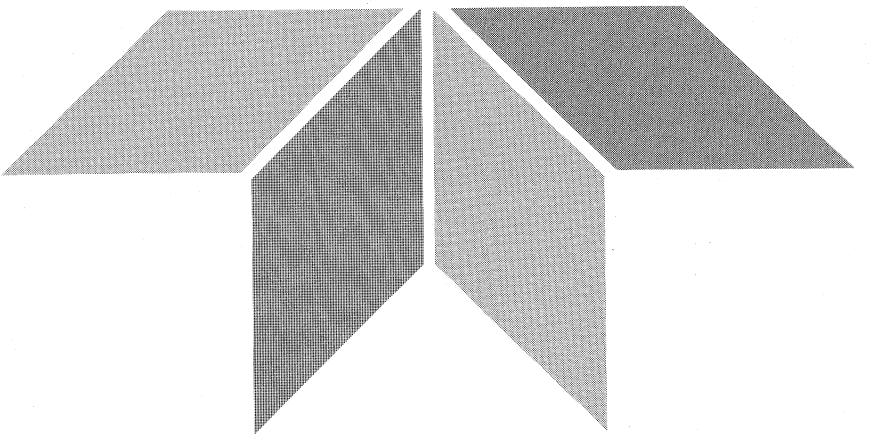
60-Pin Flat Package
(Package #21)



60-Pin Flat Package
(Package #22)



7



SECTION 8

Binary Analog-to-Digital Converters

Section 8
Binary A/D Converters 8-1

TSC7109	12-Bit Plus Sign Integrating A/D Converter	8-3
TSC800	15-Bit Plus Sign Integrating A/D Converter	8-23
TSC8700 (8-Bit)	Binary Output ADC	8-39
TSC8701 (10-Bit)	Binary Output ADC	8-39
TSC8702 (12-Bit)	Binary Output ADC	8-39
TSC8703 (8-Bit)	Three State Binary Output ADC	8-51
TSC8704 (10-Bit)	Three State Binary Output ADC	8-51
TSC8705 (12-Bit)	Three State Binary Output ADC	8-51

TELEDYNE SEMICONDUCTOR

TSC7109
12-Bit Plus Sign Integrating A/D Converter
• BUS Compatible
• Serial Data Transmission w/UART

General Description

The TSC7109 is a 12-bit plus sign CMOS low power A/D Converter. The single CMOS IC contains all the necessary active devices to interface with microprocessors.

In direct mode, Chip Select and High/Low Byte Enables control parallel bus interface. In the handshake mode the TSC7109 will operate with industry standard UART's in controlling serial data transmission, ideal for remote data logging. Control and monitoring of conversion timing is provided by the RUN/$\overline{\text{HOLD}}$ and STATUS outputs. The TSC7109 requires only the addition of eight passive components plus a crystal to operate as a dual slope integrating A/D converter. The TSC7109 has features that make it an attractive per-channel alternative to analog multiplexing for many data acquisition applications. These features include typical input bias current of 1 pA, drift of less than 1 μV/°C, input noise typically 15 μV p-p, and auto-zero. True differential input and reference allows the measurement of bridge-type transducers such as load cells, strain gauges and temperature transducers.

For applications requiring more resolution see the TSC800, 15-bit plus sign data sheet.

Features

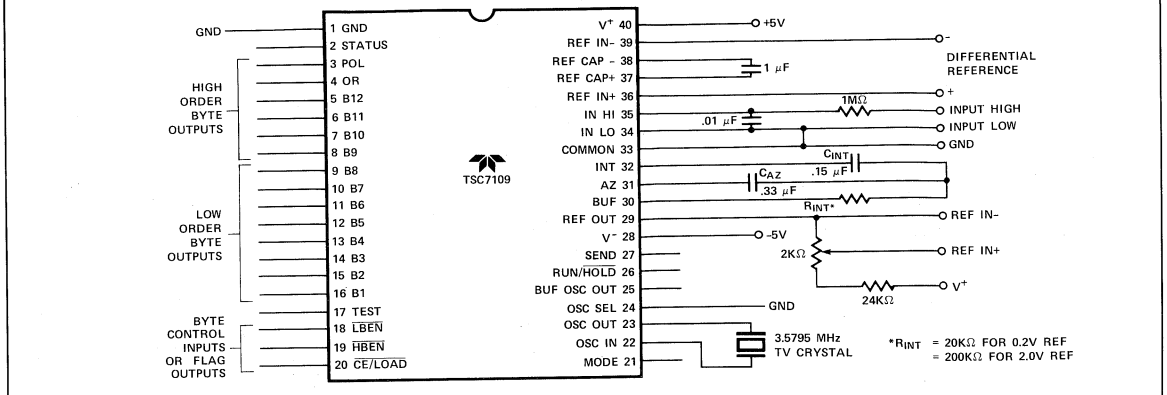
- 12-Bit Plus Sign Integrating A/D Converter with Overrange Indication
- Sign Magnitude Coding Format
- True Differential Signal Input and Differential Reference Input
- Low Noise — Typically 15 μVp-p
- High Normal Mode Noise and Line Frequency Rejection
- 1 pA Typical Input Current
- No Zero Adjustment
- TTL Compatible Byte Organized Tri-State Outputs
- UART Handshake Mode for Simple Serial Data Transmission
- Direct Bus Connection for 8 or 16-Bit Bus — 3.58 mHz Crystal Provides 7.5 Conversions Per Second for 60 Hz Rejection — External RC Network Provides up to 30 Conversions Per Second
- Power Dissipation Typically Less Than 20 mW
- Internal Voltage Reference

8

Ordering Information

Part No.	Package	Temp. Range
TSC7109CPL	40-Pin Plastic Dip	0° C to + 70° C
TSC7109BCPL	40-Pin Plastic Dip	0° C to +70° C
TSC7109IJL	40-Pin CerDIP	-25° C to +85° C
TSC7109BIJL	40-Pin CerDIP	-25° C to +85° C
TSC7109MJL	40-Pin CerDIP	-55° C to +125° C
TSC7109CBQ	60-Pin Plastic Flat Package: Formed Leads	0° C to +70° C
TSC7109CSQ	60-Pin Plastic Flat Package: Unformed Leads	0° C to +70° C
Devices Available with 160 Hour, +125° C Burn-In		
TSC7109CPL/BI	40-Pin Plastic Dip	0° C to +70° C
TSC7109IJL/BI	40-Pin CerDIP	-25° C to +85° C
Devices with MIL-STD-883 Processing		
TSC7109MJL/883	40-Pin CerDIP	-55° C to +125° C

Test Circuit (See Figure 1 for typical connection to A UART or Microcomputer)



Absolute Maximum Ratings

Positive Supply Voltage (GND to V^+) ..... +6.2 V
Negative Supply Voltage (GND to V^-) ..... -9 V
Analog Input Voltage (LOW or HIGH) (Note 1) ... V^+ to V^-
Reference Input Voltage (LOW or HIGH) (Note 1) .. V^+ to V^-
Digital Input Voltage
(Pins 2-27) (Note 2) ..... GND -0.3 V
Power Dissipation (Note 3)
Ceramic Package ..... 1 W @ +85°C
Plastic Package ..... 500 mW @ +70°C
Operating Temperature
Ceramic Package (M) ..... -55°C ≤ T_A ≤ +125°C
(I) ..... -25°C ≤ T_A ≤ +85°C
Plastic Package (C) ..... 0°C ≤ T_A ≤ +70°C
Storage Temperature ..... -55°C ≤ T_A ≤ +125°C
Lead Temperature (Soldering, 60 sec.) ..... +300°C

This device contains circuitry to protect the inputs from damage due to high static voltage or electric fields. It is advised that voltages great than those listed under absolute maximum ratings, may cause permanent damage to the devices. Normal precautions should be taken to avoid application of any voltage higher than maximum ratings.

Notes:

1. Input voltages may exceed the supply voltages if the input current is limited to ±100 μA.
2. Connecting any digital inputs or outputs to voltages greater than V^+ or less than GND may cause destructive device latchup. Therefore, it is recommended that inputs from sources other than the same power supply should not be applied to the TSC7109 before its power supply is established. In multiple supply systems, the supply to the TSC7109 should be activated first.
3. This limit refers to that of the package and will not occur during the normal operation.
4. *HANDLING PRECAUTIONS:* These devices are CMOS and must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static tubes or other conducting material. Use proper anti-static handling procedures. Do not connect in circuits under "power-on" conditions, as high transients may cause permanent damage.

Electrical Characteristics: All parameters with $V^+ = +5$ V, $V^- = -5$ V, GND = 0 V, $T_A = 25°C$, unless otherwise indicated.

Test circuit as shown on page 1.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC7109 MIN	TSC7109 TYP	TSC7109 MAX	UNIT
ANALOG	1		Zero Input Reading	V_{IN} = 0.0 V Full-Scale = 409.6 mV	-0000_8	$\pm0000_8$	$+0000_8$	Octal Reading
	2		Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 204.8 mV	3777_8	3777_8 4000_8	4000_8	Octal Reading
	3	NL	Non-Linearity (Max. Deviation From Best Straight Line Fit)	Full-Scale = 409.6 mV to 4.096 V Over Full Operating Temp. Range.	-1	±2	+1	Counts
	4		Roll-Over Error (Difference in Reading for Equal Pos. and Neg. Inputs Near Full-Scale)	Full-Scale = 409.6 mV to 4.096 V Over Full Operating Temp. Range.	-1	±2	+1	Counts
	5	CMRR	Input Common-Mode Rejection Ratio	V_{CM} ±1 V V_{IN} = 0 V Full-Scale = 409.6 mV	—	50	—	μV/V
	6	VCMR	Common-Mode Range	Input High, Input Low, Common	V^- +1.5	—	V^+ -1.0	V
	7		Noise (p-p value not Exceeded 95% of Time)	V_{IN} = 0 V Full-Scale = 409.6 mV	—	15	—	μV
	8	I_{IN}	Leakage Current at Input TSC7109	V_{IN} = 0 All Packages 25°C TSC7109CPL 0°C ≤ T_A ≤ +70°C TSC7109IJL -25°C ≤ T_A ≤ +85°C TSC7109MJL -55°C ≤ T_A ≤ +125°C	— — — —	1 20 100 2	10 100 250 5	pA pA pA nA
	9	I_{IN}	Leakage Current at Input TSC7109B	V_{IN} = 0 All Packages 25°C TSC7109BCPL 0°C ≤ T_A ≤ +70°C TSC7109BIJL -25°C ≤ T_A ≤ +85°C	— — —	1 — —	10 500 750	pA pA pA
	10	TC_{ZS}	Zero Reading Drift	V_{IN} = 0 V	—	0.2	1	μV/°C
	11	TC_{FS}	Scale Factor Temperature Coefficient	V_{IN} = 408.9 mV = >7770_8 Reading Ext. Ref. 0 ppm/°C	—	1	5	ppm/°C
	12	I^+	Supply Current V^+ to GND	V_{IN} = 0, Crystal Osc. 3.58 MHz Test Circuit Pins 2-21, 25, 26, 27, 29, Open	—	700	1500	μA
	13	I_{SUPP}	Supply Current V^+ to V^-		—	700	1500	μA
	14	V_{REF}	Ref Out Voltage	Referred to V^+, 25 kΩ Between V^+ and Ref Out	-2.4	-2.8	-3.2	V
	15	TC_{REF}	Ref Out Temp. Coefficient	25 kΩ Between V^+ and Ref Out	—	80	—	ppm/°C

Electrical Characteristics: All parameters with $V^+ = +5$ V, $V^- = -5$ V, GND = 0 V, $T_A = 25°$ C, unless otherwise indicated. Test circuit as shown on page 1.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC7109 MIN	TYP	MAX	UNIT
DIGITAL	16	V_{OH}	Output High Voltage	I_{OUT} = 100 μA Pins 2-16, 18, 19, 20	3.5	4.3	—	V
	17	V_{OL}	Output Low Voltage	I_{OUT} = 1.6 mA	—	0.2	0.4	V
	18		Output Leakage Current	Pins 3-16 High Impedance	—	±.01	±1	μA
	19		Control I/0 Pullup Current	Pins 18, 19, 20 $V_{OUT} = V^+$ -3 V MODE Input at GND	—	5	—	μA
	20		Control I/0 Loading	HBEN Pin 19 LBEN Pin 16	—	—	50	pF
	21	V_{IH}	Input High Voltage	Pins 18-21, 26, 27 referred to GND	2.5	—	—	V
	22	V_{IL}	Input Low Voltage	Pins 18-21, 26, 27 Referred to GND	—	—	1	V
	23		Input Pullup Current	Pins 26, 27 $V_{OUT} = V^+$ -3 V	—	5	—	μA
	24		Input Pullup Current	Pins 17, 24 $V_{OUT} = V^+$ -3 V	—	25	—	μA
	25		Input Pulldown Current	Pin 21, V_{OUT} = GND +3 V	—	1	—	μA
	26	O_{OH}	Oscillator Output High	V_{OUT} = 2.5 V	—	1	—	mA
		O_{OL}	Current Low	V_{OUT} = 2.5 V	—	1.5	—	mA
	27	BO_{OH}	Buffered Oscillator High	V_{OUT} = 2.5 V	—	2	—	mA
		BO_{OL}	Output Current Low	V_{OUT} = 2.5 V	—	5	—	mA
	28	t_W	MODE Input Pulse Width		60	—	—	ns

8

Pin Description

40-Pin DIP Pin Number Normal/(Reverse)	60-Pin Flat Package Pin Number	Name	Description
1	9	GND	Digital Ground, 0 V, Ground Return for all digital logic.
2	10	STATUS	Output High during integrate and deintegrate until data is latched. Output Low when analog section is in Auto-Zero configuration.
3	11	POL	Polarity — High for Positive Input.
4	12	OR	Overrange — High if Overranged.
5	13	B_{12}	Bit 12 (Most Significant Bit).
6	18	B_{11}	Bit 11.
7	19	B_{10}	Bit 10.
8	20	B_9	Bit 9.
9	21	B_8	Bit 8.
10	22	B_7	Bit 7.
11	24	B_6	Bit 6
12	25	B_5	Bit 5.
13	26	B_4	Bit 4.
14	27	B_3	Bit 3.
15	28	B_2	Bit 2.
16	33	B_1	Bit 1 (Least Significant Bit).
17	34	TEST	Input High — Normal Operation. Input Low — Forces all bit outputs high. Note: This input is used for test purposes only.

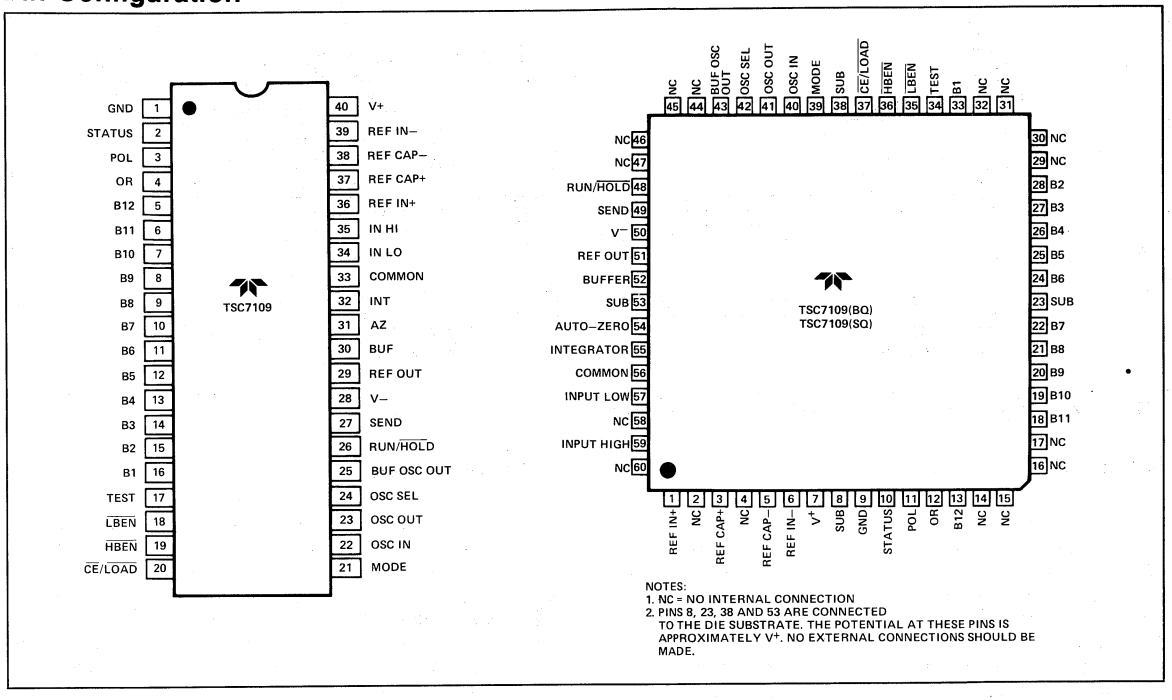
All three state output data bits

Pin Description (Cont.)

40-Pin DIP Pin Number Normal/(Reverse)	60-Pin Flat Package Pin Number	Name	Description
18	35	$\overline{\text{LBEN}}$	Low Byte Enable — With MODE (Pin 21) low, and $\overline{\text{CE}}/\overline{\text{LOAD}}$ (Pin 20) low, taking this pin low activates low order byte outputs B1-B8. With MODE (Pin 21) high, this pin serves as low byte flag output used in handshake mode. See Figures 7, 8, 9.
19	36	$\overline{\text{HBEN}}$	High Byte Enable — With MODE (Pin 21) low, and $\overline{\text{CE}}/\overline{\text{LOAD}}$ (Pin 20) low, taking this pin low activates high order byte outputs B9-B12, POL, OR. With MODE (Pin 21) high, this pin serves as high byte flag output used in handshake mode. See Figures 7, 8. 9.
20	37	$\overline{\text{CE}}/\overline{\text{LOAD}}$	Chip Enable Load — With MODE (Pin 21)low, $\overline{\text{CE}}/\overline{\text{LOAD}}$ serves as a master output enable. When high, B1-B12, POL, OR outputs are disabled. When MODE (Pin 21) low, a load strobe used in handshake mode. See Figures 7, 8, 9.
21	7	MODE	Input Low — Direct output mode where $\overline{\text{CE}}/\overline{\text{LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19) and $\overline{\text{LBEN}}$ (Pin 18) act as inputs directly controlling byte outputs. Input Pulsed High — Causes immediate entry into handshake mode and output of data as in Figure 9. Input High — Enables $\overline{\text{CE}}/\overline{\text{LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19), and $\overline{\text{LBEN}}$ (Pin 18) as outputs, handshake mode will be entered and data output as in Figures 7 and 8 at conversions completion.
22	40	OSC IN	Oscillator Input
23	41	OSC OUT	Oscillator Output
24	42	OSC SEL	Oscillator Select — Input high configures OSC IN, OSC OUT, BUF OSC OUT as RC oscillator — clock will be same phase and duty cycle as BUF OSC OUT. Input low configures OSC IN, OSC OUT for crystal oscillator — clock frequency will be 1/58 of frequency at BUF OSC OUT.
25	43	BUF OSC OUT	Buffered Oscillator Output.
26	48	RUN/$\overline{\text{HOLD}}$	Input High — Conversions continuously performed every 8192 clock pulses. Input Low — Conversion in progress completed, converter will stop in Auto-Zero seven counts before integrate.
27	49	SEND	Input — Used in handshake mode to indicate ability of an external device to accept data.
28	50	V^-	Analog Negative Supply — Nominally -5 V with respect to GND (Pin 1).
29	51	REF OUT	Reference Voltage Output — Nominally 2.8 V down from V^+ (Pin 40).
30	52	BUFFER	Buffer Amplifier Output.
31	54	AUTO-ZERO	Auto-Zero Node — Inside foil of C_{AZ}.
32	55	INTEGRATOR	Integrator Output — Outside foil of C_{INT}.
33	56	COMMON	Analog Common — System is Auto-Zeroed to COMMON.
34	57	INPUT LOW	Differential Input Low Side.
35	59	INPUT HIGH	Differential Input High Side.
36	1	REF IN +	Differential Reference Input Positive.
37	3	REF CAP +	Reference Capacitor Positive.
38	5	REF CAP -	Reference Capacitor Negative.
39	6	REF IN -	Differential Reference Input Negative.
40	7	V^+	Positive Supply Voltage — Nominally +5 V with respect to GND (Pin 1).

NOTE: All digital levels are positive true.

Pin Configuration



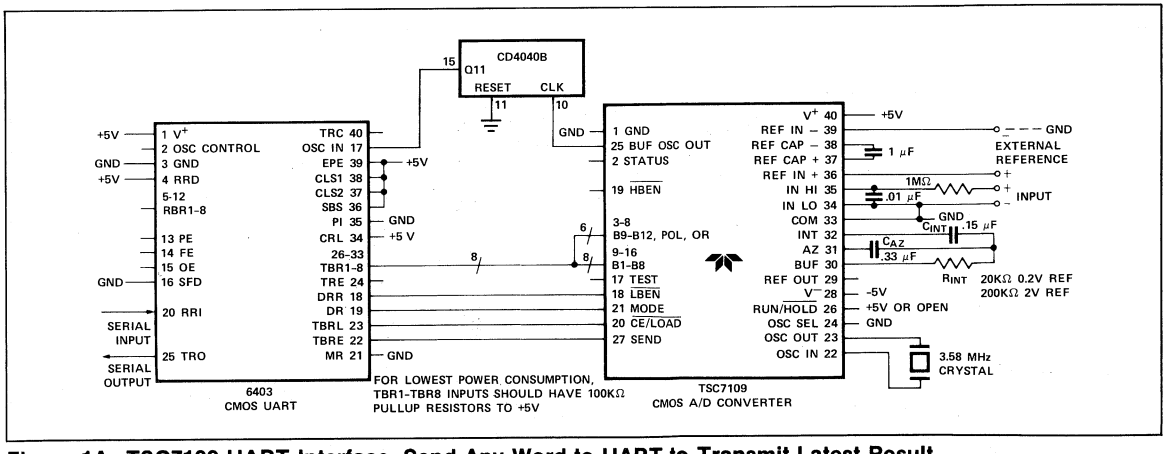


Figure 1A: TSC7109 UART Interface. Send Any Word to UART to Transmit Latest Result.

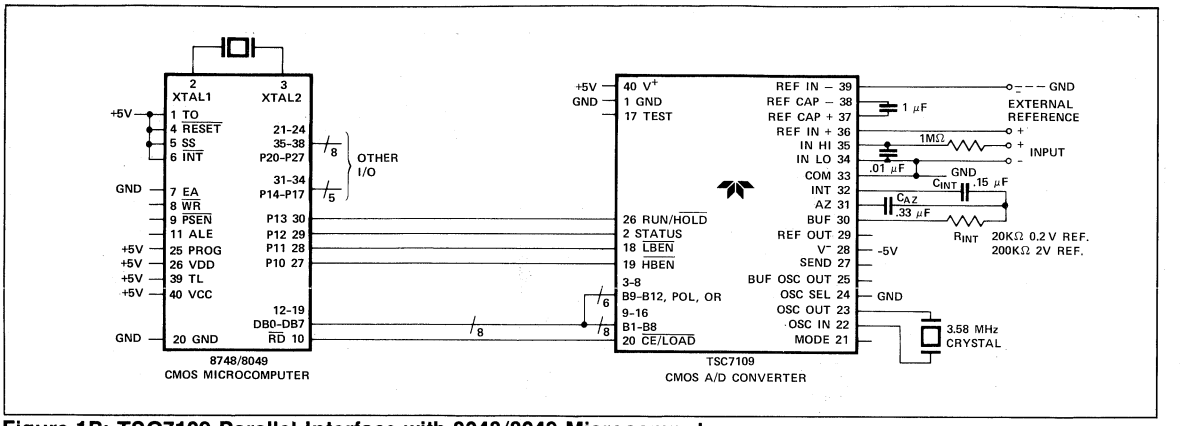


Figure 1B: TSC7109 Parallel Interface with 8048/8049 Microcomputer

Detailed Description

Analog Section

Figure 2 shows a block diagram of the Analog Section of the TSC7109. The circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle), when the RUN/HOLD input is left open or connected to V^+. Each measurement cycle is divided into three phases as shown in Figure 3. They are: (1) Auto-Zero (AZ), (2) Signal Integrate (INT), (3) Reference Deintegrate (DE).

Auto-Zero Phase

The buffer and the integrator inputs are disconnected from input high and input low and connected to analog common. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor, C_{AZ}, to compensate for offset voltage in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. The offset referred to the input is less than 10 μV.

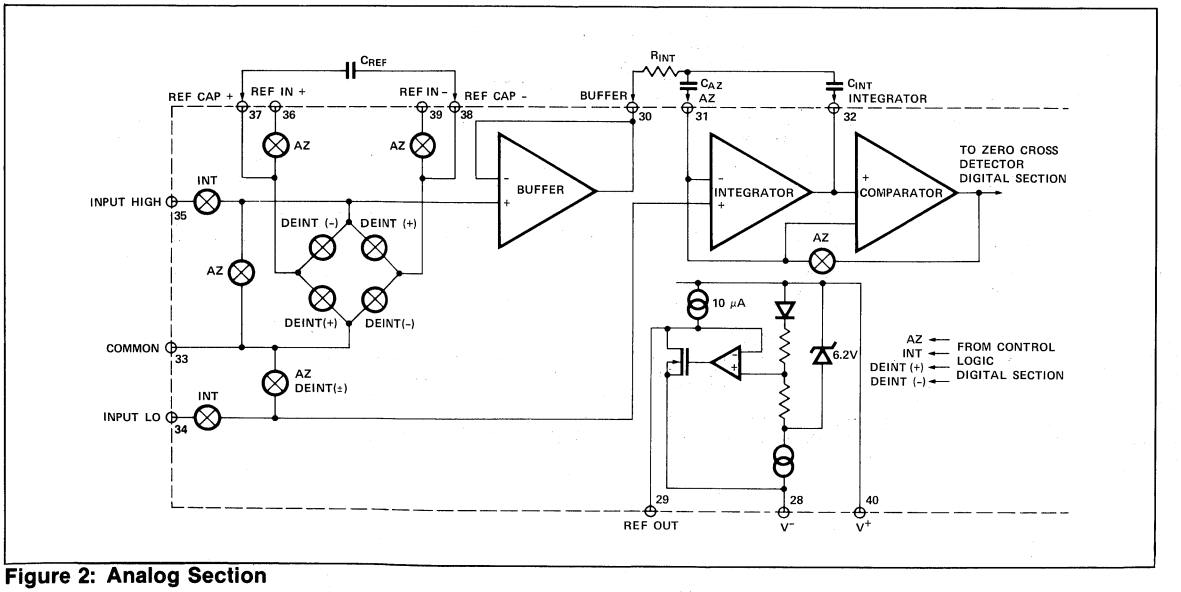


Figure 2: Analog Section

Signal Integrate Phase

The buffer and integrator inputs are removed from COMMON and connected to input high and input low. The auto-zero loop is opened. The auto-zero capacitor is placed in series in the loop to provide an equal and opposite compensating offset voltage. The differential voltage between input high and input low is integrated for a fixed time of 2048 clock periods. At the end of this phase, the polarity of the integrated signal is determined. If the input signal has no return to the converter power supply, input low can be tied to analog common to establish the correct common-mode voltage.

De-Integrate Phase

Input high is connected across the previously charged reference capacitor and input low is internally connected to analog common. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to the zero crossing (established by AUTO-ZERO) with a fixed slope. The time, represented by the number of clock periods counted for the output to return to zero, is proportional to the input signal.

Differential Input

The TSC7109 has been optimized for operation with analog-common near digital ground. With +5 V and -5 V power supplies, a full ±4 V full-scale integrator swing maximizes the analog section's performance.

A typical CMRR of 86 dB is achieved for input differential voltages anywhere within the common-mode range of 0.5 volts below the positive supply to 1.0 volts above the negative supply. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition is near a full-scale negative differential input voltage with a large positive common-mode voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. In such cases, the integrator swing can be reduced to less than the recommended ±4 V full-scale value, with some loss of accuracy. The integrator output can swing to within 0.3 volts of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. Rollover voltage is the main source of common-mode error. It is caused by the reference capacitor losing or gaining charge due to stray capacity on its modes. With a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal and lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for (+) or (-) input voltage will cause a roll-over error. This error can be held to less than 0.5 count worst case by using a large reference capacitor in comparision to the stray capacitance. To minimize roll-over error from these above sources keep the reference common-mode voltage near or at analog common.

Digital Section

The digital section is shown in block diagram Figure 4 and includes the clock oscillator and scaling circuit, a 12-bit binary counter with output latches and TTL-compatible three-state output drivers, UART handshake logic, polarity, overrange and control logic. Logic levels are referred to as "low"or "high". The actual logic levels are defined in Table 1 "Operating Characteristics."

Inputs driven from TTL gates should have 3-5 k pullup resistors added for maximum noise immunity. For minimum power consumption, all inputs should swing from GND (low) to V^+(high).

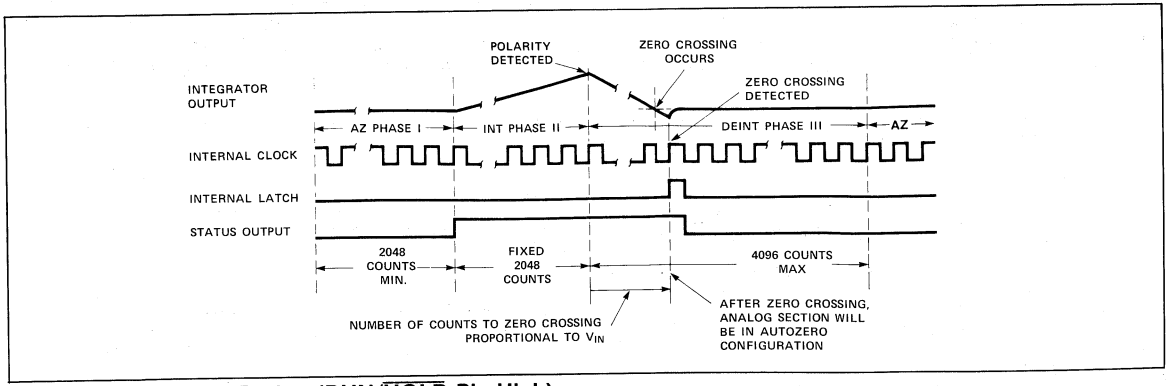


Figure 3: Conversion Timing (RUN/HOLD Pin High)

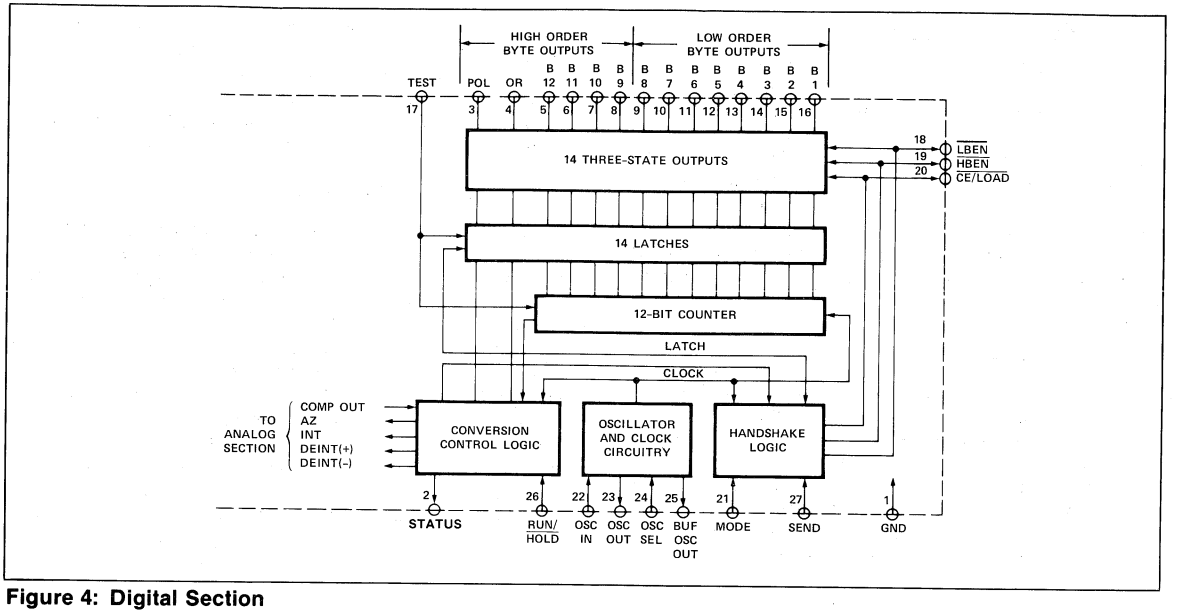


Figure 4: Digital Section

STATUS Output

During a conversion cycle, the STATUS output goes high at the beginning of Signal Integrate and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 3. The signal may be used as a "data valid" flag to drive interrupts, or for monitoring the status of the converter. (Data will not change while STATUS is low).

MODE Input

The output mode of the converter is controlled by the MODE input. The converter is in its "Direct" output mode, when the MODE pin is low or left open. The output data is directly accessible under the control of the chip and byte enable inputs (this input is provided with a pulldown resistor to ensure a low level when the pin is left open). When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in two bytes, then returns to "direct" mode. When the MODE input is kept high, the converter will output data in the handshake mode at the end of every conversion cycle with MODE = 0 (Direct BUS Transfer) the send input should be tied to V^+. (See Handshake Mode Section).

RUN/$\overline{\text{HOLD}}$ Input

With RUN/$\overline{\text{HOLD}}$ high or open, the circuit operates normally as a dual slope A/D as shown in Figure 3. Conversion cycles operate continuously with the output latches updated after zero crossing in the de-integrate mode. An internal pullup resistor is provided to insure a high level with an open input.

The RUN/$\overline{\text{HOLD}}$ may be used to shorten conversion time. If the RUN/$\overline{\text{HOLD}}$ goes low at anytime after zero crossing in the de-integrate mode, the circuit will jump to auto-zero and eliminate that portion of time normally spent in de-integrate.

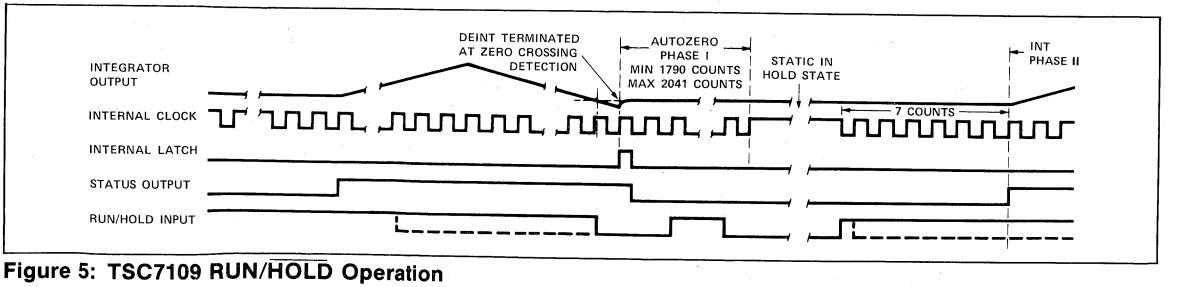


Figure 5: TSC7109 RUN/$\overline{\text{HOLD}}$ Operation

If RUN/$\overline{HOLD}$ stays or goes low the conversion will complete with minimum time in de-integrate. It will stay in auto-zero for the minimum time and wait in auto-zero for a high in the RUN/$\overline{HOLD}$ input. As shown in Figure 5, the STATUS output will go high seven clock periods after RUN/$\overline{HOLD}$ is changed to high, and the converter will begin the integrate phase of the next conversion.

The RUN/$\overline{HOLD}$ input allows controlled conversion interface. The converter may be held at idle in auto-zero with RUN/HOLD low. The conversion is started when RUN/$\overline{HOLD}$ goes high and the new data is valid when the STATUS output goes low (or is transferred to the UART — see Handshake Mode.) RUN/$\overline{HOLD}$ may now go low, terminating de-integrate and ensuring a minimum auto-zero time before stopping to wait for the next conversion. Conversion time can be minimized by ensuring RUN/$\overline{HOLD}$ goes low during de-integrate, after zero crossing, and goes high after the hold point is reached. The required activity on the RUN/$\overline{HOLD}$ input can be provided by connecting it to the Buffered Oscillator output. In this mode, the input value measured determines the conversion time.

Direct Mode

The data outputs (bits 1 through 8 low order byte, bits 9 through 12, polarity and overrange high order byte) are accessible under control of the byte and chip enable terminals as inputs with the MODE pin at a low level. These three inputs are all active low. Internal pullup resistors are provided for an inactive high level when left open. When the chip enable input is low, a byte enable input low will allow the outputs of that byte to become active. A variety of parallel data accessing techniques may be used, as shown in the section entitled "Interfacing." (See Figure 6 and Table 3)

The access of data should be synchronized with the conversion cycle by monitoring the STATUS output. This will prevent accessing the data while it is being updated and eliminate the acquisition of erroneous data.

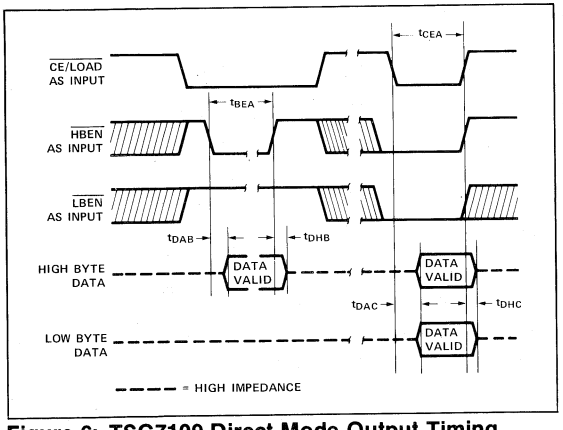


Figure 6: TSC7109 Direct Mode Output Timing

Symbol	Description	Min.	Typ.	Max.	Units
t_{BEA}	Byte Enable Width	200	500		ns
t_{DAB}	Data Access Time from Byte Enable		150	300	ns
t_{DHB}	Data Hold Time from Byte Enable		150	300	ns
t_{CEA}	Chip Enable Width	300	500		ns
t_{DAC}	Data Access Time from Chip Enable		200	400	ns
t_{DHC}	Data Hold Time from Chip Enable		200	400	ns

Table 3. TSC7109 Direct Mode Timing Requirements

Handshake Mode

An alternative means of interfacing the TSC7109 to digital systems is provided when the handshake output mode of the TSC7109 becomes active in controlling the flow of data instead of passively responding to chip and byte enable inputs. This mode allows a direct interface between the TSC7109 and industry-standard UART's with no external logic required. The TSC7109 provides all the control and flag signals necessary to sequence the two bytes of data into the UART and initiate their transmission in serial form when triggered into the handshake mode. The cost of designing remote data acquisition stations is reduced using serial data transmission to minimize the number of lines to the central controlling processor.

The MODE pin controls the handshake mode. When the MODE terminal is held high, the TSC7109 will enter the handshake mode after new data has been stored in the output latches at the end of every conversion performed (see Figures 7 and 8). Entry into the handshake mode may be triggered on demand by the MODE terminal. At any time during the conversion cycle, the low to high transition of a short pulse at the MODE input will cause immediate entry into the handshake mode. If this pulse occurs while new data is being stored, the entry into handshake mode is delayed until the data is stable. The MODE input is ignored in the handshake mode, and until the converter completes the output cycle and clears the handshake mode data updating will be inhibited (see Figure 9).

When the MODE input is high or when the converter enters the handshake mode, the chip and byte enable terminals become TTL-compatible outputs which provide the output cycle control signals (see Figures 7,8 and 9).

The SEND input is used by the converter as an indication of the ability of the receiving device (such as a UART) to accept data in the handshake mode. The sequence of the output cycle with SEND held high is shown in Figure 7. The handshake mode (internal MODE high) is entered after the data latch pulse (the $\overline{CE}$/$\overline{LOAD}$, $\overline{LBEN}$ and $\overline{HBEN}$ terminals are active as outputs since MODE remains high).

The high level at the SEND input is sensed on the same high to low internal clock edge. On the next low to high internal clock edge the high-order byte (bits 9 through 12, POL, and OR) outputs are enabled and the $\overline{CE}$/$\overline{LOAD}$ and the $\overline{HBEN}$

outputs assume a low level. The $\overline{CE}/\overline{LOAD}$ output remains low for one full internal clock period only; the data outputs remain active for 1-1/2 internal clock periods; and the high byte enable remains low for two clock periods. The $\overline{CE}/\overline{LOAD}$ output low level or low to high edge may be used as a synchronizing signal to ensure valid data, and the byte enable as an output may be used as a byte identification flag. With SEND remaining high the converter completes the output cycle using $\overline{CE}/\overline{LOAD}$ and $\overline{LBEN}$ while the low order byte outputs (bits 1 through 8) are activated. When both bytes are sent the handshake mode is terminated. The typical UART interfacing timing is shown in Figure 8. The SEND input is used to delay portions of the sequence, or handshake to ensure correct data transfer. This timing diagram shows an industry-standard HD6402 or CDP1854 CMOS UART to interfacing serial data channels. The SEND input to the TSC7109 is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the $\overline{CE}/\overline{LOAD}$ terminal of the TSC7109 drives the TBRL (Transmitter Buffer Register Load) input to the UART. The eight transmitter Buffer Register inputs accept the parallel data outputs. With the UART Transmitter Buffer Register empty, the SEND input will be high when the handshake mode is entered after new data is stored. The high order byte outputs become active and the $\overline{CE}/\overline{LOAD}$ and $\overline{HBEN}$ terminals will go low after SEND is sensed. When $\overline{CE}/\overline{LOAD}$ goes high at the end of one clock period, the high order byte data is clocked into the UART Transmitter Buffer Register. The UART TBRE output will go low, which halts the output cycle with the $\overline{HBEN}$ output low, and the high order byte outputs active. When the UART has transferred the data to the Transmitter Register and cleared the Transmitter Buffer Register, the TBRE returns high. The high order byte outputs are disabled on the next TSC7109 internal clock high to low edge, and one-half internal clock later, the $\overline{HBEN}$ output returns high. The $\overline{CE}/\overline{LOAD}$ and $\overline{LBEN}$ outputs go low at the same time as the low order byte outputs become active. When the $\overline{CE}/\overline{LOAD}$ returns high at the end of one clock period, the low order data is clocked into the UART Transmitter Buffer Register, and TBRE again goes low. The next TSC7109 internal clock high to low edge will sense when TBRE returns to a high, disabling the data outputs. One-half internal clock later, the handshake mode is cleared, and the $\overline{CE}/\overline{LOAD}$, $\overline{HBEN}$ and $\overline{LBEN}$ terminals return high and stay active, if MODE still remains high.

Handshake output sequences may be performed on demand by triggering the converter into handshake mode with a low to high edge on the MODE input. A handshake output sequence triggered is shown in Figure 9. The SEND input is low when the converter enters handshake mode. The whole output sequence is controlled by the SEND input, and the sequence for the first (high order) byte is similar to the sequence for the second byte.

This diagram also shows that the output sequence takes longer than a conversion cycle. New data will not be latched when the handshake mode is still in progress and is therefore lost.

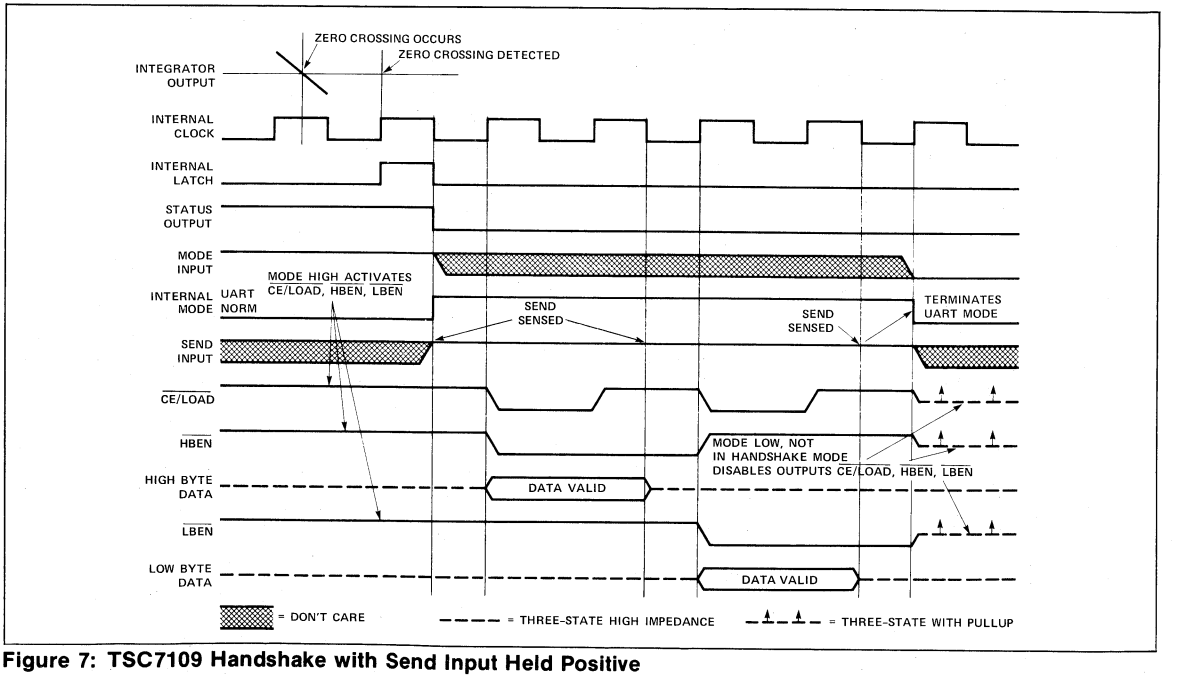


Figure 7: TSC7109 Handshake with Send Input Held Positive

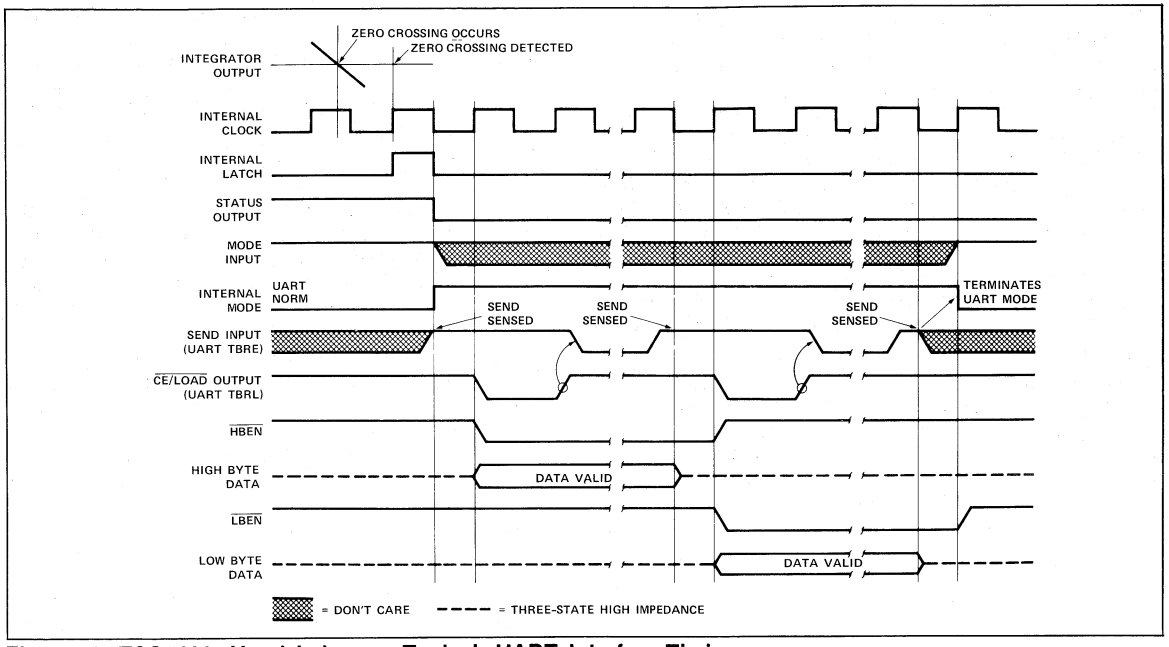


Figure 8: TSC7109 Handshake — Typical UART Interface Timing

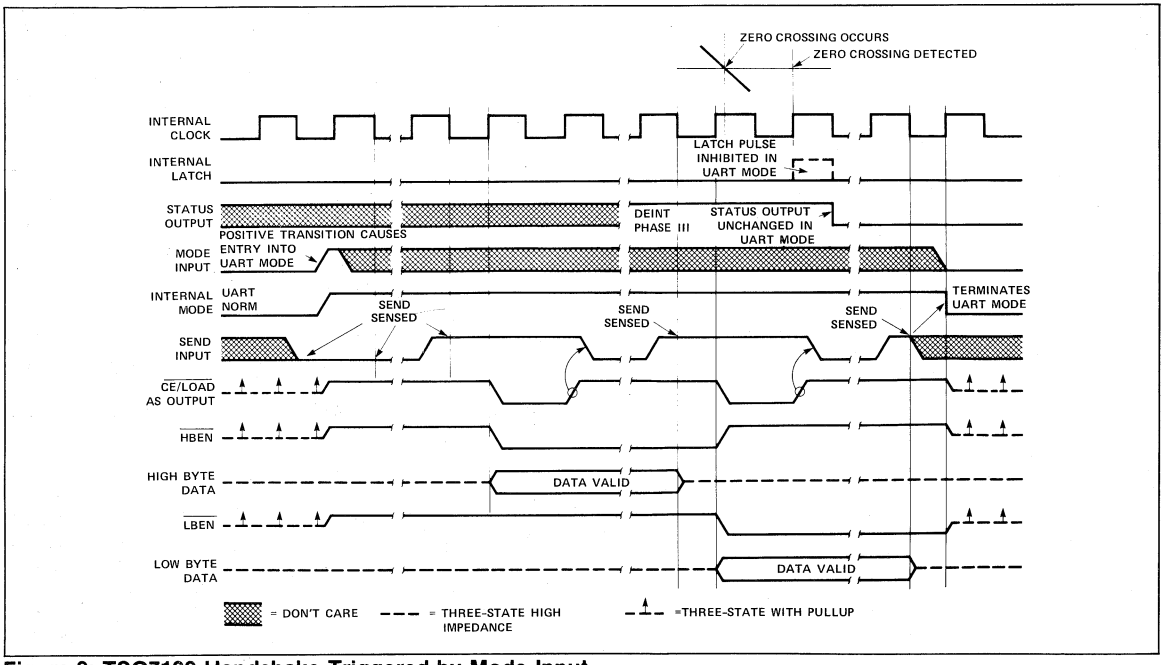


Figure 9: TSC7109 Handshake Triggered by Mode Input

Oscillator

The oscillator may be overdriven, or may be operated as an RC or crystal oscillator. The OSCILLATOR SELECT input optimizes the internal configuration of the oscillator for RC or crystal operation. The OSCILLATOR SELECT input is provided with a pullup resistor. When the OSCILLATOR SELECT input is high or left open, the oscillator is configured for RC operation. The internal clock will be the same frequency and phase as the signal at the BUFFERED OSCILLATOR OUTPUT. Connect the resistor and capacitor as in Figure 10. The circuit will oscillate at a frequency given by f = 0.45/RC. a 100 k resistor is recommended for useful ranges of frequency. The capacitor value should be chosen such that 2048 clock periods are close to an integral multiple of the 60 Hz period for optimum 60 Hz line rejection.

With OSCILLATOR SELECT input low, two on-chip capacitors and a feedback device are added to the oscillator. In this configuration, the oscillator will operate with most crystals in the 1 to 5 MHz range with no external components (Figure 11). The OSCILLATOR SELECT input low inserts a fixed ÷58 divider circuit between the BUFFERED OSCILLATOR OUTPUT and the internal clock. A 3.58 MHz TV crystal gives a division ratio providing an integration time given by:

$$T = (2048 \text{ clock periods}) \frac{58}{3.58 \text{ MHz}} = 33.18 \text{ ms}$$

The error is less than one percent from two 60 Hz periods or 33.33 ms which will give better than 40 dB, 60 Hz rejection. The converter will operate reliably at conversion rates of up to 30 per second, corresponding to a clock frequency of 245.8 kHz.

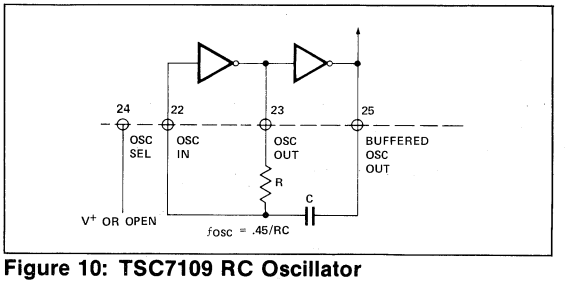


Figure 10: TSC7109 RC Oscillator

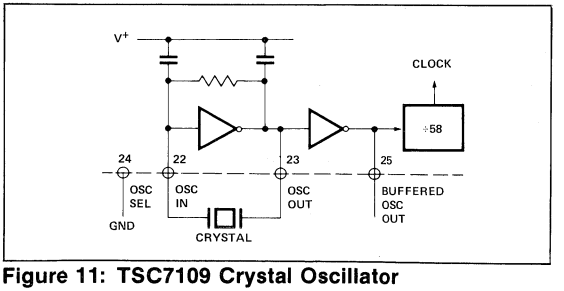


Figure 11: TSC7109 Crystal Oscillator

When the oscillator is to be overdriven, the OSCILLATOR OUTPUT should be left open, and the overdriving signal should be applied at the OSCILLATOR INPUT. The internal clock will be of the same duty cycle, frequency and phase as the input signal. When the OSCILLATOR SELECT is at GND, the clock will be 1/58 of the input frequency.

Test Input

The counter and its outputs may be tested easily. When the TEST input is connected to GND, the internal clock is disabled, and the counter outputs are all forced into the high state. When the input returns to the 1/2 (V^+ -GND) voltage or to V^+ and one clock is input, the counter outputs will all be clocked to the low state.

The counter output latched are enabled when the TEST input is taken to a level halfway between V^+ and GND allowing the counter contents to be examined anytime.

Component Value Selection

The integrator output swing for full-scale should be as large as possible. For example, with +5 V supplies and COMMON connected to GND, the nominal integrator output swing at full-scale is ±4 V. Since the integrator output can go to 0.3 V from either supply without significantly affecting linearity, a 4 V integrator output swing allows 0.7 V for variations in output swing due to component value and oscillator tolerances. With ±5 V supplies and a common-mode voltage range of ±1 V required, the component values should be selected to provide ±3 V integrator output swing. Noise and rollover errors will be slightly worse than in the ±4 V case. For large common-mode voltage ranges, the integrator output swing must be reduced further. This will increase both noise and rollover errors. To improve the performance, ±6 V supplies may be used.

Integrating Capacitor

The integrating capacitor C_{INT} should be selected to give the maximum integrator output voltage swing that will not saturate the integrator to within 0.3 volt from either supply. A ±3.5 to ±4 volt integrator output swing is nominal for the TSC7109 with ±5 volt supplies and analog common connected to GND. For 7-1/2 conversions per second (61.72 kHz internal clock frequency) nominal values C_{INT} and C_{AZ} are 0.15 μF and 0.33 μF, respectively. These values should be changed if different clock frequencies are used to maintain the integrator output voltage swing. The value of C_{INT} is given by:

$$C_{INT} = \frac{(2048 \times \text{Clock Period})\ (20\ \mu)}{\text{Integrator Output Voltage Swing}}$$

The integrating capacitor must have low dielectric absorption to prevent rollover errors. Polypropylene capacitors give undetectable errors at reasonable cost up to 85° C. Teflon® capacitors are recommended for the military temperature range. While their dielectric absorption characteristics vary somewhat between units, devices may be selected to less than 0.5 count of error due to dielectric absorption.

Integrating Resistor

The integrator and the buffer amplifier both have a class A output stage with 100 μA of quiescent current. They supply 20 μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 4.095 volt full-scale a 200 kΩ and for 409.6 mV full-scale a 20 kΩ are recommended. R_{INT} may be selected for other values of full-scale by:

$$R_{INT} = \frac{\text{Full-Scale Voltage}}{20\ \mu A}$$

Auto-Zero Capacitor

As the auto-zero capacitor is made large the system noise is reduced. Since it is in parallel with the integrating capacitor, it forms an RC time constant that determines the error that exists at the end of an auto-zero cycle and speed of recovery from overloads. For 4.096 V full-scale where recovery is most important, a value of C_{AZ} equal to half of C_{INT} should be used.

For 409.6 mV full-scale where noise is very important and the integrating resistor is small, use a value of C_{AZ} twice C_{INT}. The inner foil of C_{AZ} should be connected to pin 31 and the outer foil to the RC summing junction. The inner foil of C_{INT} should be connected to the RC summing junction and the outer foil to pin 32 for best rejection of the stray pickup. For low leakage at temperatures above 85°C use Teflon® capacitors.

Reference Capacitor

A 1 μF capacitor is recommended for most circuits. However, where a large common-mode voltage exists a larger value is required to prevent rollover error (for example: the reference low is not analog common) and a 409.6 mV scale is used. The rollover error will be held to 0.5 count with a 10 μF capacitor. For temperatures above 80°C use Teflon® or equivalent capacitors for their low leakage characteristics.

Reference Voltage

To generate full-scale output of 4096 counts the analog input required is $V_{IN} = 2\ V_{REF}$. For a 4.096 V full-scale use a reference of 2.048 V. In many applications where the A/D is connected to a transducer, there will exist a scale factor between the input voltage and the digital reading. For instance, in a measuring system, the designer might like to have a full-scale reading when the voltage from the transducer is 700 mV. Instead of dividing the input down to 409.6 mV, the designer should use the input voltage directly and select V_{REF} = 350 mV. Suitable values for integrating resistor and capacitor would be 34 k and 0.15 μF. This makes the system slightly quieter and also avoids a divider network on the input. Another advantage of this system occurs when temperature and weight measurements with an offset or tare are desired for non-zero input. The offset may be introduced by connecting the voltage output of the transducer between common and analog high, and the offset voltage between common and analog low, observing polarities carefully. In processor-based systems using the TSC7109, it may be more desirable to use software and perform this type of scaling or tare subtraction digitally.

Reference Sources

A major factor in the absolute accuracy of the converter is the stability of the reference voltage. The 12-bit resolution of the TSC7109 is one part in 4096, or 244 ppm. Thus, for the on-board reference temperature coefficient of 80 ppm/°C a temperature difference of 3°C will introduce a one-bit absolute error. Where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made it is recommended that an external high-quality reference be used.

A Reference Output (pin 29) is provided which may be used with a resistive divider to generate a suitable reference voltage. 20 mA may be sunk without significant variation in output voltage. A pullup bias device is provided which sources about 10 μA. The output voltage is nominally 2.8 V below V^+. When using the on-board reference, Ref Out (pin 29) should be connected to Ref — (Pin 39), and Ref + should be connected to the wiper of a precision potentiometer between Ref Out and V^+. The test circuit shows the circuit for a 204.8 mV reference, generated by a 2 kΩ precision potentiometer in series with a 24 kΩ fixed resistor.

8

Interfacing

Direct Mode

Combinations of chip enable and byte enable control signals which may be used when interfacing the TSC7109 to parallel data lines as shown in Figure 12. The $\overline{CE}/\overline{LOAD}$ input may be tied low, allowing either byte to be controlled by its own enable (Figure 12A). Figure 12B shows the $\overline{HBEN}$ and $\overline{LBEN}$ as flag inputs, and $\overline{CE}/\overline{LOAD}$ as a master enable, which could be the READ strobe available from most microprocessors. Figure 12C shows a configuration where the two byte enables are connected together. The $\overline{CE}/\overline{LOAD}$ is a chip enable, and the $\overline{HBEN}$ and $\overline{LBEN}$ may be used as a second chip enable or connected to ground. The 14 data outputs will be enabled at the same time. In the direct MODE, SEND should be tied to V^+.

Figure 13 interfaces several TSC7109's to a bus, ganging the $\overline{HBEN}$ and $\overline{LBEN}$ signals to several converters together, and using the $\overline{CE}/\overline{LOAD}$ inputs to select the desired converter.

Figures 14-19 give practical circuits utilizing the parallel tri-state output capabilities of the TSC7109. Figure 14 shows parallel interface to the intel MCS-48, -80 and -85 systems via an 8255 PPI, where the TSC7109 data outputs are active at all times. The 8155 I/O ports may be used in an identical manner. This interface can be used in an identical manner. This interface can be used in a read-after-update sequence, as shown in Figure 15. The data is accessed by the high to low transition of the STATUS driving an interrupt to the microprocessor.

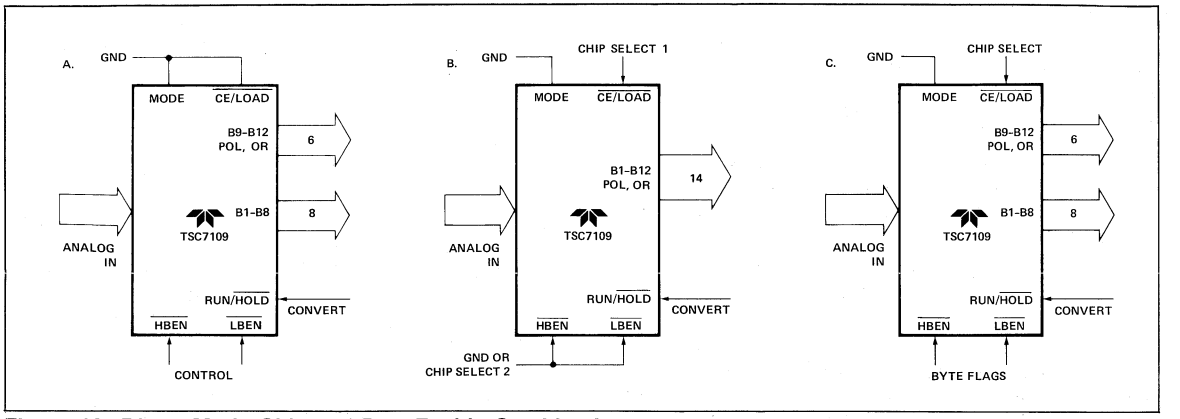


Figure 12: Direct Mode Chip and Byte Enable Combinations

The RUN/$\overline{\text{HOLD}}$ input is also used to initiate conversions under software control. Figure 16 gives an interface to Motorola MC6800 or MOS technology MCS650X systems.

An interrupt is generated through the control Resistor B, CB1 line from the high to low transition of the STATUS output. The RUN/$\overline{\text{HOLD}}$ pin is controlled by CB2 through Control Register B, allowing software control of conversions.

Direct interfacing to most microprocessor busses is easily accomplished through the tri-state output of the TSC7109.

Figures 1B, 17 and 18 are typical connection diagrams. To be sure that requirements for setup and hold times, minimum pulse widths, and the drive limitations on long busses are met, it is necessary to carefully consider the system timing in this type of interface. This type of interface is used when the memory peripheral address density is low providing simply address decoding. Interrupt handling can be simplified by using an interface to reduce the component count.

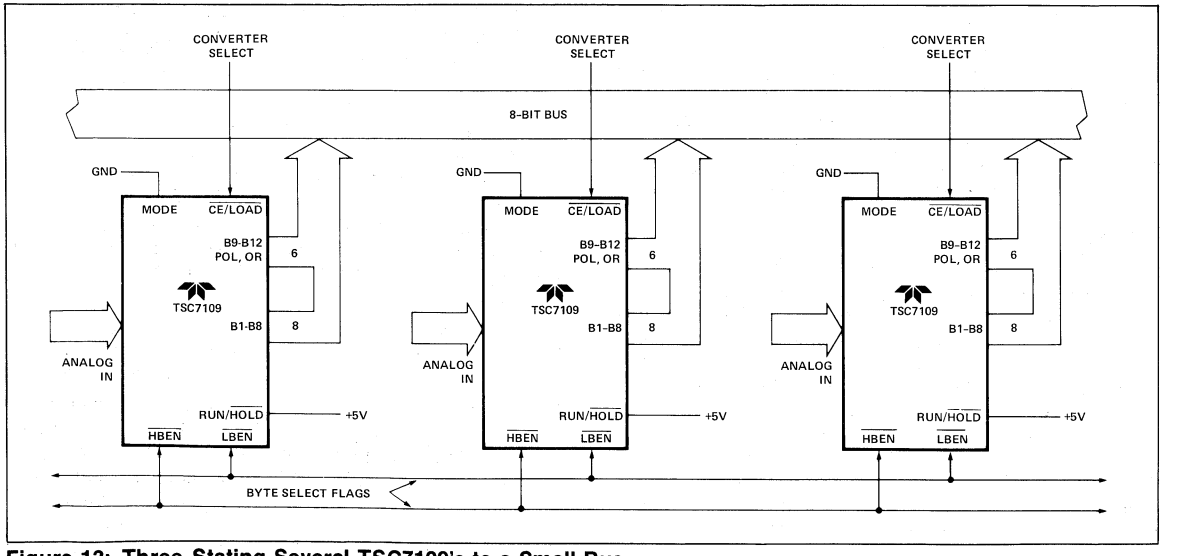


Figure 13: Three-Stating Several TSC7109's to a Small Bus

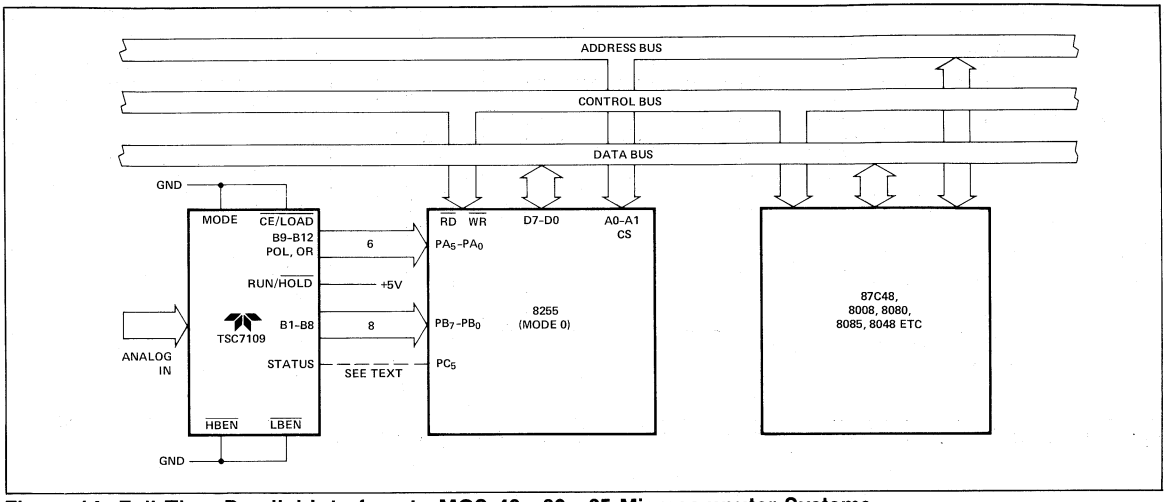


Figure 14: Full-Time Parallel Interface to MCS-48, -80, -85 Microcomputer Systems

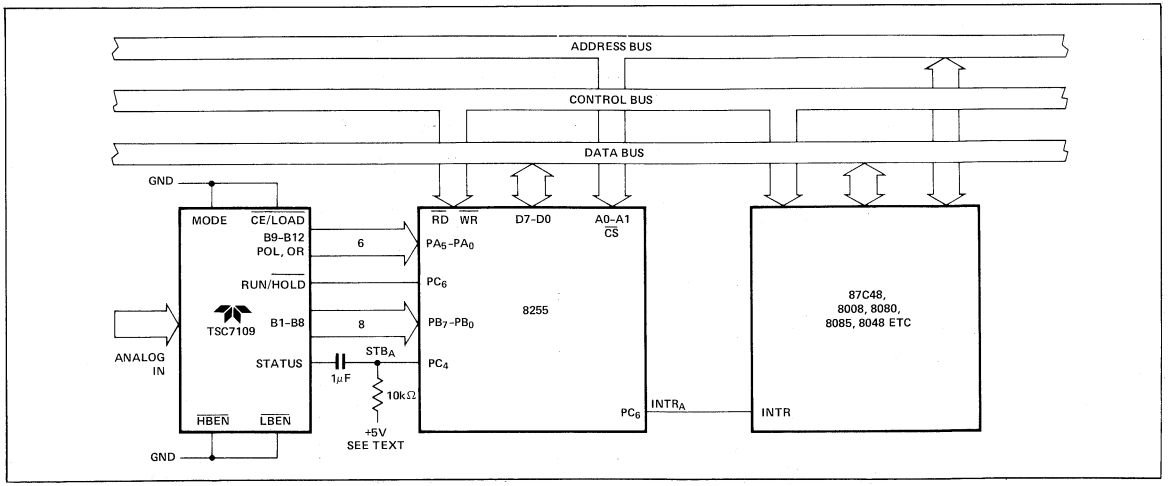


Figure 15: Full-Time Parallel Interface to MCS-48, -80, -85 Microcomputers with Interrupt

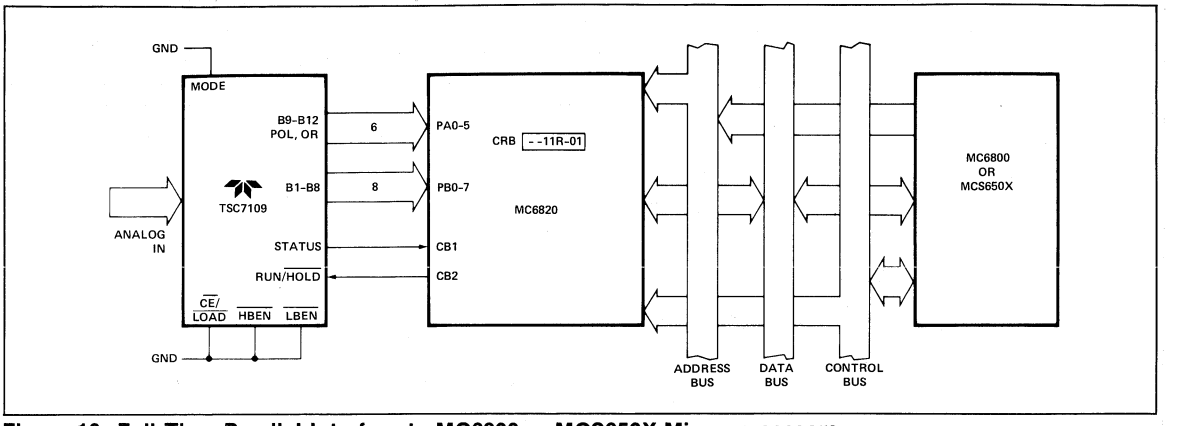


Figure 16: Full-Time Parallel Interface to MC6800 or MCS650X Microprocessors

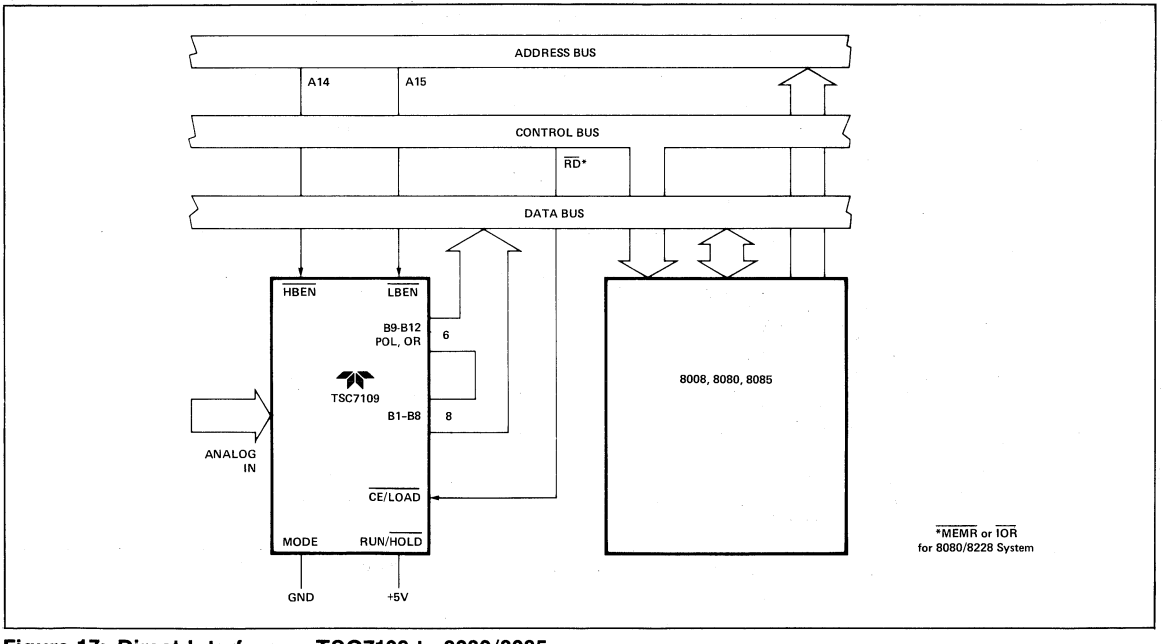


Figure 17: Direct Interface — TSC7109 to 8080/8085

Handshake Mode

The handshake mode provides an interface to a wide variety of external devices. The byte enables may be used as byte identification flags or as load enables and external latches may be clocked by the rising edge of $\overline{CE}/\overline{LOAD}$. A handshake interface to Intel microprocessors using an 8255 PPI as shown in Figure 19. The handshake operation with the 8255 is controlled by inverting its Input Buffer Full (IBF) flag to drive the SEND input to the TSC7109, and using the $\overline{CE}/\overline{LOAD}$ to drive the 8255 strobe. The internal control register of the PPI should be set in MODE 1 for the port used. If the 8255 IBF flag is low and the TSC7109 is in handshake mode the next word will be strobed into the port. The strobe will cause IBF to go high (SEND goes low), which will keep the enabled byte outputs active. The PPI will generate an interrupt which when executed will result in the data being read. The IBF will be reset low when the byte is read causing the TSC7109 to sequence into the next byte. The MODE input to the TSC7109 is connected to the control line on the PPI.

The data from every conversion will be sequenced in two bytes in the system, if this output is left high, or tied high separately. (The data access must take less time than a conversion). The output sequence can be obtained on demand if this output is made to go from low to high and the interrupt may be used to reset the MODE bit.

Conversions may be obtained on command under software control by driving the RUN/$\overline{HOLD}$ input to the TSC7109 by a bit of the 8255. Another peripheral device may be serviced by the unused port of the 8255. The 8155 may be used in a similar manner. The MCS650X microprocessors are shown in Figure 20 with MODE and RUN/$\overline{HOLD}$ tied high to save port outputs.

The handshake mode is particularly useful for directly interfacing to industry standard UARTs (such as Western Digital TR1602) providing a means of serially transmitting converted data with minimum component count.

A typical UART connection is shown in Figure 1A. In this circuit, any word received by the UART causes the UART DR (Data Ready) output to go high. The MODE input to the TSC7109 goes high, triggering the TSC7109 into handshake mode. The high order byte is output to the UART and when the UART has tranferred the data to the Transmitter Register, TBRE (SEND) goes high again, $\overline{LBEN}$ will go high, driving the UART DRR (Data Ready Reset) which will signal the end of the transfer of data from the TSC7109 to the UART.

An extension of the Typical Connection to several TSC7109's with one UART is shown in Figure 21. In this circuit, the word received by the UART (available at the RBR outputs when DR is high) is used to select which converter will handshake with the UART. Up to eight TSC7109's may interface with one UART, with no external components. Up to 256 converters may be accessed on one serial line with additional components.

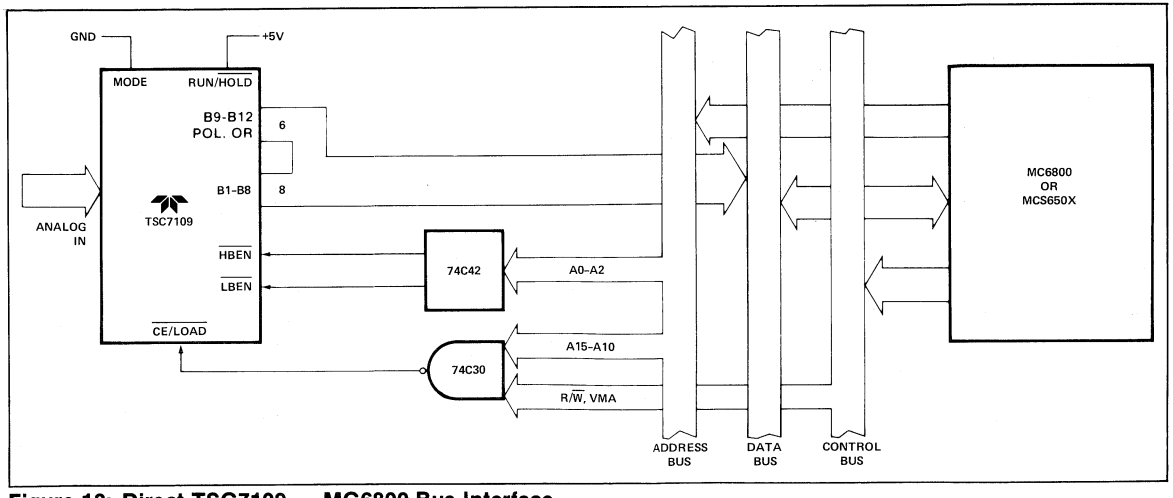


Figure 18: Direct TSC7109 — MC6800 Bus Interface

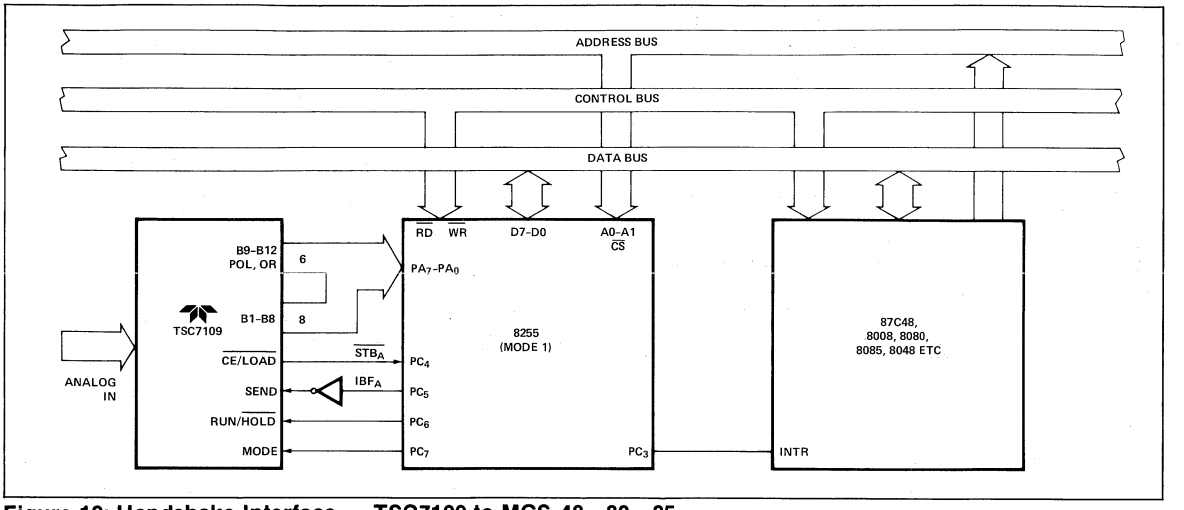


Figure 19: Handshake Interface — TSC7109 to MCS-48, -80, -85

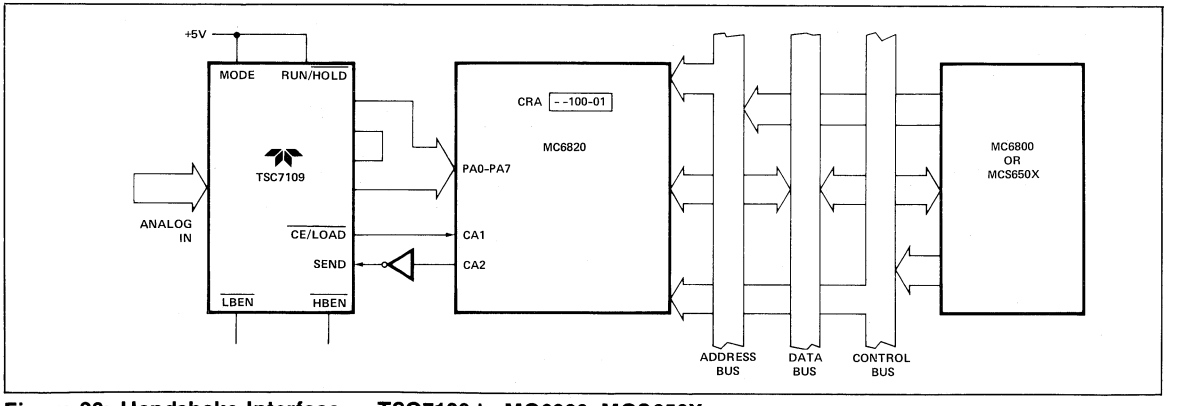


Figure 20: Handshake Interface — TSC7109 to MC6800, MCS650X

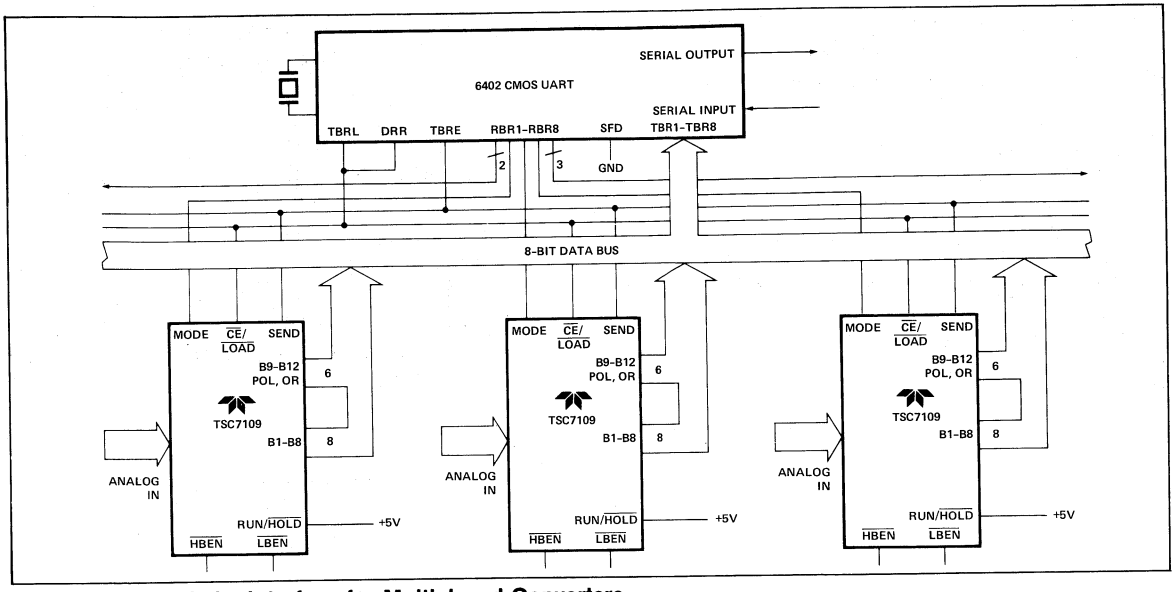


Figure 21: Handshake Interface for Multiplexed Converters

Integrating Converter Features

The output of Integrating A/D converters represents the integral or average of an input voltage over a fixed period of time. Compared with techniques in which the input is sampled and held, the integrating converter will average the effects of noise. A second important characteristic is that time is used to quantise the answer, resulting in extremely small non-linearity errors and no missing output codes. The integrating converter also has very good rejection of frequencies whose periods are an integral multiple of the measurement period. This feature can be used to advantage in reducing line frequency noise. (Figure 22)

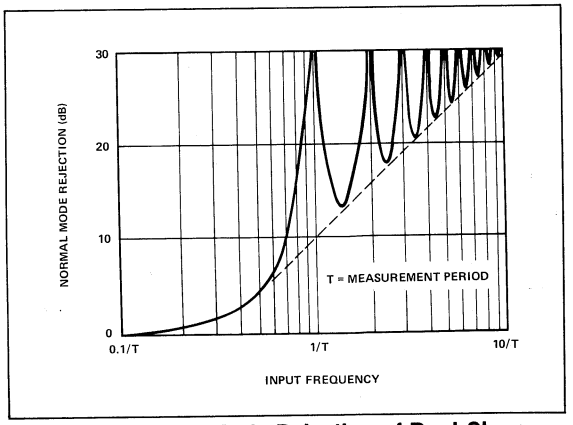
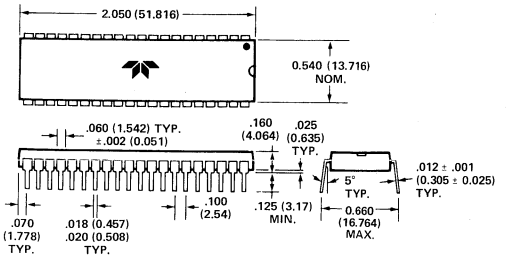


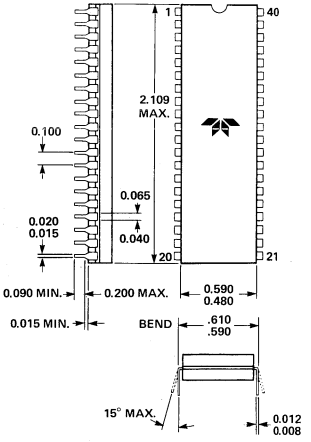
Figure 22: Normal Mode Rejection of Dual-Slope Converter as a Function of Frequency.

Package Information

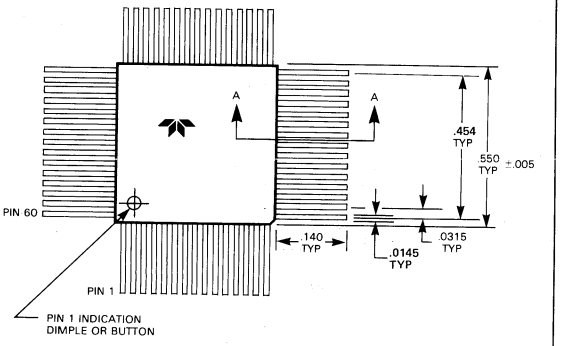
40-Pin Plastic Dual-In-Line Package
(Package #17)



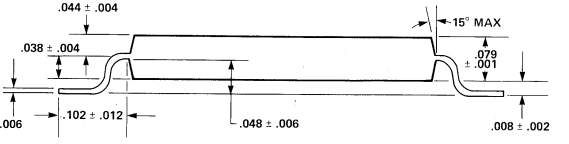
40-Pin CerDIP
(Package #20)



60-Pin Plastic Flat Package



"SQ" Package — Unformed Leads
(Package #22)



"BQ" Package — Formed Leads
(Package #21)

TELEDYNE SEMICONDUCTOR

TSC800
15-Bit Plus Sign Integrating Analog to Digital Converter
• BUS Compatible
• UART Interface

General Description

The TSC800 is a 15-bit plus sign integrating analog to digital converter. The TSC800 improves the conventional two cycle dual slope conversion cycle by incorporating system zero and integrator output zero phases. Offset error sources are automatically zeroed and overrange recovery time is reduced. The integrating conversion technique is immune to the noise spikes that introduce conversion errors in successive approximation converters.

The externally adjustable clock allows integration periods which are integral multiples of 50 Hz or 60 Hz for maximum power-line noise rejection. By using the 2.4576 MHz crystal oscillator mode (2.5 CONV/SEC) 50, 60 and 400 Hz signals are rejected.

Micro-processor interface signals support single byte (16-bit) or two byte (8-bit) parallel data transfers. A "handshake" operating mode supports serial data transmission via a UART. A serial count output is derivable by gating the clock signal with data valid (DVD). The count output pulses may be used in serial fiber optic transmission systems.

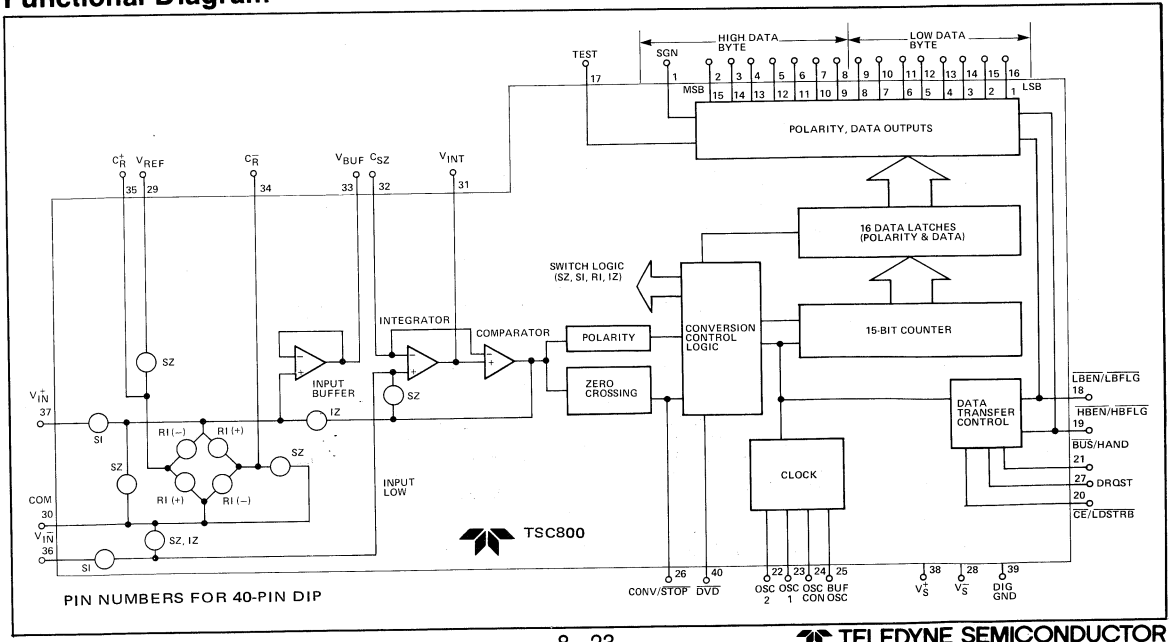
The high impedance differential inputs, 5 pA input leakage current, 16-bit dynamic range and interface control signals make the high resolution TSC800 the ideal analog to digital converter for process control, data logging and "intelligent" measurement systems.

Features

- 15 Bit Resolution Plus Sign Bit
  - 96 dB Dynamic Range
- Integrating Dual Slope Converter
  - Monotonic
  - Eliminate 50/60 Hz "Line" Interference
  - High Noise Immunity
  - Auto Zero Cycle Eliminates Trimming
  - Incorporates Integrator Zero Cycle for Fast Overload Recovery
- Three State Data Bit/Sign Outputs
  - 8 or 16 Bit Parallel Data Transfer to μ-Processor Bus
- UART Control Signals
  - Serial Data Transmission
  - "Handshake" Data Transfer
  - Distributed Control Systems
  - Fiber Optic Transmission Systems
- Easy Conversion Cycle Monitoring and Control
  - Data Valid Output Signal
  - Continuous or Convert on Command Operation
- High Impedance Differential Input
  - 15 pA Maximum Input Current
- Low Input Noise
  - 15 μ V_{p-p}
- On Chip Crystal Oscillator for 2.5 Conversions/Sec.
  - f_{xtal} = 2.4576 MHz
  - 100 mSEC Integration Period Rejects 50, 60, 400 Hz Interference Signals
- Convenient ±5 V Supply Operation
  - Low Power Dissipation ..... 20 mW
- Static Discharge Protected Inputs
- Available in 60-Pin Flat Package

8

Functional Diagram



Absolute Maximum Ratings[2]

Positive Supply Voltage (V_S^+ to Gnd) ..... +6.2 V
Negative Supply Voltage (V_S^- to Gnd) ..... -9.0 V
Analog Input Voltage (V^+_{IN} or V_{IN}^-) ..... V_S^+ to V_S^-
Voltage Reference Input (V_{REF}) ..... V_S^+ to V_S^-
Logic Input Voltage ..... V_S^+ + 0.3 V to Gnd - 0.3 V
Package Power Dissipation
CerDIP Package ..... 1 Watt @ +85° C
Plastic Package ..... 0.5 Watt @ +70° C
Ambient Operating Temperature Range
CerDIP Package (MJL) ..... -55° C to +125° C
(IJL) ..... -25° C to +85° C
Plastic Package (CPL, CBQ, CSQ) ... 0° C to +70° C
Storage Temperature ..... -55° C to 150° C
Lead Soldering Temperature (60 Seconds) ..... +300° C

Electrical Characteristics: V_S = ±5 V, Conversion Rate = 2.5 CONV/SEC, Crystal Frequency = 2.4576 MHz, T_A = 25° C, Full-Scale Voltage = 3.2768 V, Note 1.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC800 MIN	TSC800 TYP	TSC800 MAX	UNIT
ANALOG INPUT	1	V_{ZSE}	Zero-Scale Error	Vin = 0 V	—	—	±0.5	LSB
	2	NL	Non-Linearity	Best Straight Line - Full-Scale ≤ V_{IN} ≤ + Full-Scale	—	1.3	2	LSB
	3	NL	Nonlinearity	End Point - Full-Scale ≤ V_{IN} ≤ + Full-Scale	—	2.8	—	LSB
	4	DNL	Differential Nonlinearity		—	—	±0.5	LSB
	5	I_{IN}	Input Current	Vin = 0 V, T_A = 25° C 0° C ≤ T_A ≤ 70° C -25° C ≤ T_A ≤ 85° C -55° C ≤ T_A ≤ 125° C	— — — —	5 25 70 2.5	15 125 175 7.5	pA pA pA nA
	6	V_{CMR}	Common-Mode Input Range	Over Operating Temp. Range	V_S^- +1.5 V	—	V_S^+ -1.0 V	V
	7	CMRR	Common-Mode Rejection Ratio	Vin = 0 V Vcm = ±1 V	—	80	—	μV/V
	8	V_{FSTC}	Full-Scale Gain Temp. Coefficient	External Ref. Temperature Coefficient = 0 ppm/° C 0° C ≤ T_A ≤ 70° C	—	1.5	5	ppm/° C
	9	V_{ZSTC}	Zero-Scale Error Temp. Coefficient	Vin = 0 V 0° C ≤ T_A ≤ 70° C	—	0.8	2	μV/° C
	10	V_{SYE}	Full-Scale Magnitude Symmetry Error	Vin = 3.27 V	—	—	2	LSB
	11	E_N	Input Noise	Not exceeded 95% of time	—	15	—	μVpp
DIGITAL	12	t_{conv}	Conversion Speed		—	2.5	—	Conv/Sec
	13	V_{OH}	Output High Voltage	I_o = 100 μA	3.5	4.4	—	V
	14	V_{OL}	Output Low Voltage	I_o = 1.6 mA (Note 4)	—	0.18	0.4	V
	15	I_{OP}	Output Leakage Current	High Impedance State	—	0.1	1	μA
	16	I_{CP}	Control Pin Pullup Current	Pins 18, 19, 20 Pin 21 = 0 V, V_O = 2 V	—	5	—	μA
	17	V_{IH}	Input High Voltage	Pins 18-21, 26, 26	2.5 V	—	—	V

Electrical Characteristics: V_S = ±5 V, Conversion Rate = 2.5 CONV/SEC, Crystal Frequency = 2.4576 MHz, T_A = 25° C, Full-Scale Voltage = 3.2768 V, Note 1.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC800 MIN	TSC800 TYP	TSC800 MAX	UNIT
DIGITAL	18	V_{IL}	Input Low Voltage	Pins 18-21, 26, 27	—	—	1	V
	19	I_{IP}	Input Pin Pullup Current	Pins 26,27 V = 2 V	—	5	—	μA
	20	I_{IP}	Input Pin Pullup Current	Pin 17, 24 V = 2 V	—	25	—	μA
	21	I_{ID}	Input Pin Pulldown Current	Pin 21 V = 3 V	—	5	—	μA
	22	I_{OSCI}	Oscillator Output Current	V_O = 2.5 V	—	1.0	—	mA
	23	I_{BUFOSC}	Buffered Oscillator Output Current	V_O = 2.5 V	—	5	—	mA
	24	C_{IN}	Input Capacitance	Pin 18, 19	—	—	50	pF
	25	T_{PW}	$\overline{BUS}$/Hand Control Pin Minimum Pulse Width	Pin 21	70	—	—	ns
	26	T_{WBE}	Byte Enable Pulse width	Note 1	350	200	—	ns
	27	T_{WCE}	Chip Enable Pulse Width	Note 1	400	250	—	ns
	28	T_{ABE}	Byte Enable Access Time	Note 1	—	200	350	ns
	29	T_{ACE}	Chip Enable Access Time	Note 1	—	250	400	ns
	30	T_{DHB}	Data Hold From Byte Enable Change	Note 1	—	140	300	ns
	31	T_{DHC}	Data Hold From Chip Enable Change	Note 1	—	240	400	ns
POWER	32	I_S^+	Positive Supply Current		—	2.0	3.5	mA
	33	I_S^-	Negative Supply Current		—	2.0	3.5	mA

Notes:
1. Parallel Data Transfer ($\overline{BUS}$/Hand = 0). See Figure 1.
2. Operation at or above the absolute maximum stress ratings is not implied.
3. Static sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields.
4. For Pins 18, 19, 20 I_O = 750 μA

Pin Description and Function

PIN NO. 40-Pin DIP)	PIN NO. (60-Pin FP)	SYMBOL	DESCRIPTION
1	9	SGN	Sign Bit: 1 = Positive Input. The input signal polarity is determined at the end of the signal integrate phase.
2	10	DB_{15}	Data Bit 15 (MSB): Three State Output Data Bit
3	11	DB_{14}	14
4	12	DB_{13}	13
5	13	DB_{12}	12
6	18	DB_{11}	11
7	19	DB_{10}	10
8	20	DB_9	9
9	21	DB_8	8
10	22	DB_7	7
11	24	DB_6	6
12	25	DB_5	5
13	26	DB_4	4
14	27	DB_3	3
15	28	DB_2	2
16	33	DB_1	1 (LSB)
			NOTE: DB_{15} -DB, are at a logic "1" state for an overrange conversion.
17	34	Test	Test: 0 V; Data Outputs forced to Logic 1 and clock is disabled Test = V^+; Counter latches enabled.
18	35	$\overline{LBEN}/\overline{LBFLG}$ (Input/Output)	A low data byte enable input or flag output depending on $\overline{BUS}$/HAND (Pin 21) status 1. $\overline{BUS}$/HAND = 0: With Pin 21 low and $\overline{CE}/\overline{LDSTRB}$ = 0 (Pin 20) data bits 8 through 1 are output (pins 9 - 16) when the input pin $\overline{LBEN}$ = 0. 2. $\overline{BUS}$/HAND = 1: Valid data on pins 9 - 16 is indicated by the flag output $\overline{LBFLG}$ = 0.
18	36	$\overline{HBEN}/\overline{HBFLG}$ (Input/Output)	A high data byte enable input or flag output depending on BUS/HAND (pin 21) status. 1. $\overline{BUS}$/HAND = 0: With pin 21 low and $\overline{CE}/\overline{LDSTRB}$ = 0 (pin 20) the high data byte (Sign Bit plus Data Bits 15 - 9) are output when the input $\overline{HBEN}$ = 0 2. $\overline{BUS}$/HAND = 1: Valid Data on pins 1 - 8 is indicated by the flag output $\overline{HBLFG}$ = 0.
20	37	$\overline{CE}/\overline{LDSTRB}$ (Input/Output)	1. $\overline{BUS}$/HAND = 0: $\overline{CE}$ is master chip enable, With $\overline{CE}$ = 1 sign bit plus DB_{15} - DB_1 are disabled (Hi-Impedance State). $\overline{CE}$ = 0 enables outputs and data is transferred under control of $\overline{LBEN}$ and $\overline{HBEN}$ input signals.

$\overline{CE}$	$\overline{LBEN}$	$\overline{HBEN}$	FUNCTION
0	0	1	Low Data Byte Output
0	1	0	High Data Byte Output
0	0	0	Low + High Data Byte Output
0	1	1	High Impedance State

2. $\overline{BUS}$/HAND = 1: $\overline{LDSTRB}$ is a load strobe output sign. In the handshake mode, $\overline{LDSTRB}$ = 0 output signal instructs the receiving device to accept data.

Note:
Pin connections in description section refer to 40-pin package.

Pin Description and Function (Cont.)

PIN NO. 40-Pin DIP)	PIN NO. (60-Pin FP)	SYMBOL	DESCRIPTION
21	39	$\overline{BUS}$/HAND	1. $\overline{BUS}$ = 0: Parallel output data mode where the $\overline{CE}$, $\overline{HBEN}$, and $\overline{LBEN}$ signals are inputs that directly control the 16 data bits. 2. HAND = 1: $\overline{LDSTRB}$, $\overline{LBFLG}$, $\overline{HBFLG}$ are outputs used in the handshake data transfer mode. 3. Hand = ⎍ (Pulsed High): Causes entry into handsake mode for UART interfacing.
22	40	OSC_2	Oscillator input
23	41	OSC_1	Oscillator output
24	42	OSC CON	Selects internal oscillator structure 1. OSC CON = 1: RC oscillator. Internal clock frequency is same frequency and duty cycle as BUF OSC. 2. OSC CON = 0: Crystal oscillator, Internal clock frequency is frequency at BUF OSC ÷ 15.
25	43	BUFOSC	Buffered oscillator output
26	48	CONVERT/ $\overline{STOP}$	CONVERT = 1: Conversions performed continuously. $\overline{STOP}$ = 0: Conversion process stops 7 counts before entering signal integrate phase. The conversion in progress when $\overline{STOP}$ = 0 is completed.
27	49	DRQST	DATA OUTPUT request signal. An input used in the handshake mode that indicates an external device is ready to accept data.
28	50	V_S^-	Negative power supply
29	51	V_{REF}	Voltage reference input
30	52	COM	Analog common. The TSC800 is auto-zeroed to the analog common potential.
31	54	V_{INT}	Integrator output
32	55	C_{SZ}	SYSTEM-ZERO capacitor
33	56	V_{BUF}	Output of input signal buffer
34	57	C_R^-	Reference capacitor
35	59	C_R^+	Reference capacitor
36	1	V_{IN}^-	Negative differential analog input
37	3	V_{IN}^+	Positive differential analog input
38	5	V_S^+	Positive power supply
39	6	GND	Digital ground. Ground return point for Digital logic.
40	7	$\overline{DVD}$	DATA VALID SIGNAL: $\overline{DVD}$ = 1 during signal integrate and reference integrate phases until data is latched. $\overline{DVD}$ = 0 when in auto zero-phase. Data does not change when $\overline{DVD}$ = 0.

Note:
Pin connections in description section refer to 40-pin package.

8

General Theory of Operation

Dual Slope Conversion Principles

The TSC800 is a dual slope, integrating analog to digital converter. An understanding of the dual slope conversion technique will aid in following the detailed TSC800 operation theory.

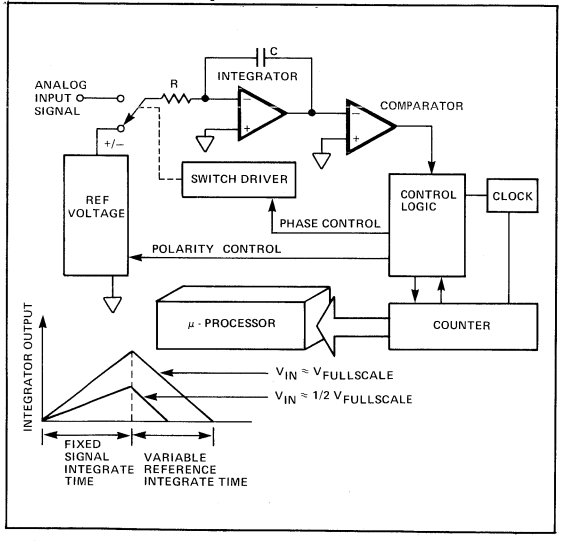
The conventional dual slope converter measurement cycle has two distinct phases:

- Input Signal Integration
- Reference Voltage Integration (Deintegration)

The input signal being converted is integrated for a fixed time period. Time is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output voltage returns to zero. The reference integration time is directly proportional to the input signal.

In a simple dual slope converter a complete conversion requires the integrator output to "ramp-up" and "ramp-down."

Basic Dual Slope Converter



The dual slope converter accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent benefit is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters in high noise environments.

A simple mathematical equation relates the input signal, reference voltage and integration time:

$$\frac{1}{RC}\int_0^{T_{SI}} V_{IN}(t)\,dt = \frac{V_R\,T_{RI}}{RC}$$

where:

V_R = Reference Voltage

T_{SI} = Signal Integration Time (Fixed)

T_{RI} = Reference Voltage Integration Time (Variable)

For a constant V_{IN}:

$$V_{IN} = V_R\left[\frac{T_{RI}}{T_{SI}}\right]$$

TSC800 Analog Input Description

System Zero Phase (Figure 3A)

During this phase errors due to buffer, integrator and comparator offset voltages are compensated for by charging C_{SZ} (system-zero capacitor) with a compensating error voltage. With a zero input voltage the integrator output will remain at zero.

The external input signal is disconnected from the internal circuitry by opening the two SW_I switches. The internal input points connect to analog common. The reference capacitor charges to the reference voltage potential through SW_R. A feedback loop, closed around the integrator and comparator, charges the C_{SZ} capacitor with a voltage to compensate for buffer amplifier, integrator and comparator offset voltages.

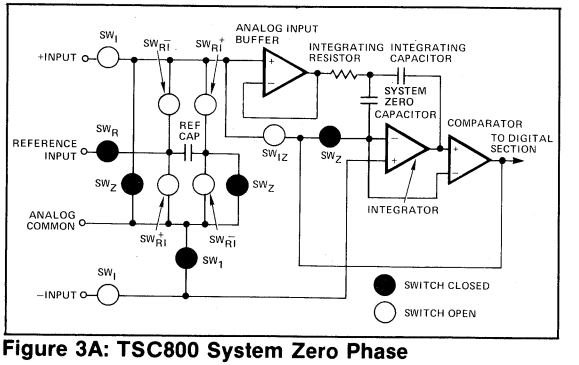


Figure 3A: TSC800 System Zero Phase

Analog Input Signal Integration Phase

(Figure 3B)

The TSC800 integrates the differential voltage between the + input and - input. The differential voltage must be within the device common-mode range; 1 V from either supply rail typically. The input signal is integrated for 16, 384 clock cycles.

The input signal polarity is determined at the end of the phase.

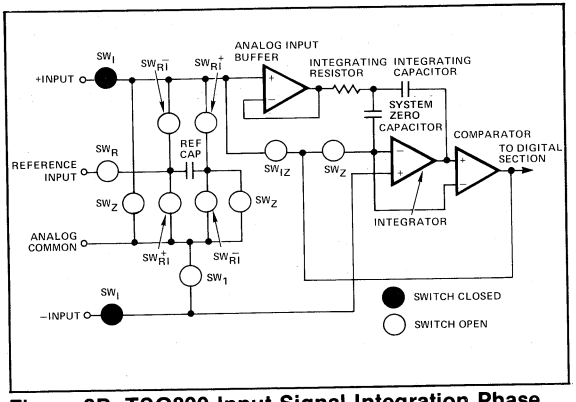


Figure 3B: TSC800 Input Signal Integration Phase

Reference Voltage Integration (Figure 3C)

The previously charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero. The time for the output to return to zero is proportional to the input signal magnitude. The phase lasts for a maximum of 32, 768 clock periods.

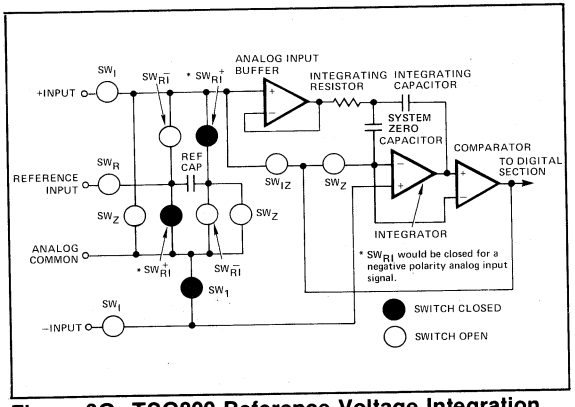


Figure 3C: TSC800 Reference Voltage Integration Cycle

Integrator Output Zero (Figure 3D)

This phase guarantees the integrator output is at zero volts when the system zero phase is entered and that the true system offset voltages are compensated for. This phase normally lasts 4096 clock cycles.

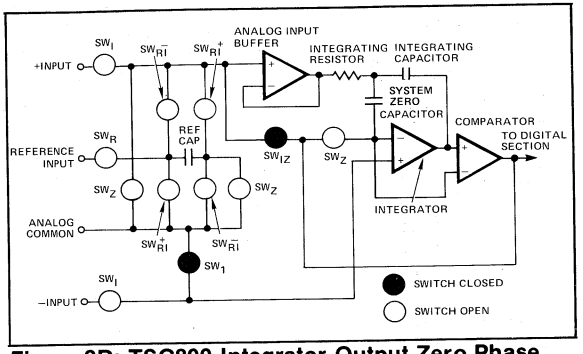


Figure 3D: TSC800 Integrator Output Zero Phase

Differential Inputs (V_{IN}^{+} (Pin 37) and V_{IN}^{-} (Pin 36))

The TSC800 operates with differential voltages within the input amplifier common-mode range. The input amplifier common-mode range extends from 1.0 V below the positive supply to 1.0 V above the negative supply. Within this common-mode voltage range an 86 dB common-mode rejection ratio is typical.

The integrator output also follows the common-mode voltage. The integrator output must not be allowed to saturate. A worst case condition exists, for example, when a large positive common-mode voltage with a near full scale negative differential input voltage is applied. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced. The integrator output can swing within 0.4 volts of either supply without loss of linearity.

Analog Common (Pin 30)

Analog common is used as the V_{IN}^{-} return during system-zero and reference-integrate. If V_{IN}^{-} is different from analog common, a common-mode voltage exists in the system. This signal is rejected by the excellent CMRR of the converter. In most applications V_{IN}^{-} will be set at a fixed known voltage (power supply common, for instance). In this application, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The reference voltage is referenced to analog common.

8

Digital Section Description

Digital Control Signals

$\overline{BUS}$/Hand (Pin 21)

The BUS/Hand input signal selects the parallel BUS data transfer mode or handshake transfer mode. An internal pull-down resistor guarantees parallel mode operation when the input pin is open. The handshake mode allows serial data transmission with a UART. In the parallel mode the TSC800 outputs data under control of the $\overline{HBEN}$, $\overline{LBEN}$ and $\overline{CE}$ signals. In the handshake mode TSC800 output signals communicate with peripheral devices to control the data transmission.

For $\overline{BUS}$ = 0 the $\overline{HBEN}$ (Pin 19), $\overline{LBEN}$ (Pin 18), and $\overline{CE}$ (Pin 20) input signals control the TSC800 data transmission. Figure 1 shows typical timing relationships and operation. The $\overline{HBEN}$, $\overline{LBEN}$ and $\overline{CE}$ signals are asynchronous to the internal conversion clock. Output data is immediately accessed. To avoid accessing data as updates are occuring the DATA VALID ($\overline{DVD}$, Pin 40) signal can be used as an enable signal. Data will not change if $\overline{DVD}$ = 0.

In the handshake mode two data transfer methods are possible. If HAND is pulsed high (HAND = ⎍) for a minimum of 70 nsec the TSC800 enters the handshake mode. If HAND = 1 continuously the parallel mode is not re-entered, and a handshake data transfer will occur at the end of each conversion cycle.

The $\overline{BUS}$/Hand input signal configures dual purpose pins 18, 19 and 20 as inputs or outputs. In conjunction with the DATA REQUEST (DRQST, Pin 27) input signal the handshake data transfer is controlled by the output signals: $\overline{LBFLG}$, $\overline{HBFLG}$, and $\overline{LDSTRB}$.

Data Request Input (DRQST, Pin 27)

This input is used only in the handshake data transfer mode. a DRQST = 1 input signal indicates an external receiving device is ready to accept data from the TSC800. It serves as a send data command. When $\overline{BUS}$/HAND = 0, DRQST should be tied to V_S^+.

Convert/$\overline{Stop}$ Input (CONV/$\overline{STOP}$, Pin 26)

The CONV/$\overline{STOP}$ control input is pulled high through an internal pull-up resistor. If CONV/$\overline{STOP}$ = 1 or left open the TSC800 continuously performs conversions. Each measurement cycle will be 65,536 counts long. The measurement cycle time for one conversion is:

$$T\ Conversion\ (msec) = 65.536\ 1/f_C(kHz)$$

Where: f_C = Internal Clock Frequency in kHz.

If CONV/$\overline{STOP}$ = 0 during the reference integrate phase and after a zero-crossing has been detected the integrator zero phase is immediately entered and completed. This eliminates the time spent in the reference integrate phase after the output data latches are updated.

If CONV/$\overline{STOP}$ remains low, the TSC800 will wait in the system zero phase. The signal integrate phase will begin 7 clock counts after a CONV = 1 signal is detected. The CONV/$\overline{STOP}$ signal is detected synchronously with the internal clock. The system zero phase is 7 counts long in this operating mode. See Figures 6 and 7 for CONV/$\overline{STOP}$ conversion timing diagrams.

If CONV/$\overline{STOP}$ goes low and remains low during the system zero phase, the TSC800 will stop at the end of the phase and wait for CONV = 1. The signal integrate phase will start seven clock counts after CONV = 1 is detected.

OPERATING MODE	PIN DESCRIPTION		
$\overline{BUS}$ Transfer Mode	$\overline{LBEN}$/$\overline{LBFLG}$ (Pin 18)	$\overline{HBEN}$/$\overline{HBFLG}$ (Pin 19)	$\overline{CE}$/$\overline{LDSTRB}$ (Pin 20)
$\overline{BUS}$/HAND = 0	$\overline{LBEN}$: Low Data Byte Enable Input. A logic 0 activates the low order data (DB_8 - DB_1) if $\overline{CE}$ = 0.	$\overline{HBEN}$: High Data Byte Enable Input. A logic 0 activates the high order data (SGN, DB_{15} - DB_9) if $\overline{CE}$ = 0.	$\overline{CE}$: Master Output Enable Input. When $\overline{CE}$ = 1 outputs (SGN, DB_{15} - DB_1) are disabled and in a high impedance state.
Handshake Transfer Mode $\overline{BUS}$/HAND = 1 or ⎍	$\overline{LBFLG}$: Low Data Byte Flag Output. Indicates output data is DB_8 - DB_1.	$\overline{HBFLG}$: High Data Byte Flag Output. Indicates output data is DB_{15} - DB_9.	$\overline{LDSTRB}$: Load Strobe Output Signal. A logic 0 or falling edge indicates valid data is present at the output.

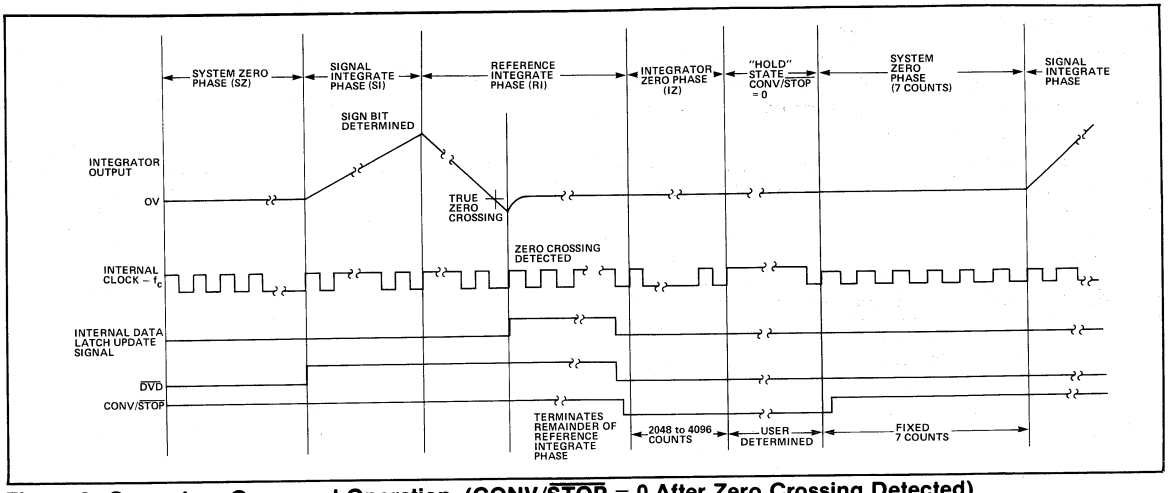


Figure 6: Convert on Command Operation. (CONV/STOP = 0 After Zero Crossing Detected)

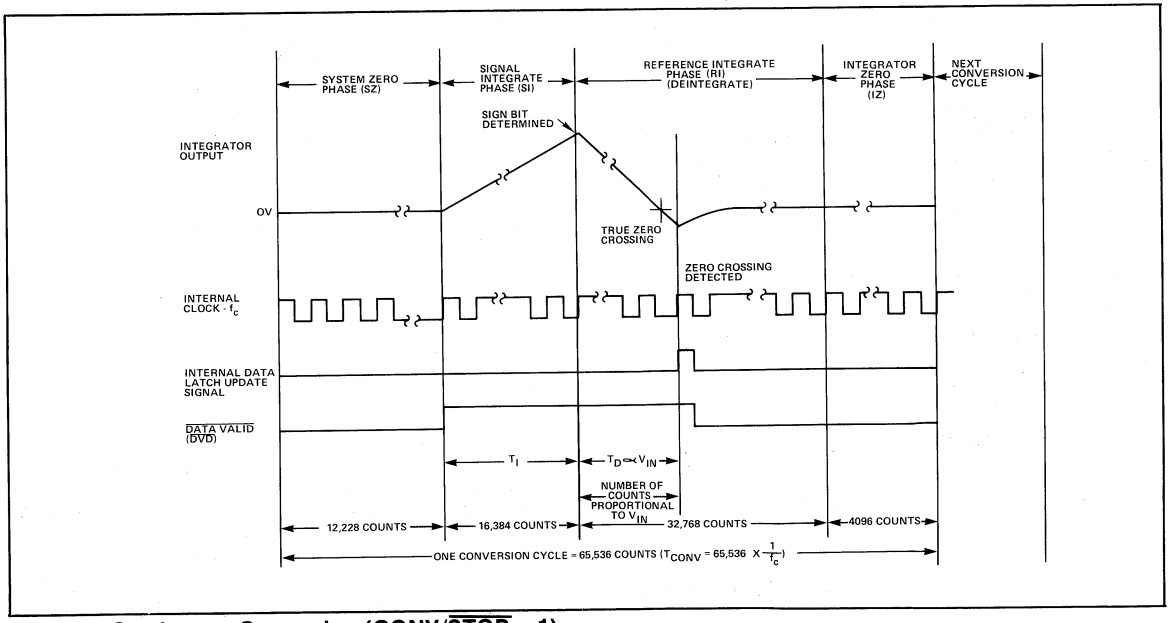


Figure 7: Continuous Conversion (CONV/STOP = 1)

Test Input (Pin 17)

When Test = 1 the counter data latches are enabled. If Test = 0 the counter outputs are forced to a 1 state and the internal clock is disabled. When Test is returned to a logic 1 and one clock pulse is applied all the counter outputs are clocked low.

Data Valid (DVD, Pin 40)

DVD = 1 at the start of signal integrate and DVD = 0 one half clock period after new data is stored in the data latches. Since DVD is always low when data is not changing the signal may be used as a "Data Valid Flag". See Figures 6 and 7 for timing relationships.

Data Output Description

Parallel Mode Data Interface

With $\overline{BUS}$/Hand = 0 the sign and data bits are controlled by the $\overline{CE}$ (Pin 20), $\overline{LBEN}$ (Pin 18) and $\overline{HBEN}$ (Pin 19) inputs. All three inputs have internal pullup resistors. Inactive data bits are in a high impedance state.

The $\overline{HBEN}$ signal controls the most significant data byte (SGN, DB_{15} - DB_9). $\overline{LBEN}$ controls the least significant data byte (DB_8 - DB_1).

$\overline{CE}$	$\overline{HBEN}$	$\overline{LBEN}$	High Data Byte (SGN, DB_{15} - DB_9)	Low Data Byte (DB_8 - DB_1)
1	X	X	Inactive (High Z State)	Inactive (High Z State)
0	0	0	Active	Active
0	0	1	Active	Inactive (High Z State)
0	1	0	Inactive (High Z State)	Active
0	1	1	Inactive (High Z State)	Inactive (High Z State)

"X" = 1 or 0

The $\overline{HBEN}$, $\overline{LBEN}$ and $\overline{CE}$ input signals are asynchronous with the internal conversion clock. Output data is immediately available. To avoid accessing data as data updates occur the DATA VALID (Pin 40) signal can control the data access. DATA will not change if $\overline{DVD}$ = 0.

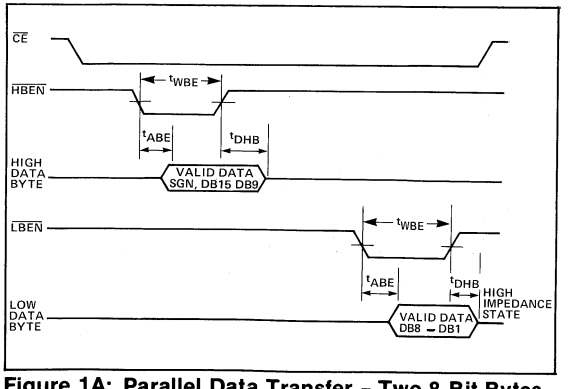


Figure 1A: Parallel Data Transfer - Two 8-Bit Bytes

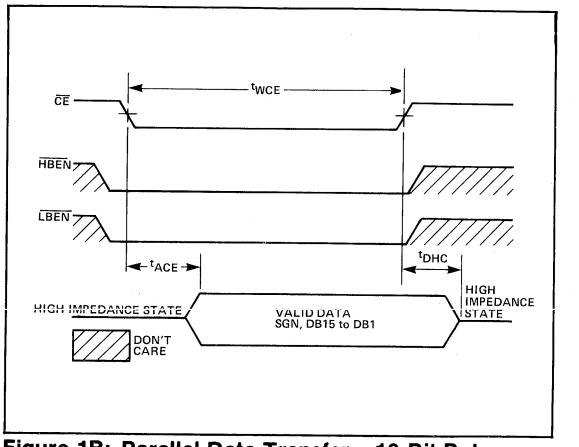


Figure 1B: Parallel Data Transfer - 16-Bit Bytes

Handshake Mode Data Transfer

The TSC800 actively controls the data transfer to peripherals through the handshake data transfer mode. In the handshake mode pins 18, 19 and 20 ($\overline{LBFLG}$, $\overline{HBFLG}$, and $\overline{LDSTRB}$) are TTL compatible outputs. The $\overline{LDSTRB}$ signal indicates valid data is available for the peripheral. The $\overline{LBFLG}$ and $\overline{HBFLG}$ signals indicate which data byte is being transferred. The data request signal (DRQST, Pin 27) informs the TSC800 a peripheral is ready to accept data. A complete cycle transfers two 8-bit bytes.

The $\overline{BUS}$/Hand signal is ignored after the handshake mode is entered. Conversions continue but data latch updating is inhibited until the TSC800 transfers two data bytes and clears the internal mode latch.

The handshake mode is entered in two ways:

- Set $\overline{BUS}$/Hand = 1
- Pulse $\overline{BUS}$/Hand High (⎍)

$\overline{BUS}$/Hand = 1

With Hand = 1 the TSC800 will enter the handshake mode after data is stored in the output data latches. Once the handshake mode internal latch signal is set the $\overline{BUS}$/Hand signal is ignored. The Data Request Input Signal (DRQST) signal controls data transfer to the external requesting peripheral. Figure 2 shows the timing diagram for the data transfer with $\overline{BUS}$/Hand = 1 (throughout the transfer). Note that DRQST = 1 throughout the transfer. The data transfer rate is set by the TSC800 internal clock. A complete data transfer occurs in 4 clock periods after a DRQST = 1 is detected on a high to low internal clock edge transition.

For peripherals that cannot accept data at the TSC800 clock rate the DRQST input signal can be used to delay the transmit sequence. This mode is useful in interfacing to UARTS. Figure 3 shows a typical 2502 UART interface.

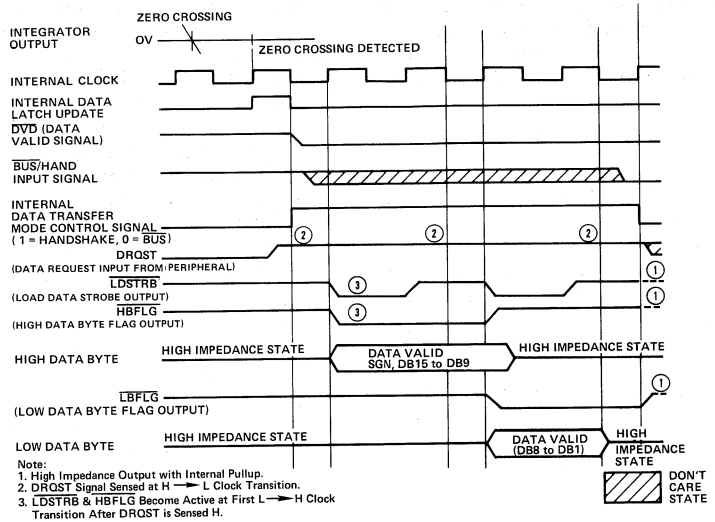


Figure 2: Data Transfer with $\overline{BUS}$/Hand = 1

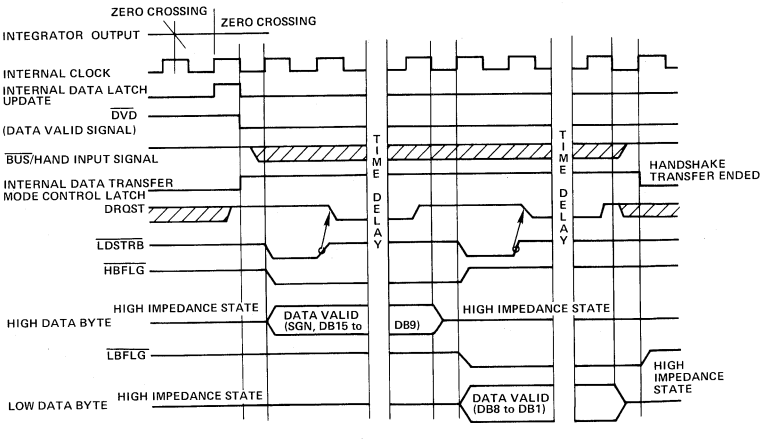


Figure 3A: Typical UART Interface Timing with DRQST Signal Controlling Data Transfer Timing

The UART data transfer sequence begins with a DRQST = 1 signal. This indicates the UART transmitter buffer register is empty (TBMT = 1). $\overline{\text{LDSTRB}}$ and $\overline{\text{HBFLG}}$ become active when DRQST is sensed synchronously. The high order data byte is stored in the UART transmitter buffer register when $\overline{\text{LDSTRB}}$ = 1. This occurs one clock period after DRQST is sensed. The DRQST signal (TBMT) goes low halting the cycle with the SGN and DBN$_{15}$ - DB$_9$ data bits active. After the UART transfers the received data to the transmitter register the DRQST input (TBMT) again goes high. On the first high to low internal clock transition the high byte data is disabled and one-half clock period later $\overline{\text{HBFLG}}$ = 1. Concurrently $\overline{\text{LDSTRB}}$ = 0 and DB$_8$ - DB$_1$, become active. One clock period later $\overline{\text{LDSTRB}}$ = 1 and the low data byte is clocked into the UART transmitter buffer register. DRQST goes low. When DRQST returns high it will be sensed on the first TSC800 internal clock high to low edge transition thus causing all outputs to be disabled. One half clock period later the internal handshake mode latch is cleared and $\overline{\text{LDSTRB}}$ = $\overline{\text{HBFLG}}$ = $\overline{\text{LBFLG}}$ = 1. The outputs remain active as long as Hand = 1.

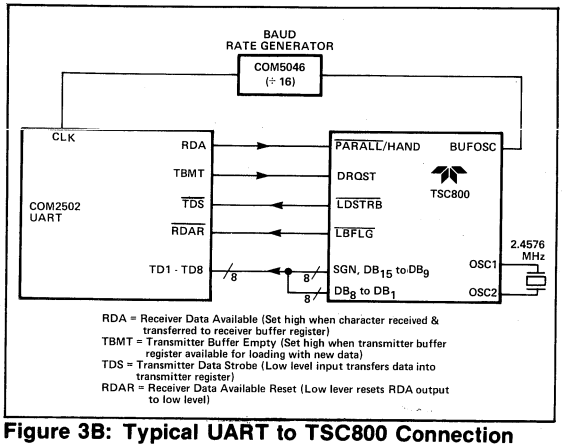


Figure 3B: Typical UART to TSC800 Connection

$\overline{\text{BUS}}$/Hand = ⎍ (Pulse)

The TSC800 outputs every conversion (except those completed during a handshake transfer) with Hand held high. Handshake output sequences on demand are possible by triggering the Hand control input with a low to high edge. Figure 4 shows a typical data transfer. The output cycle is controlled by the DRQST input signal. The complete two byte data transfer can take any length of time. Conversions are made and the $\overline{\text{DVD}}$ and CONV/$\overline{\text{STOP}}$ inputs function normally but new data will not be latched until the handshake mode is terminated.

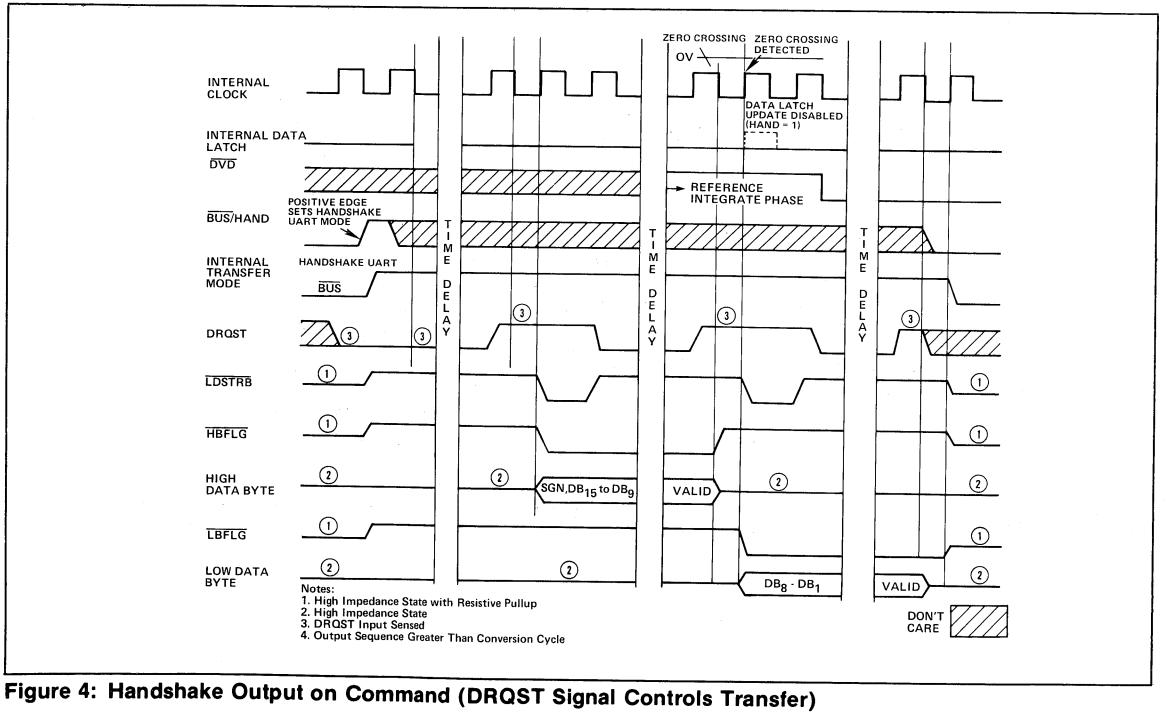


Figure 4: Handshake Output on Command (DRQST Signal Controls Transfer)

Oscillator Control and Operation

OSC CON (Pin 24) configures the internal oscillator as a crystal or RC oscillator. OSC CON = 1 establishes the RC oscillator. The internal clock matches the frequency and phase of the BUF OSC (Pin 25) signal. In the crystal oscillator mode (OSC CON = 0) a ÷ 15 is between the buffered oscillator output and the internal clock. The internal oscillator may be over-driven by driving OSC 1 (Pin 23). The OSC CON pin controls whether the internal clock is divided by 15.

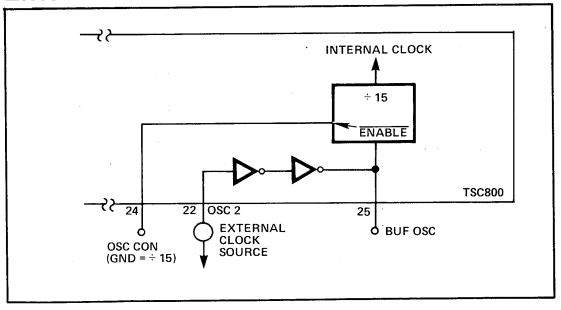
Oscillator Type	OSC CON (Pin 24)	Internal Clock Frequency	Signal Integration Time	Conversion Cycle Time
RC	V_S^+ or open	.45/RC	$16384\left(\frac{RC}{.45}\right)\frac{RC}{.45}$	[65,536]
Crystal	Ground	$f_{XTAL} \div 15$	$16384\left(\frac{15}{f_{XTAL}}\right)\frac{15}{f_{XTAL}}$	[65,536]

f_{XTAL} = Crystal Frequency

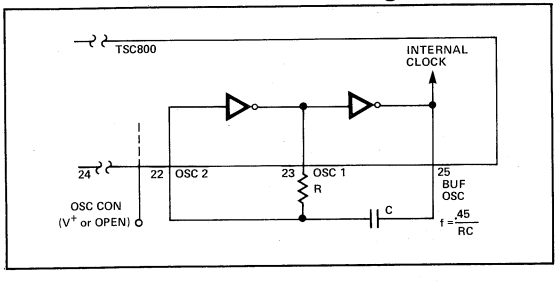
Typical Crystal Operation:

- f_X = 2.4576 mHz
- Internal Clock Frequency = 163.8 kHz
- Signal Integration Time = 100 msec
- Conversion Cycle Time = 400 msec (2.5 Conversions/Sec)

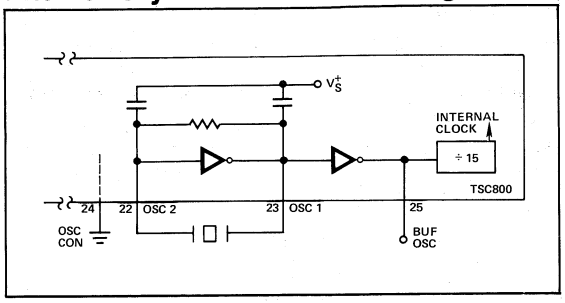
External Oscillator Control



Internal RC Oscillator Configuration



Internal Crystal Oscillator Configuration



Component Value Selection

Integrating Resistor (R_{INT})

The desired full-scale input voltage and output current capability of the input buffer and integrator amplifier set the integration resistor value. The internal class A output stage amplifiers will supply a 20 μA drive current with minimal linearity error. R_{INT} is easily calculated for a 20 μA full scale current:

$$R_{INT}\ (M\ \Omega) = \frac{\text{Full-Scale Input Voltage (V)}}{20}$$

Full-Scale Input Voltage (V_{FS})	R_{INT}
3.2768	160 k Ω
4.0000	200 k Ω

Integrating Capacitor (C_{INT})

The integrating capacitor should be selected to maximize integrator output swing. The integrator output will swing to within 0.4 V of V_S^+ or V_S^- without saturating. With ± 5 V power supplies and analog common connected to supply ground a 3.5 V to 4.3 V swing is adequate.

Using the suggested 20 μA full-scale buffer output current the integrating capacitor is easily calculated:

$$C_{INT}\ (\mu F) = \frac{16.384\left(\frac{1}{f_{CLK}\ (kHz)}\right)\ 20\ \mu A}{\text{Integrator Output Voltage Swing (V)}}$$

Where: f_{CLK} = Internal Clock Frequency

8

Component Value Selection (Cont.)

Integrating Capacitor (C_{INT})

For 2.5 CONV/SEC the internal clock is 163.8 kHz. The TSC800 operates at 2.5 CONV/SEC with an external crystal equal to 2.4576 MHz. A 0.47 μF capacitor is recommended.

The integrating capacitor should be selected for low dielectric absorption to prevent roll-over errors. Polypropylene capacitors are suggested. The outer foil of C_{INT} should be connected to C_{INT} (Pin 31).

System Zero Capacitor (C_{SZ})

A 1.0 μF polypropylene capacitor is suggested. The inner foil should be conected to C_{AZ} (Pin 32).

Reference Capacitor (C_{REF})

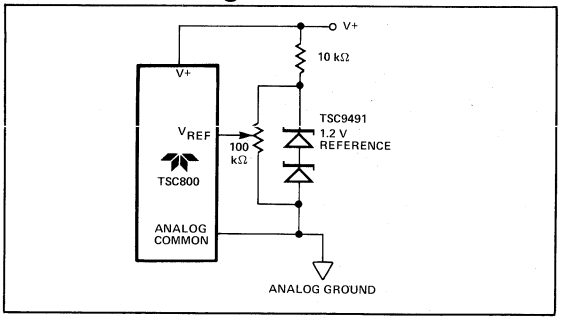
A 1.0 μF capacitor is suggested. Larger values may be used to limit roll-over errors. Low leakage capacitors such as polypropylene or Teflon® should be used.

Reference Voltage

The analog input required to generate the 32,768 full-scale count is $V_{INPUT} = 2\ V_{REF}$. The reference voltage source should be selected for temperature stability. The TSC800 provides 30 ppm resolution. With a 5 ppm/°C reference a 6° change will introduce a 1-bit absolute error. A stable reference must be used where ambient temperature is controlled and accurate absolute measurements are needed.

The reference voltage input must be a positive voltage with respect to analog common. Reference voltage circuits are shown below.

Reference Voltage Circuits

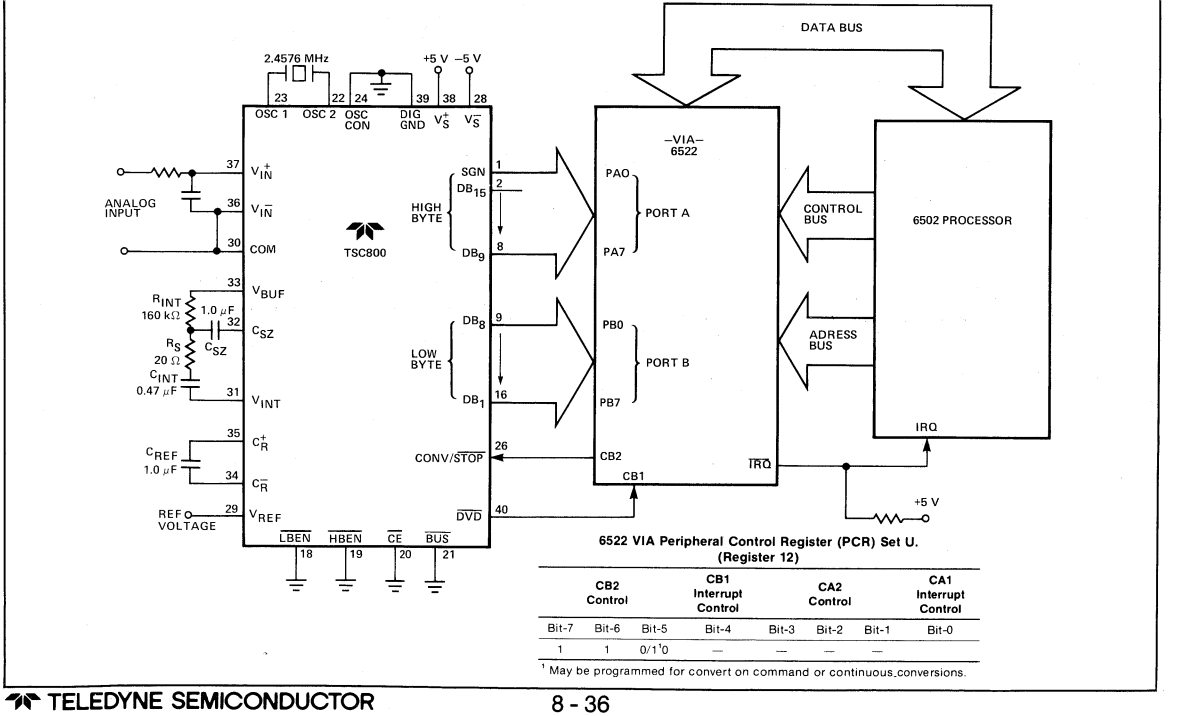


Delay Resistor (R_S)

The R_S, C_{INT} combination compensates for comparator delay time. With a 0.47 μF integrating capacitor a 20 Ω series resistor is suggested.

Applications Information

TSC800 Parallel Interface to 6522 Versatile Interface Adapter



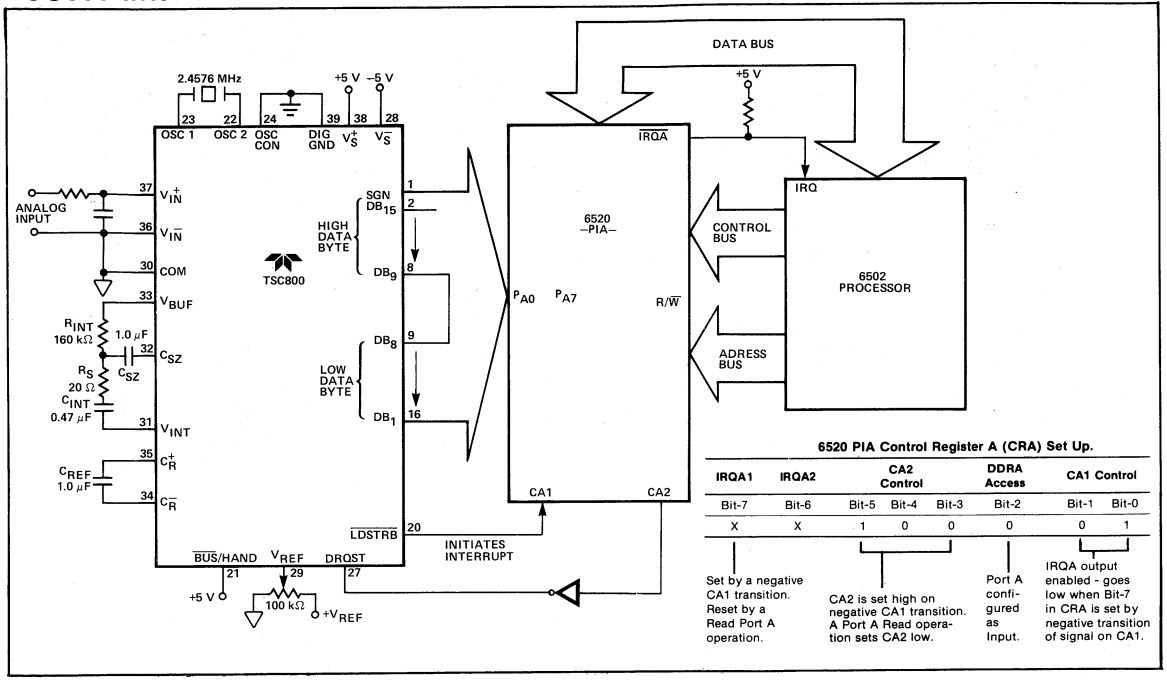
6522 VIA Peripheral Control Register (PCR) Set U. (Register 12)

CB2 Control			CB1 Interrupt Control	CA2 Control			CA1 Interrupt Control
Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
1	1	0/1[1]0	—	—	—	—	

[1] May be programmed for convert on command or continuous conversions.

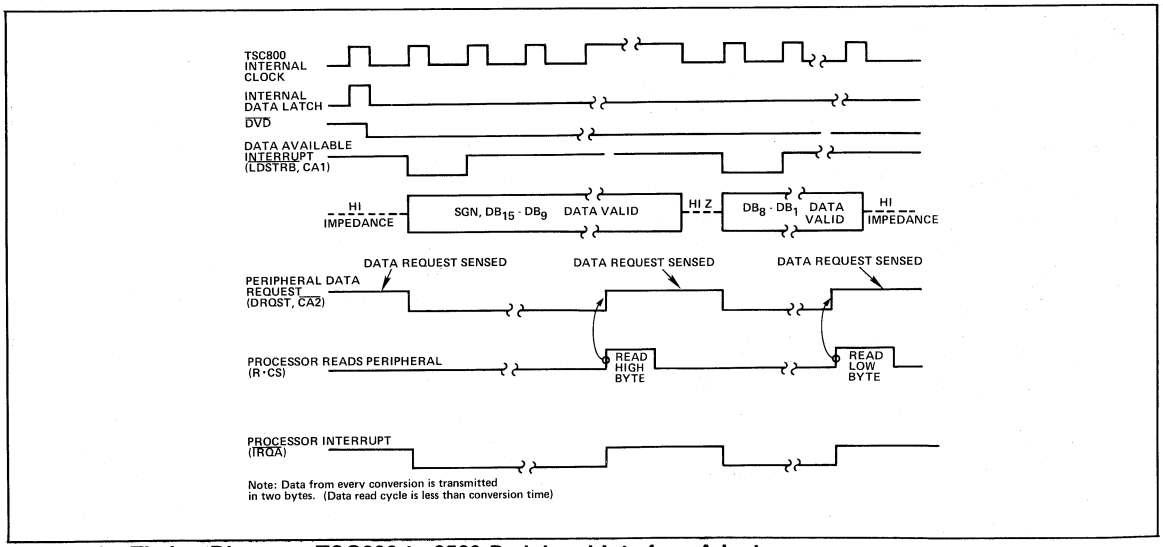
Applications Information (Cont.)

TSC800 Interface to 6520 VIA



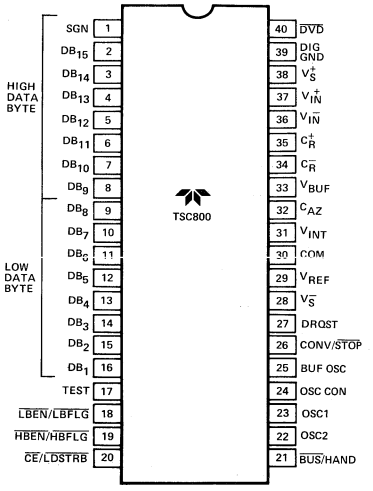
6520 PIA Control Register A (CRA) Set Up.

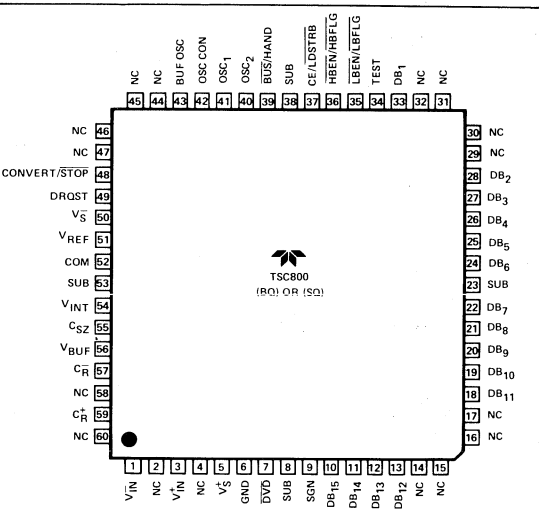
IRQA1	IRQA2	CA2 Control			DDRA Access	CA1 Control	
Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
X	X	1	0	0	0	0	1
Set by a negative CA1 transition. Reset by a Read Port A operation.		CA2 is set high on negative CA1 transition. A Port A Read operation sets CA2 low.			Port A configured as Input.	IRQA output enabled - goes low when Bit-7 in CRA is set by negative transition of signal on CA1.	



Handshake Timing Diagram: TSC800 to 6520 Peripheral Interface Adapter

Pin Configuration and Ordering Information



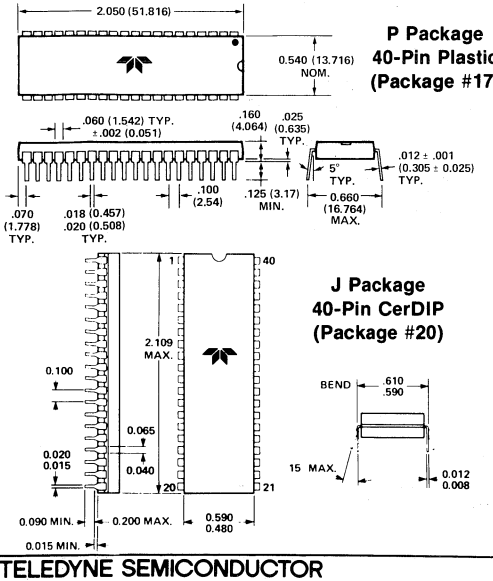


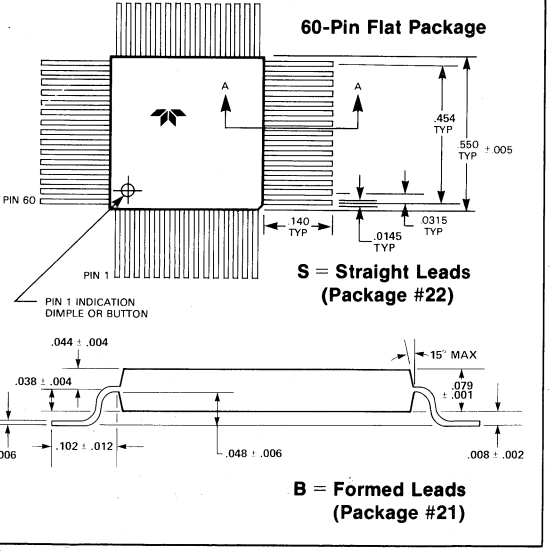
NOTE:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.

Ordering Information

Part No.	Package	Temp. Range
TSC800CPL	40-Pin Plastic	COM
TSC800IJL	40-Pin CerDIP	IND
TSC800MJL	40-Pin CerDIP	MIL
TSC800CBQ	60-Pin Plastic Flat Package: Formed Leads	COM
TSC800CSQ	60-Pin Plastic Flat Package: Unformed Leads	COM

Package Dimensions





TELEDYNE SEMICONDUCTOR

TSC8700 (8-Bit)
TSC8701(10-Bit)
TSC8702(12-Bit)
Binary Output ADCs

- **High Speed Conversion: 1-20 mSec**
- **Latched Parallel Output**

General Description

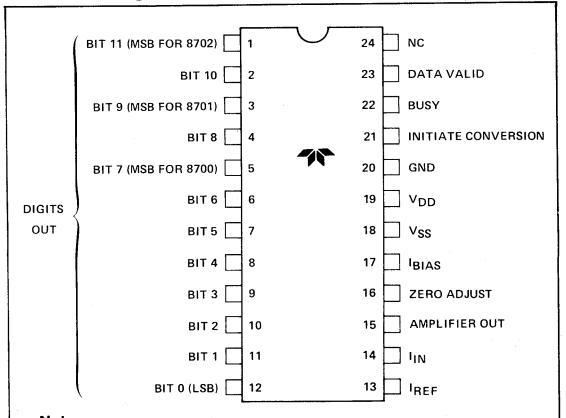
The TSC8700/8701/8702s are 8/10/ 12 bit monolithic CMOS analog-to-digital converters. Fully self-contained in a single 24-pin dual in-line package, each converter requires only passive support components, reference and power supplies.

Conversion is performed by an incremental charge balancing technique which has inherently high accuracy, linearity and noise immunity. An amplifier integrates the sum of the unknown analog current and pulses of a reference current, and the number of pulses (charge increments) needed to maintain the amplifier summing junction near zero is counted. At the end of conversion the total count is latched into the digital outputs as an 8/10/12-bit binary word.

Ordering Information

Part No.	Resolution	Conv. Time	Package	Temp. Range
TSC8700CJ	8-Bit	1.25 mSec	24-Pin Plastic Dip	0°C to +70°C
TSC8700CL	8-Bit	1.25 mSec	24-Pin CerDIP	-40°C to +85°C
TSC8701CL	10-Bit	5.0 mSec	24-Pin CerDIP	-40°C to +85°C
TSC8702CN	12-Bit	20 mSec	24-Pin Ceramic	-40°C to +85°C

Pin Configuration



Note:
Do not make connections to pin 1, 2, 3 or 4 on 8700; pin 1 or 2 on 8701. These pins are internally connected.

Features

- High Accuracy — Up to 12-Bit Resolution With < ±1/2 LSB Error
- Tight DNL of < ±1/2 LSB
- Monotonic Performance — No Missing Codes
- Monolithic CMOS Construction Gives Low Power Dissipation — 20 mW Typical
- Contains All Required Active Elements — Needs only Passive Support Components, Reference Voltage and Dual Power Supply
- High Stability Over Full Temperature Range
  - — Gain Temperature Coefficient Typically <25 ppm/°C
  - — Zero Drift Typically <30 μV/°C
  - — Differential Non-Linearity Drift Typically <25 ppm/°C
- Latched Parallel Binary Outputs
- LPTTL, 74LS, CMOS Compatible Outputs and Control Inputs
- Strobed or Free Running Conversion
- Infinite Input Range — Any Positive Voltage Can Be Applied Via a Scaling Resistor

Absolute Maximum Ratings

Storage Temperature ..... -65°C to + 150°C
Operating Temperature
(L, N) Package ..... -40°C to + 85°C
J Package ..... 0° to + 70°C
V_{DD} -V_{SS} ..... 18 V
I_{IN} ..... ±10 mA
I_{REF} ..... ±10 mA
Digital Input Voltage ..... -0.3 to V_{DD} +0.3 V
Operating V_{DD} and V_{SS} Range ..... 3.5 V to 7 V
Package Dissipation ..... 500 mW
Lead Temperature ..... 300°C
(Soldering, 10 seconds)

Handling Precautions

The 8700 series are CMOS devices must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static tubes or other conductive material. Use proper anti-static handling procedures. Do not connect in circuits under "power on" conditions, as high transients may cause permanent damage.

Electrical Characteristics: Unless otherwise specified, V_{DD} = +5 V, V_{SS} = -5 V, V_{GND} = 0, V_{REF} = -6.4 V, R_{BIAS} = 100 kΩ, test circuit shown. T_A = 25° C unless Full Temperature Range is specified (-40° C to +85° C for N and L package, 0° to 70° C for J package).

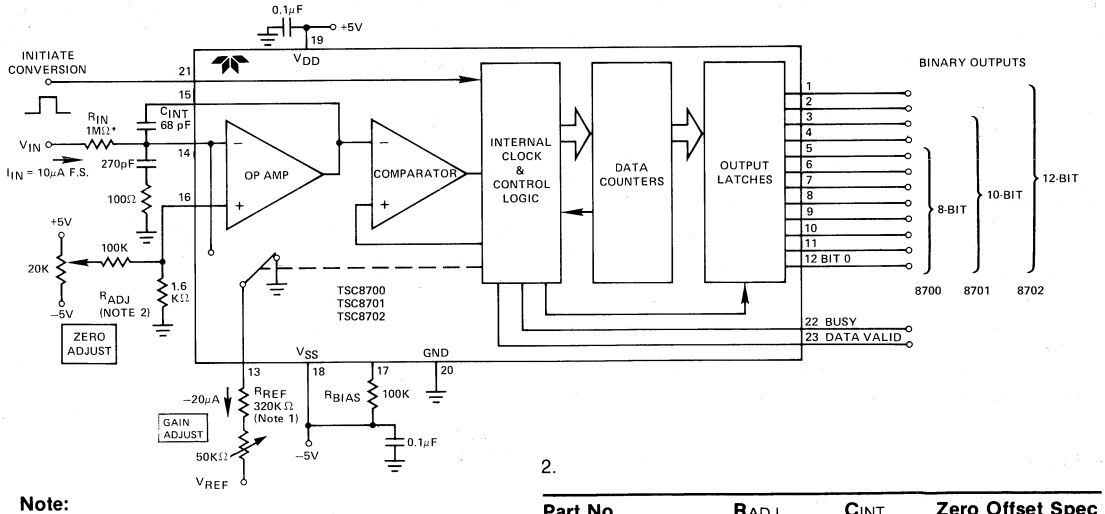
PARAMETER	CONDITIONS	DEFINITION	MIN	TYP	MAX	UNITS
Accuracy						
Resolution		Binary Word Length Of Digital Output				
Accuracy		TSC8700	8	—	—	Bits
		TSC8701	10	—	—	Bits
		TSC8702	12	—	—	Bits
Relative Accuracy		Output Deviation From Straight Line Between Normalized Zero and Full-Scale Input	—	—	±1/2	LSB
Differential Non-Linearity		Deviation From 1 LSB Between Transition Points	—	±1/4	±1/2	LSB
Differential Non-Linearity Temperature Drift	Full Temperature Range	Variation in Differential Non-Linearity Due To Temperature Change	—	±2.5	±5	ppm/° C
Gain Variance		Variation From Exact A (Compensate By Trimming R_{IN} or R_{REF})	—	±2	+5 -3	% of Nominal
Gain Temperature Drift	Full Temperature Range	Variation In A Due To Temperature Change	—	±25	±75	ppm/° C
Zero Offset (TSC8700)	I_{IN} = 0 C_{INT} = 68 pF R_{ADJ} = 1.6 kΩ See Test Circuit.	Correction at Zero Adjust to Give Zero Output When Input Is Zero Integration Cap. = 68 pF R_{ADJ} = 1.6 kΩ	—	—	±80	mV
Zero Offset (TSC8700)	I_{IN} = 0 C_{INT} = 33 pF R_{ADJ} = 1.0 kΩ See Test Circuit.	Correction at Zero Adjust to Give Zero Output When Input Is Zero Integration Cap. = 33 pF R_{ADJ} = 1.0 kΩ	—	±10	±50	mV
Zero Offset (TSC8701) (TSC8702)	I_{IN} = 0 C_{INT} = 68 pF R_{ADJ} = 1.0 kΩ See Test Circuit.	Correction at Zero Adjust to Give Zero Output When Input Is Zero Integration Cap. = 68 pF R_{ADJ} = 1.0 kΩ	—	±10	±50	mV
Zero Temperature Drift	Full Temperature Range	Variation in Zero Offest Due to Temperature Change	—	±30	±50	μV/° C
Analog Inputs						
I_{IN} Full-Scale		Full-Scale Analog Input Current To Achieve Specified Accuracy	—	10	—	μA
I_{REF} (Note 1)		Reference Current Input To Achieve Specified Accuracy	—	-20	—	μA
Digital Inputs						
$V_{IN}^{(1)}$	Full Temperature Range	Logical "1" Input Threshold For Initiate Conversion Input	3.5	—	—	V
$V_{IN}^{(0)}$	Full Temperature Range	Logical "0" Input Threshold For Initiate Conversion Input	—	—	1.5	V
Digital Outputs						
$V_{OUT}^{(1)}$	Full Temp. Range I_{OUT} = -10 μA I_{OUT} = -360 μA	Logical "1" Output Voltage For Digits Out, Busy, and Data Valid Outputs	4.5 2.4	— —	— —	V V
$V_{OUT}^{(0)}$	Full Temp. Range V_{DD} = 4.75 V I_{OUT} = 360 μA	Logical "0" Output Voltage For Digits Out, Busy, and Data Valid Outputs	—	—	0.4	V
Dynamic						
Conversion Time	Full Temp. Range	Time Required to Perform One Complete A/D Conversion				
		TSC8700	—	1.25	1.8	ms
		TSC8701	—	5	6	ms
		TSC8702	—	20	24	ms
Conversion Rate in Free-Run Mode	$V_{INT\ CONV}$ = + 5 V	TSC8700	555	800	—	Conv'ns
		TSC8701	167	200	—	per
		TSC8702	42	50	—	Second

Electrical Characteristics (Cont.)

PARAMETER	CONDITIONS	DEFINITION	MIN	TYP	MAX	UNITS
Minimum Pulse Width for Initiate Conversion	Full Temp. Range		500	—	—	ns
Supply Current						
I_{DD} Quiescent (L/N Package) (J Package)	Full Temp. Range $V_{INT\ CONV}$ = 0V	Current Required From Positive Supply During Operation	— —	1.4 1.4	2.5 5.0	mA mA
I_{SS} Quiescent (L/N Package) (J Package)	Full Temp. Range $V_{INIT\ CONV}$ = 0V	Current Required From Negative Supply During Operation	— —	-1.4 -1.4	-2.5 -5.0	mA mA
Supply Sensitivity	V_{DD} ± 1V, V_{SS} ±1.V	Change in Full-Scale Gain vs Supply Voltage Change	—	±0.5	±1.0	%/V
	$\|V_{DD}\| = \|V_{SS}\|$ = 5 V ± 1	Change in Full-Scale Gain vs Supply Voltage Change for Tracking Supplies	—	±0.05	±0.1	%/V

NOTE:
I_{IN} and I_{REF} pins connect to the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors. See Test Circuit.

Test Circuit



Note:
1. Any V_{REF} greater than -1 V can be used.

$$R_{REF} = \frac{V_{REF}}{-20\ \mu A}$$

For example with V_{REF} = -5 V, R_{REF} = 250 K.

2.

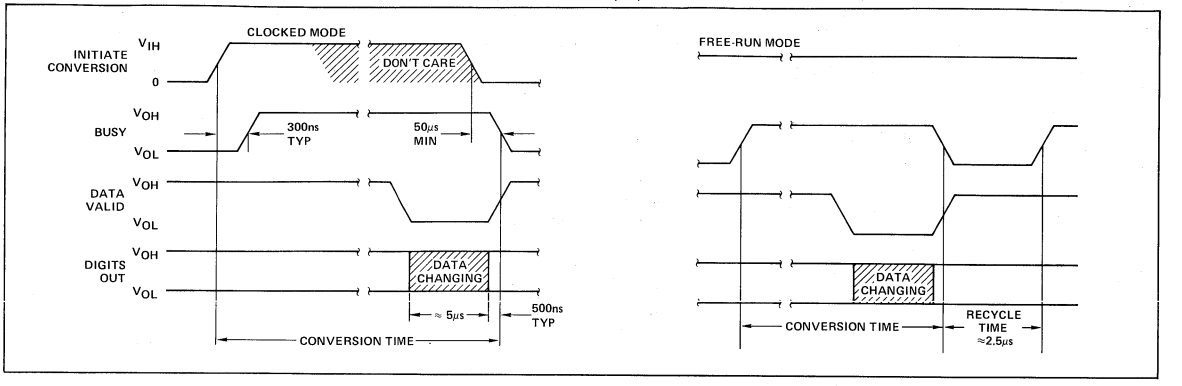
Part No.	R_{ADJ}	C_{INT}	Zero Offset Spec
TSC8700	1.6 kΩ	68 pF	±80 mV
TSC8700	1.0 kΩ	33 pF	±50 mV
TSC8701/8702	1.0 kΩ	68 pF	±50 mV

Circuit Description

During conversion the sum of a continuous current I_{IN} and pulses of a reference current I_{REF} is integrated for a fixed number of clock periods. I_{IN} is proportional to the analog input voltage; I_{REF} is switched in for exactly one clock period just frequently enough to maintain the output of the integrator near zero. Thus, the charge from the continuous I_{IN} current is balanced against the pulses of I_{REF} current. The total number of I_{REF} pulses needed during the conversion period to maintain the charge balance is counted, and the result (in Binary) is latched into the outputs at the end of conversion.

The converter contains two counters and a clock in addition to an operational amplifier, comparator, latching output buffers and housekeeping logic. One counter is a clock counter which (after a reset pulse) starts counting clock pulses; when the required count is reached, the clock counter generates a pulse to start the end-of-conversion routine.

Timing Diagrams (Rise, fall times = 200 ns typ., C_L = 50 pF)



The other counter is a data counter, which is reset synchronously with the clock counter and counts the number of times the I_{REF} current is switched into the summing input of the amplifier during the period defined by the clock counter.

When the Initiate Conversion input is strobed with a positive signal, the busy line latches high and a 10 μs (times given are approximate) start up cycle begins. The integrating capacitor is discharged and both counters are reset during this start up period. Conversion begins at the end of the reset pulse and ends with a pulse generated either by the clock counter or by an overflow condition in the data counter. This pulse disables further inputs into both counters and triggers a 10 μs shutdown cycle. During the shutdown cycle Data Valid goes low for 5 μs. This binary sequence is shown in the timing diagrams. Busy is true high, and when the circuit is busy, Initiate Conversion has no effect and may be high or low. Data Valid is also true high. The data from a conversion remain valid for as long as power is applied to the circuit or until Data Valid falls at the end of a subsequent conversion, at which time the output data are updated to reflect the latest conversion.

Pin Functions

Initiate Conversion Input

Accepts CMOS and most 5 V logic inputs. Applying a logic "1" to the Initiate Conversion pin initiates the A/D conversion cycle. Once conversion has been initiated, the cycle cannot be interrupted, and the Initiate Conversion pin is disabled until conversion is complete. Two modes of operation are permitted, clocked or free-running. For clocked operation the Initiate Conversion input is held at logic "0" for standby and taken to logic "1" when a conversion is desired. For free-running operation the Initiate Conversion pin is connected to V_{DD} or similar permanent logic "1" voltage.

Busy Output

A digital status output which is compatible with CMOS logic and low power TTL (can sink and source 500 μA). A logic "1" output on the Busy pin indicates a conversion cycle is in process. A logic "1" to logic "0" transition indicates that conversion is complete and the result has been latched at the Digits Out pins. A logic "0" to logic "1" transition indicates a new conversion cycle has been initiated. If the device is operating in the free-running mode, the Busy output will remain low for approximately 2.5 μs, marking the completion and initiation of consecutive conversion cycles.

Data Valid Output

A digital status which is compatible with CMOS logic and low power TTL (can sink and source 50 μA). A logic "1" output at the Data Valid pin indicates that the Digits Out pins are latched with the result of the last conversion cycle. The Data Valid output goes to logic "0" approximately 5 μs before the completion of a conversion cycle. During this 5 μs interval new data is being transferred to the Digits Out pins, and the Digits Out are not valid.

Digits Out
(Bit 0, Bit 1, etc.)

The binary digit outputs which are the result of the A/D conversion. These outputs are CMOS logic and low power TTL compatible.

Applications Information

Input/Output Relationships

The analog input voltage (V_{IN}) is related to the output by the transfer equation:

$$\text{Digital Counts} = \frac{V_{IN} \cdot A \cdot R_{REF}}{R_{IN} \cdot V_{REF}}$$

A = 528 for 8700
A = 2064 for 8701
A = 8208 for 8702

where Digital Counts is the value of the binary output word presented at Digits Out pins in response to V_{IN}.

The digital output code format is as follows:

Analog Input	Digital Output MSB ... LSB
$V_{IN} \leq$ Full-Scale	1 . . . 111 . . . 1
= Full-Scale -1 LSB	1 . . . 111 . . . 1
= 1 LSB	0 . . . 000 . . . 1
≤ 0	0 . . . 000 . . . 0

Two's complement coding can be generated by inverting the Most Significant Bit (MSB) signal.

External Component Selection

Obtaining a high accuracy conversion system depends on the voltage regulation of V_{REF} and the thermal stability of R_{IN} and R_{REF}. The exact dependence is given by the transfer function. System accuracy also depends, to a lesser degree, on the voltage regulation of V_{DD} and V_{SS}. The supply connections V_{DD} and V_{SS} should have bypass capacitors of value 0.1 μF or larger right at the device pins.

R_{IN}, R_{EF}

Values of these components are chosen to give a full-scale input current of approximately 10 μA and a reference current of approximately -20 μA.

$$R_{IN} \cong \frac{V_{IN}\ \text{Full-Scale}}{10\ \mu A} \qquad R_{REF} \cong \frac{V_{REF}}{-20\ \mu A}$$

Examples:

$$R_{IN} \cong \frac{10\ V}{10\ \mu A} = 1\ M\Omega \qquad R_{REF} \cong \frac{-6.4\ V}{-20\ \mu A} = 320\ k\Omega$$

Note that these values are approximations, and the exact relationships are defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed using the optional gain adjust circuit to obtain full-scale output at V_{IN} Full-Scale (see adjustment procedure). Metal film resistors with 1% tolerance or better are recommended for high accuracy applications because of their thermal stability and low noise generation.

R_{BIAS}

Specifications for the TSC87XX are based on R_{BIAS} = 100 kΩ $\pm$10% unless otherwise noted. However, there are instances when the designer may want to change this resistor in order to affect the conversion time and the supply current. By decreasing R_{BIAS} the A/D will convert much faster and the supply current will be higher. (For example: When R_{BIAS} is 20 k the conversion time is reduced by 1/3, and the supply current will increase from 2 mA to 7 mA.) Likewise, if the R_{BIAS} is increased the conversion time will be longer and the supply current will be much lower. (For example: When R_{BIAS} = 1 MΩ the conversion time will be six times longer, and tne supply current is now reduced to .5 mA). For details of this relationship refer to AN 9 typical performance curves.

R_{DAMP}

Exact value not critical but should have a nominal value of 100 Ω $\pm$10%. Locate close to pin 14.

C_{DAMP}

Exact value not critical but should have a nominal value of 270 pF $\pm$20%. Locate close to pin 14.

C_{INT}

Exact value not critical but should have a nominal value of 68 pF $\pm$10%. Low leakage types are recommended, although mica or ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 14, 15. For the TSC8700 C_{INT} = 33 pF is adequate with R_{ADJ} = 1.0 kΩ.

V_{REF}

A negative reference voltage must be supplied. This may be obtained from a constant current source circuit or from the negative supply.

V_{DD}, V_{SS}

Power supplies of $\pm$5 V are recommended, with 0.05% line and load regulation and 0.1 μF decoupling capacitors.

Adjustment Procedure

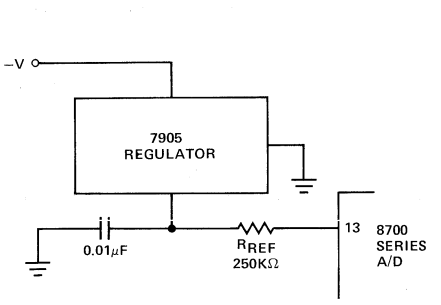
The test circuit diagram shows optional circuits for trimming the zero location and full-scale gain. Because the digital outputs remain constant outside of the normal operating range (i.e. below zero and above full-scale), it is recommended that transition points be used in setting the zero and full-scale values. Recommended procedure is as follows:

- Set the initiate conversion control high to provide free-run operation and verify that converter is operating.
- Set V_{IN} to +1/2 LSB and trim the zero adjust circuit to obtain a 000 . . . 000 . . . to 000 . . . 001 transition. This will correctly locate the zero end.
- For full-scale adjustment, set V_{IN} to the full-scale value less 1 1/2 LSB and trim the gain adjust circuit for a 111 . . . 110 to 111 . . . 111 transition.

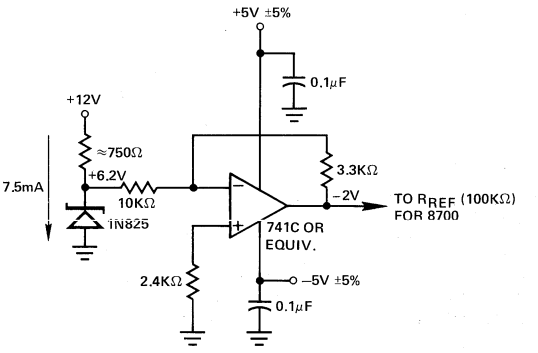
If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

Typical Circuits

Reference Voltage Supply

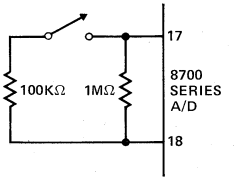


-5 V Reference

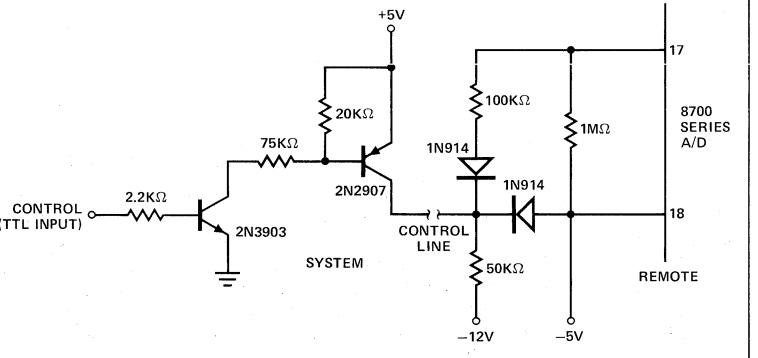


-2 V Reference for 8700 Using Voltages Derived From 8080A μP

Power Reduction (Reduces Power Consumption to Approximately 500 μA).

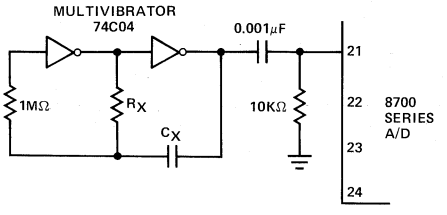


Switch Controlled - Relay
Could be Substituted for Switch



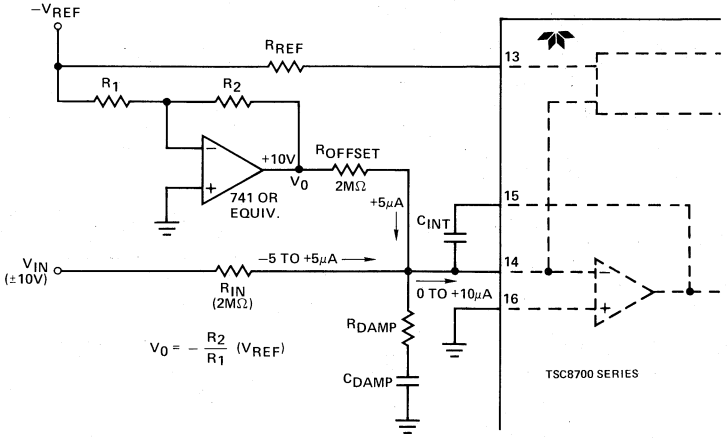
TTL System-Controlled — Trades Off Additional Power
Consumption at System for Reduced Usage at Remote A/D

Free-Running Conversion Rate Control



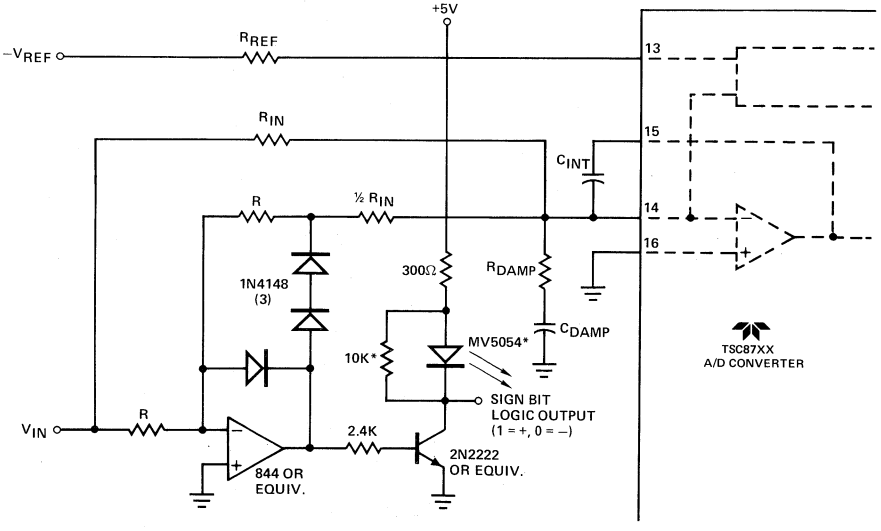
Multivibrator circuit at Pin 21 (Initiate Conversion) strobes converter at rates slower than the normal free-run mode. ($\tau = R_X C_X$)

Bipolar Operation



Two's complement coding may be generated by inverting the MSB output.

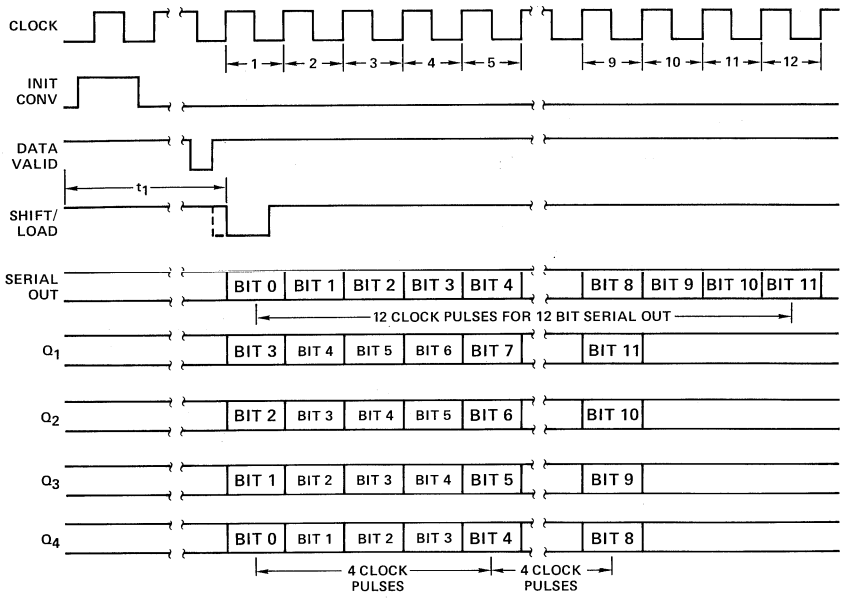
Offset Binary



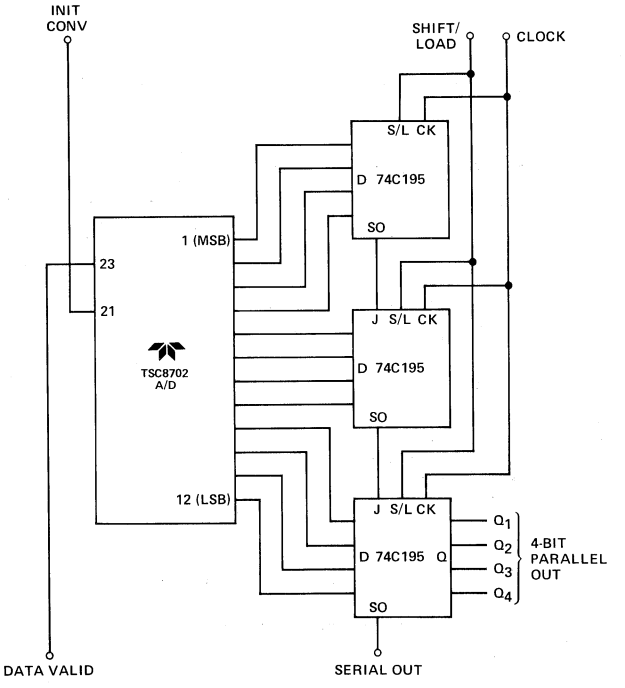
*Optional visual indication of negative input

Magnitude-and-Sign Binary

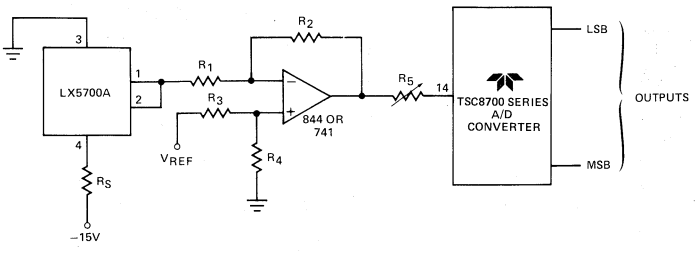
12-Bit Serial or 3 x 4-Bit Parallel Output Format



System reads parallel outputs at clock pulse 1, 5, 9.
Shift/load may be taken low when Data Valid goes high or at fixed time t_1, after INIT CONV ($t_1 \geq 24$ ms for TSC8702). Shift/load then must return high before clock pulse 2 and must remain high until all data is read out. Recommended clock frequency 2 kHz min for serial, 750 Hz min for parallel output.



Digital Temperature Monitor



R_1. Typically 10K min. This resistor should be chosen for the proper loading R_L of the LX5700A.

R_2. This resistor is adjusted to give a full scale reading of 10.00V for the A/D.

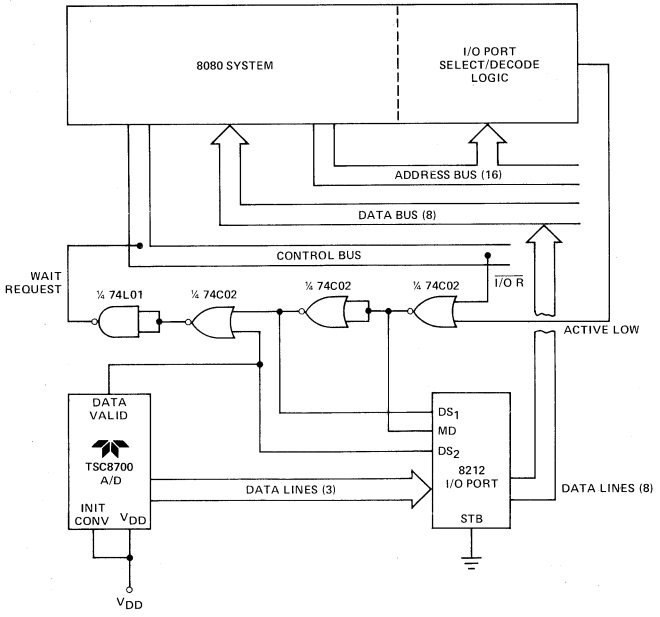
R3 = R4. Is set to give minimum offset. The value is approximately equal to $R_2 \parallel R_1$.

R_5. 1M typical. This resistor is adjusted to give full scale gain for the A/D.

R_S. 7.5KΩ. $R_S = (V^+ - 6.8) \times 10^{-3}\Omega$.

V_{REF}. The value of V_{REF} is chosen to set the temperature range desired.

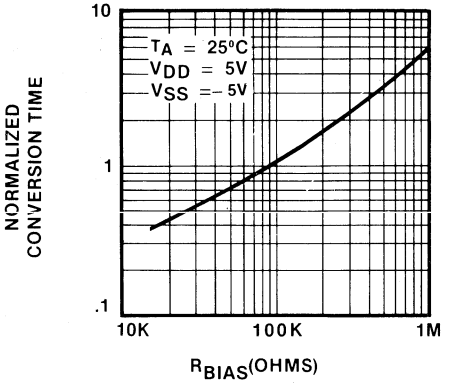
8-Bit Microprocessor Interface



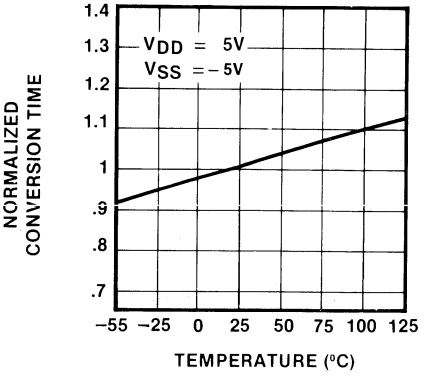
8

TYPICAL PERFORMANCE CURVES

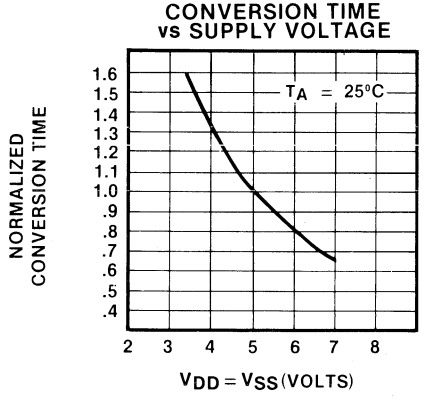
CONVERSION TIME vs R_{BIAS}



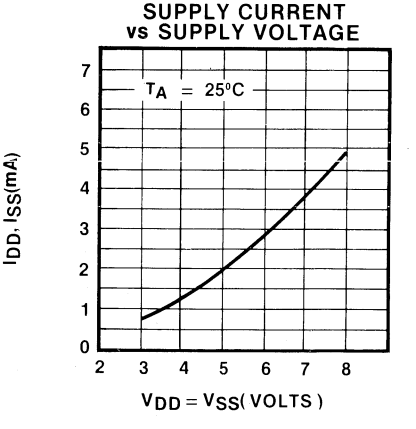
CONVERSION TIME vs TEMPERATURE



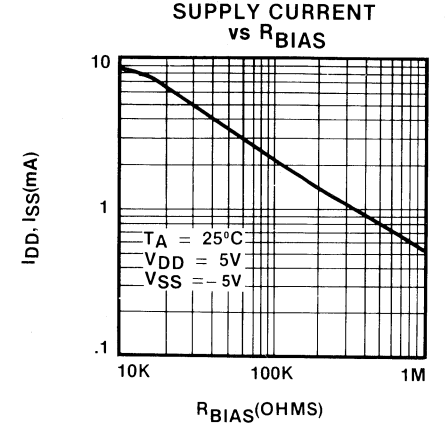
CONVERSION TIME vs SUPPLY VOLTAGE



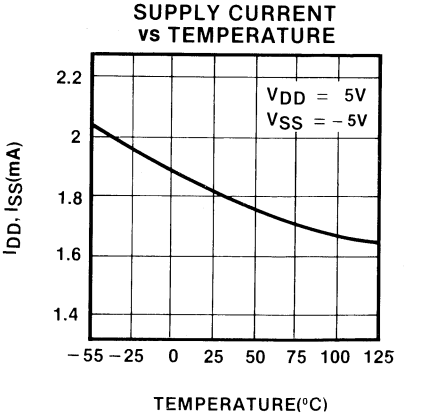
SUPPLY CURRENT vs SUPPLY VOLTAGE



SUPPLY CURRENT vs R_{BIAS}

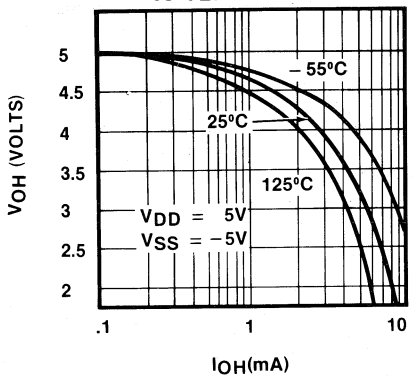


SUPPLY CURRENT vs TEMPERATURE

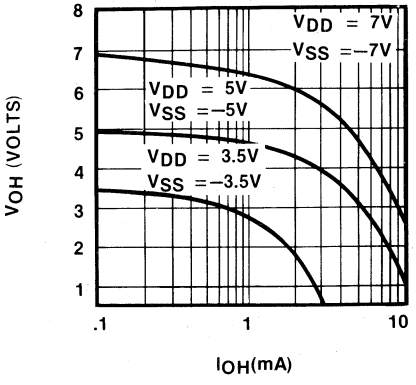


TYPICAL PERFORMANCE CURVES

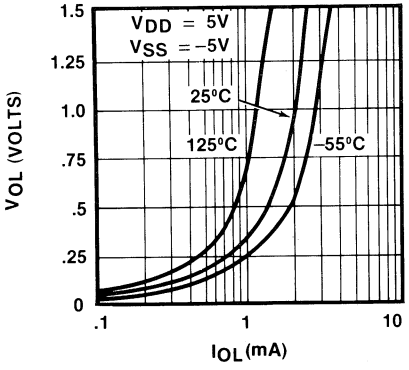
OUTPUT SOURCE CURRENT vs TEMPERATURE



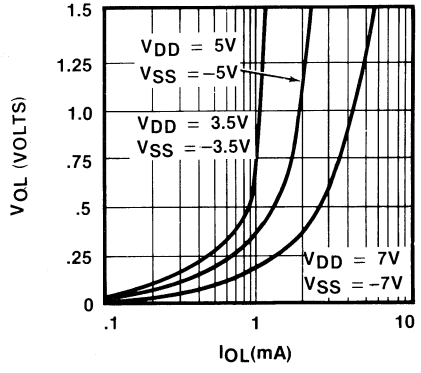
OUTPUT SOURCE CURRENT vs SUPPLY VOLTAGE



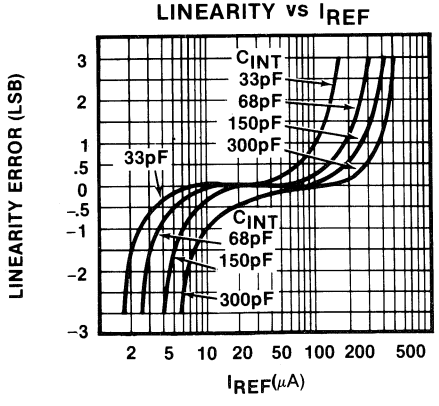
OUTPUT SINK CURRENT vs TEMPERATURE



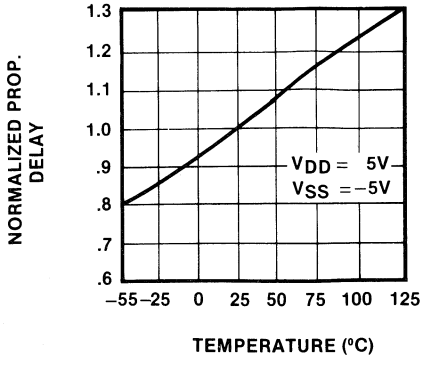
OUTPUT SINK CURRENT vs SUPPLY VOLTAGE



LINEARITY vs I_{REF}



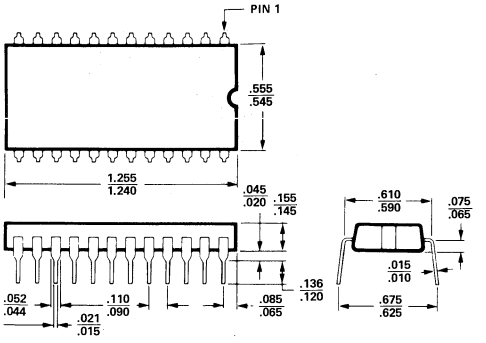
TRI-STATE PROPAGATION DELAY



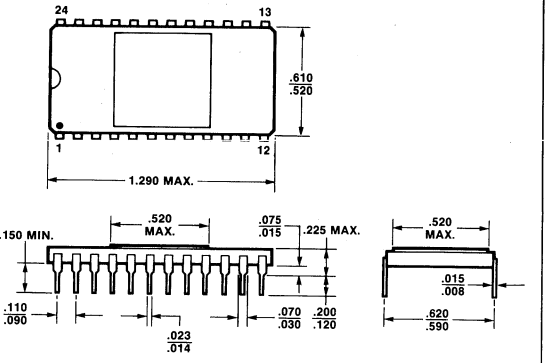
8

Package Information

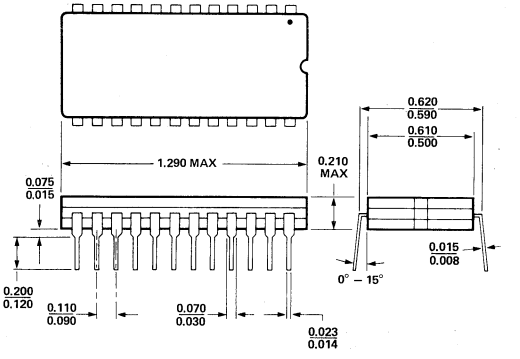
24-Pin Plastic Dip (J Package)
(Package #12)



24-Pin Ceramic Dip (N Package)
(Package #13)



24-Pin CerDIP (L Package)
(Package #14)



TELEDYNE SEMICONDUCTOR

TSC8703 (8-Bit)
TSC8704 (10-Bit)
TSC8705 (12-Bit)
Binary Output ADC

- **Three State, Latched Outputs**
- **High Speed Conversion: 1-20 mSec**

General Description

The TSC8703/8704/8705 are 8/10/ 12 bit monolithic CMOS analog-to-digital converters. Fully self-contained in a single 24-pin dual in-line package, each converter requires only passive support components, reference and power supplies.

Conversion is performed by an incremental charge balancing technique which has inherently high accuracy, linearity and noise immunity. An amplifier integrates the sum of the unknown analog current and pulses of a reference current, and the number of pulses (charge increments) needed to maintain the amplifier summing junction near zero is counted. At the end of conversion the total count is latched into the digital outputs as an 8/10/12 bit binary word. The Output Enable control switches the outputs to a high impedance or off state when held high. The off state allows bus organized output connections.

Ordering Information

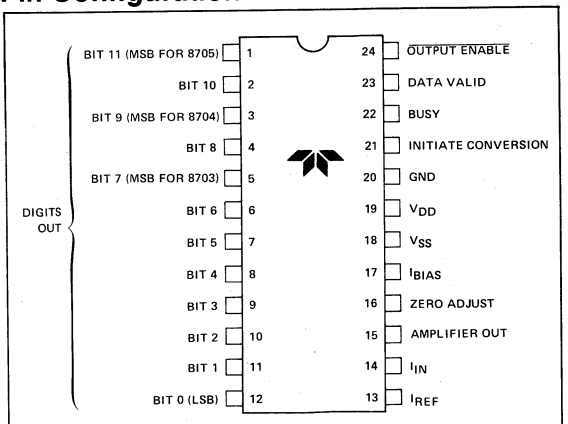
Part No.	Resolution	Conv. Time	Package	Temp. Range
TSC8703CJ	8-Bit	1.25 mSec	24-Pin Plastic Dip	0° C to +70° C
TSC8703CL	8-Bit	1.25 mSec	24-Pin CerDIP	-40° C to +85° C
TSC8703BL	8-Bit	1.25 mSec	24-Pin CerDIP	-55° C to +125° C
TSC8704CJ	10-Bit	5.0 mSec	24-Pin Plastic Dip	0° C to +70° C
TSC8704CL	10-Bit	5.0 mSec	24-Pin CerDIP	-40° C to +85° C
TSC8704BL	10-Bit	5.0 mSec	24-Pin CerDIP	-55° C to +125° C
TSC8705CJ	12-Bit	20 mSec	24-Pin Plastic Dip	0° C to +70° C
TSC8705CN	12-Bit	20 mSec	24-Pin Ceramic	-40° C to +85° C
TSC8705BN	12-Bit	20 mSec	24-Pin Ceramic	-55° C to +125° C
Devices with MIL-STD-883 Processing				
TSC8703BL/883	8-Bit	1.25 mSec	24-Pin CerDIP	-55° C to +125° C
TSC8704BL/883	10-Bit	5.0 mSec	24-Pin CerDIP	-55° C to +125° C
TSC8705BN/883	12-Bit	20 mSec	24-Pin Ceramic	-55° C to +125° C

Features

- High Accuracy — Up to 12 Bit Resolution With < ±1/2 LSB Error
- Monotonic Performance — No Missing Codes
- Monolithic CMOS Construction Gives Low Power Dissipation — 20 mW Typical
- Contains All Required Active Elements — Needs only Passive Support Components, Reference Voltage and Dual Power Supply
- High Stability Over Full Temperature Range
  - — Gain Temperature Coefficient Typically <25 ppm/° C
  - — Zero Drift Typically <30 μV/° C
  - — Differential Non-Linearity Drift Typically <25 ppm/° C
- Latched Parallel Binary Outputs
- LPTTL, 74LS, CMOS Compatible Outputs and Control Inputs
- Strobed or Free Running Conversion
- Infinite Input Range — Any Positive Voltage Can Be Applied Via a Scaling Resistor

8

Pin Configuration



Note:
Do not make connections to pin 1, 2, 3 or 4 on 8703; pin 1 or 2 on 8704. These pins are internally connected.

Handling Precautions

The 8700 series are CMOS devices must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static tubes or other conductive material. Use proper anti-static handling procedures. Do not connect in circuits under "power on" conditions, as high transients may cause permanent damage.

Absolute Maximum Ratings

Storage Temperature ..... -65°C to + 150°C
Operating Temperature
(BL, BN) ..... -55°C to +125°C
(CL) Package ..... -40°C to + 85°C
(CJ) Package ..... 0° to + 70°C
V_{DD} -V_{SS} ..... 18 V

I_{IN} ..... ±10 mA
I_{REF} ..... ±10 mA
Digital Input Voltage ..... -0.3 to V_{DD} +0.3 V
Operating V_{DD} and V_{SS} Range ..... 3.5 V to 7 V
Package Dissipation ..... 500 mW
Lead Temperature ..... 300°C
(Soldering, 10 seconds)

Electrical Characteristics: Unless otherwise specified, V_{DD} = +5 V, V_{SS} = -5 V, V_{GND} = 0, V_{REF} = -6.4 V, R_{BIAS} = 100 kΩ, test circuit shown. T_A = 25°C unless Full Temperature Range is specified (-55°C to +125°C for BN and BL package, -40°C to +85°C for CL package, 0° to 70°C for CJ package).

PARAMETER	CONDITIONS	DEFINITION	MIN	TYP	CJ/CN MAX	BN/BL MAX	UNITS
Accuracy							
Resolution		Binary Word Length Of Digital Output					
Accuracy		TSC8703	8	—	—	—	Bits
		TSC8704	10	—	—	—	Bits
		TSC8705	12	—	—	—	Bits
Relative Accuracy		Output Deviation From Straight Line Between Normalized Zero and Full-Scale Input	—	±1/4	±1/2	±1/2	LSB
		TSC8705CJ (Only)	—	1.0	±1.5		LSB
Differential Non-Linearity		Deviation From 1 LSB Between Transition Points	—	±1/4	±1/2	±1/2	LSB
Differential Non-Linearity Temperature Drift	Full Temperature Range	Variation in Differential Non-Linearity Due To Temperature Change	—	±2.5	±5	±5	ppm/°C
Gain Variance		Variation From Exact A (Compensate By Trimming R_{IN} or R_{REF})		±2	±5	±5	% of Nominal
Gain Temperature Drift	Full Temperature Range	Variation In A Due To Temperature Change	—	±25	±75	±80	ppm/°C
Zero Offset (TSC8703)	I_{IN} = 0 C_{INT} = 68 pF R_{ADJ} = 1.6 kΩ See Test Circuit.	Correction at Zero Adjust to Give Zero Output When Input Is Zero Integration Cap. = 68 pF R_{ADJ} = 1.6 kΩ	—	—	±80	±80	mV
Zero Offset (TSC8703)	I_{IN} = 0 C_{INT} = 33 pF R_{ADJ} = 1.0 kΩ See Test Circuit.	Correction at Zero Adjust to Give Zero Output When Input Is Zero Integration Cap. = 33 pF R_{ADJ} = 1.0 kΩ	—	±10	±50	±50	mV
Zero Offset (TSC8704) (TSC8705)	I_{IN} = 0 C_{INT} = 68 pF R_{ADJ} = 1.0 kΩ See Test Circuit.	Correction at Zero Adjust to Give Zero Output When Input Is Zero Integration Cap. = 68 pF R_{ADJ} = 1.0 kΩ	—	±10	±50	±50	mV
Zero Temperature Drift	Full Temperature Range	Variation in Zero Offest Due to Temperature Change	—	±3	±5	±8	ppm/°C
Analog Inputs							
I_{IN} Full-Scale		Full-Scale Analog Input Current To Achieve Specified Accuracy	—	10	—	—	μA
I_{REF} (Note 1)		Reference Current Input To Achieve Specified Accuracy	—	-20	—	—	μA
Digital Inputs							
$V_{IN}^{(1)}$	Full Temperature Range	Logical "1" Input Threshold For Initiate Conversion Input	3.5	—	—	—	V
$V_{IN}^{(0)}$	Full Temperature Range	Logical "0" Input Threshold For Initiate Conversion Input	—	—	1.5	1.5	V
Propagation Delay							
Output Enable	C_L = 100 pF, R_L = 1 KΩ	T_{PLH}, T_{PHL}	—	500	—	1,000	ns

Electrical Characteristics (Cont.)

PARAMETER	CONDITIONS	DEFINITION	MIN	TYP	CJ/CN MAX	BN/BL MAX	UNITS
Digital Outputs							
$I_{O(OFF)}$	OE = 3.5 V, 0.4 V < V_C <2.4	Off-state Output Current	—	0.1	±10	±10	μA
V_{OUT}[1]	Full Temp. Range	Logical "1" Output Voltage	4.5	—	—	—	V
	I_{OUT} = -10 μA	For Digits Out, Busy, and	2.4	—	—	—	V
	I_{OUT} = -500 μA	Data Valid Outputs					
V_{OUT}[0]	Full Temp. Range	Logical "0" Output Voltage	—	—	0.4	0.4	V
	V_{DD} = 4.75 V	For Digits Out, Busy, and					
	I_{OUT} = 500 μA	Data Valid Outputs					
Dynamic							
Conversion Time	Full Temp. Range	Time Required to Perform One Complete A/D Conversion					
		TSC8703	—	1.25	1.8	1.8	ms
		TSC8704	—	5	6	6	ms
		TSC8705	—	20	24	24	ms
Conversion Rate in Free-Run Mode	$V_{INT\ CONV}$ = + 5 V	TSC8703	555	800	—	—	Conv'ns per Second
		TSC8704	167	200	—	—	
		TSC8705	42	50	—	—	
Minimum Pulse Width for Initiate Conversion	Full Temp. Range		500	—	—	—	ns
Supply Current							
I_{DD} Quiescent	Full Temp. Range	Current Required From Positive	—	1.4	2.5	3.5	mA
(L/N Package)	$V_{INT\ CONV}$ = 0V	Supply During Operation	—	1.4	5.0		mA
(J Package)							
I_{SS} Quiescent	Full Temp. Range	Current Required From Negative	—	-1.6	-2.5	-3.5	mA
(L/N Package)	$V_{INIT\ CONV}$ = 0V	Supply During Operation	—	-1.6	-5.0		mA
(J Package)							
Supply Sensitivity	V_{DD} ± 1 V, V_{SS} ±1 V	Change in Full-Scale Gain vs Supply Voltage Change	—	±0.5	±1.0	±1.0	%/V
	$\|V_{DD}\| = \|V_{SS}\|$ = 5 V ± 1 V	Change in Full-Scale Gain vs Supply Voltage Change for Tracking Supplies	—	±0.05	±0.1	±0.1	%/V

NOTE:
I_{IN} and I_{REF} pins connect to the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors. See Test Circuit.

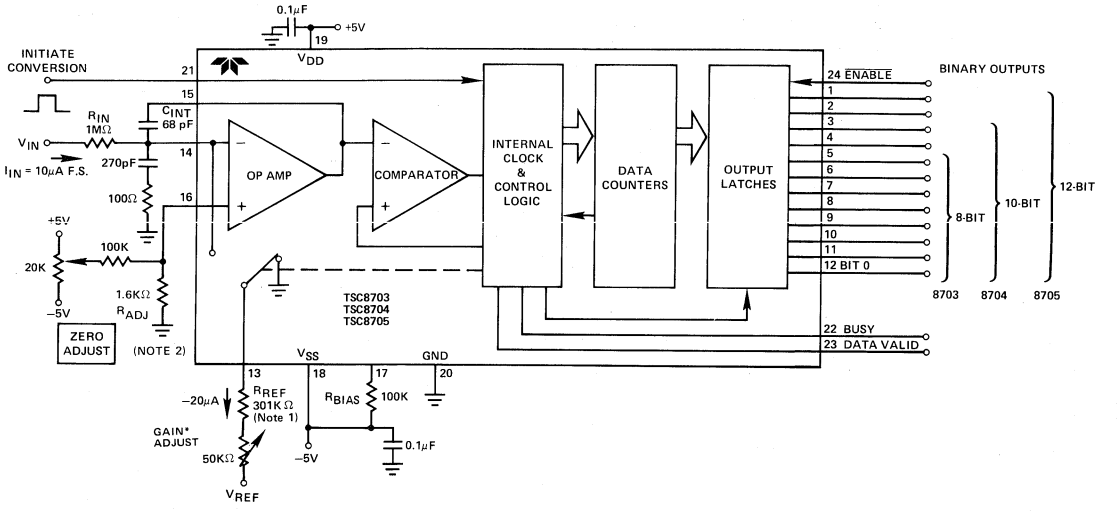
Circuit Description

During conversion the sum of a continuous current I_{IN} and pulses of a reference current I_{REF} is integrated for a fixed number of clock periods. I_{IN} is proportional to the analog input voltage; I_{REF} is switched in for exactly one clock period just frequently enough to maintain the output of the integrator near zero. Thus, the charge from the continuous I_{IN} current is balanced against the pulses of I_{REF} current. The total number of I_{REF} pulses needed during the conversion period to maintain the charge balance is counted, and the result (in Binary) is latched into the outputs at the end of the conversion.

The converter contains two counters and a clock in addition to an operational amplifier, comparator, latching output buffers and housekeeping logic. One counter is a clock counter which (after a reset pulse) starts counting clock pulses; when the required count is reached, the clock counter generates a pulse to start the end-of-conversion routine. The other counter is a data counter, which is reset synchronously with the clock counter and counts the number of times the I_{REF} current is switched into the summing input of the amplifier during the period defined by the clock counter.

When the Initiate Conversion input is strobed with a positive signal, the busy line latches high and a 10 μs (times given are approximate) start up cycle begins. The integrating capacitor is discharged and both counters are reset during this start up period. Conversion begins at the end of the reset pulse and ends with a pulse generated either by the clock counter or by an overflow condition in the data counter. This pulse disables further inputs into both counters and triggers a 10 μs shutdown cycle. During the shutdown cycle Data Valid goes low for 5 μs. This binary sequence is shown in the timing diagrams. Busy is true high, and when the circuit is busy, Initiate Conversion has no effect and may be high or low. Data Valid is also true high. The data from a conversion remain valid for as long as power is applied to the circuit or until Data Valid falls at the end of a subsequent conversion, at which time the output data are updated to reflect the latest conversion.

Test Circuit



Note:

1. Any V_{REF} greater than -1 V can be used.

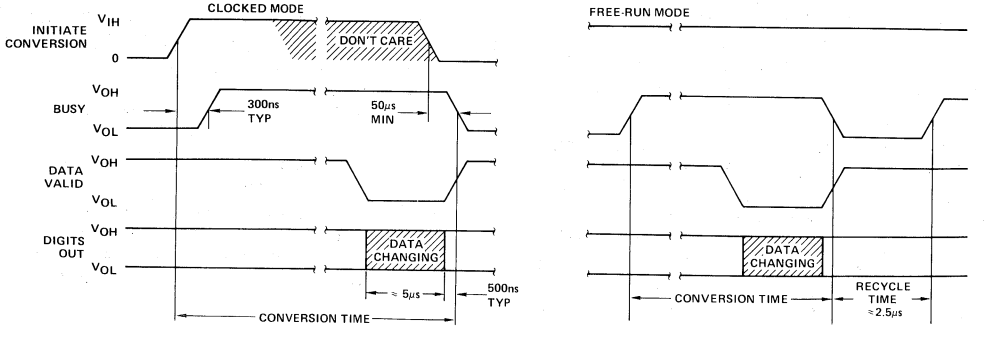
$$R_{REF} = \frac{V_{REF}}{-20\ \mu A}$$

For example with V_{REF} = -5 V, R_{REF} = 250 k.

2.

Part No.	R_{ADJ}	C_{INT}	Zero Offset Spec
TSC8703	1.6 kΩ	68 pF	±80 mV
TSC8703	1.0 kΩ	33 pF	±50 mV
TSC8704/8705	1.0 kΩ	68 pF	±50 mV

Timing Diagrams (Rise, fall times = 200 ns typ., C_L = 50 pF)



Pin Functions

Initiate Conversion Input

Accepts CMOS and most 5 V logic inputs. Applying a logic "1" to the Initiate Conversion pin initiates the A/D conversion cycle. Once conversion has been initiated, the cycle cannot be interrupted, and the Initiate Conversion pin is disabled until conversion is complete. Two modes of operation are permitted, clocked or free-running. For clocked operation the Initiate Conversion input is held at logic "0" for standby and taken to logic "1" when a conversion is desired. For free-running operation the Initiate Conversion pin is connected to V_{DD} or similar permanent logic "1" voltage.

Busy Output

A digital status output which is compatible with CMOS logic and low power TTL (can sink and source 500 μA). A logic "1" output on the Busy pin indicates a conversion cycle is in process. A logic "1" to logic "0" transition indicates that conversion is complete and the result has been latched at the Digits Out pins. A logic "0" to logic "1" transition indicates a new conversion cycle has been initiated. If the device is operating in the free-running mode, the Busy output will remain low for approximately 2.5 μs, marking the completion and initiation of consecutive conversion cycles.

Data Valid Output

A digital status which is compatible with CMOS logic and low power TTL (can sink and source 50 μA). A logic "1" output at the Data Valid pin indicates that the Digits Out pins are latched with the result of the last conversion cycle. The Data Valid output goes to logic "0" approximately 5 μs before the completion of a conversion cycle. During this 5 μs interval new data is being transferred to the Digits Out pins, and the Digits Out are not valid.

Digits Out

(Bit 0, Bit 1, etc.)

The binary digit outputs which are the result of the A/D conversion. These outputs are CMOS logic and low power TTL compatible.

Applications Information

Input/Output Relationships

The analog input voltage (V_{IN}) is related to the output by the transfer equation:

$$\text{Digital Counts} = \frac{V_{IN} \cdot A \cdot R_{REF}}{R_{IN} \cdot V_{REF}}$$

A = 528 for 8703
A = 2064 for 8704
A = 8208 for 8705

where Digital Counts is the value of the binary output word presented at Digits Out pins in response to V_{IN}.

The digital output code format is as follows:

Analog Input	Digital Output MSB ... LSB
$V_{IN} \leq$ Full-Scale	1 . . . 111 . . . 1
= Full-Scale -1 LSB	1 . . . 111 . . . 1
= 1 LSB	0 . . . 000 . . . 1
≤ 0	0 . . . 000 . . . 0

Two's complement coding can be generated by inverting the Most Significant Bit (MSB) signal.

External Component Selection

Obtaining a high accuracy conversion system depends on the voltage regulation of V_{REF} and the thermal stability of R_{IN} and R_{REF}. The exact dependence is given by the transfer function. System accuracy also depends, to a lesser degree, on the voltage regulation of V_{DD} and V_{SS}. The supply connections V_{DD} and V_{SS} should have bypass capacitors of value 0.1 μF or larger right at the device pins.

8

R_{IN}, R_{EF}

Values of these components are chosen to give a full-scale input current of approximately 10 μA and a reference current of approximately -20 μA.

$$R_{IN} \cong \frac{V_{IN}\ \text{Full-Scale}}{10\ \mu A} \qquad R_{REF} \cong \frac{V_{REF}}{-20\ \mu A}$$

Examples:

$$R_{IN} \cong \frac{10\ V}{10\ \mu A} = 1\ M\Omega \qquad R_{REF} \cong \frac{-6.4\ V}{-20\ \mu A} = 320\ k\Omega$$

Note that these values are approximations, and the exact relationships are defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed using the optional gain adjust circuit to obtain full-scale output at V_{IN} full-scale (see adjustment procedure). Metal film resistors with 1% tolerance or better are recommended for high accuracy applications because of their thermal stability and low noise generation.

R_{BIAS}

Specifications for the 87XX are based on R_{BIAS} = 100 kΩ $\pm$10% unless otherwise noted. However, there are instances when the designer may want to change this resistor in order to affect the conversion time and the supply current. By decreasing R_{BIAS} the A/D will convert much faster and the supply current will be higher. (For example: When R_{BIAS} is 20 k the conversion time is reduced by 1/3, and the supply current will increase from 2 mA to 7 mA.) Likewise, if the R_{BIAS} is increased the conversion time will be longer and the supply current will be much lower. (For example: When R_{BIAS} = 1 mΩ the conversion time will be six times longer, and supply current is now reduced to .5 mA). For details of this relationship refer to AN9 typical performance curves.

Applications Information (Cont.)

R_{DAMP}

Exact value not critical but should have a nominal value of 100 Ω ±10%. Locate close to pin 14.

C_{DAMP}

Exact value not critical but should have a nominal value of 270 pF ±20%. Locate close to pin 14.

C_{INT}

Exact value not critical but should have a nominal value of 68 pF ± 10%. Low leakage types are recommended, although mica or ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 14, 15. For the TSC8703 C_{INT} = 33 pF is adequate with R_{ADJ} = 1 kΩ.

V_{REF}

A negative reference voltage must be supplied. This may be obtained from a constant current source circuit or from the negative supply.

V_{DD}, V_{SS}

Power supplies of ±5 V are recommended, with 0.05% line and load regulation and 0.1 μF decoupling capacitors.

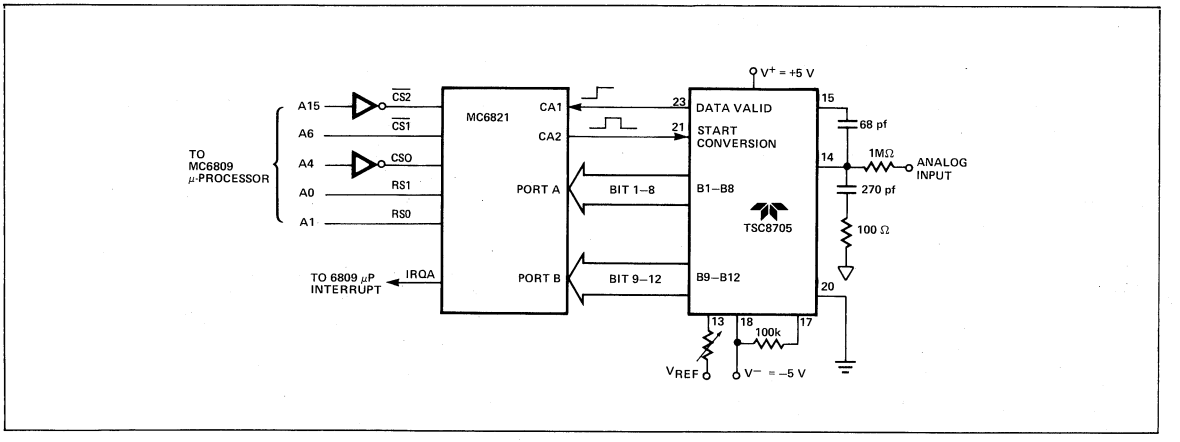
Adjustment Procedure

The test circuit diagram shows optional circuits for trimming the zero location and full-scale gain. Because the digital outputs remain constant outside of the normal operating range (i.e. below zero and above full-scale), it is recommended that transition points be used in setting the zero and full-scale values. Recommended procedure is as follows:

- Set the initiate conversion control high to provide free-run operation and verify that converter is operating.
- Set V_{IN} to +1/2 LSB and trim the zero adjust circuit to obtain a 000 . . . 000 . . . to 000 . . . 001 transition. This will correctly locate the zero end.
- For full-scale adjustment, set V_{IN} to the full-scale value less 1 1/2 LSB and trim the gain adjust circuit for a 111 . . . 110 to 111 . . . 111 transition.

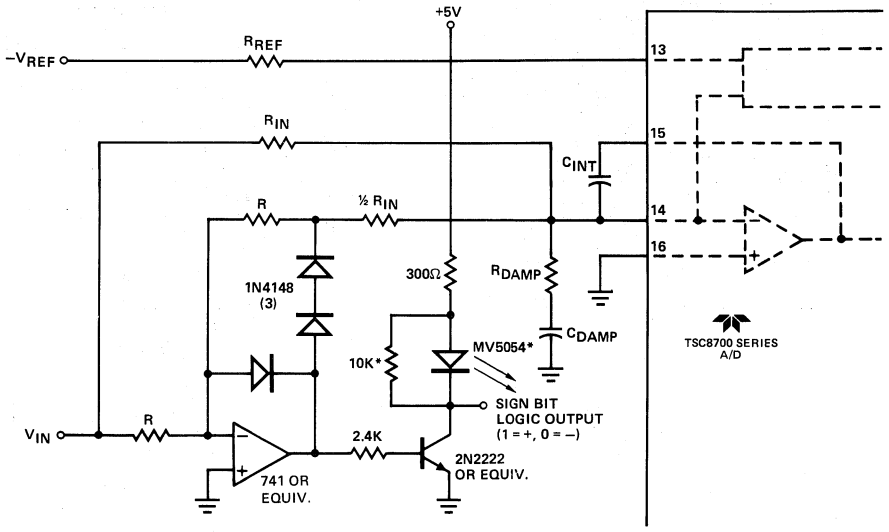
If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

TSC8705 Interface to MC6821 PIA



Application/Design Circuits

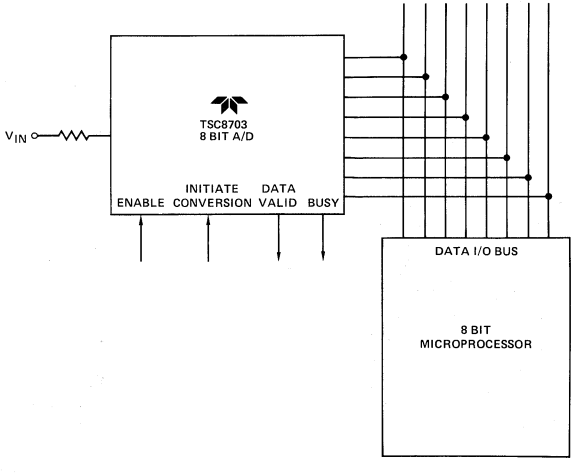
Bipolar Operation (+ and −Inputs)



*Optional visual indication of negative input
NOTE: Values for R should be between 10KΩ and 100KΩ

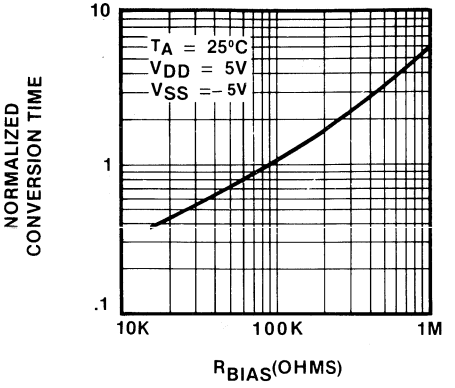
Absolute Value Circuit With Sign

8-Bit Microprocessor Interface

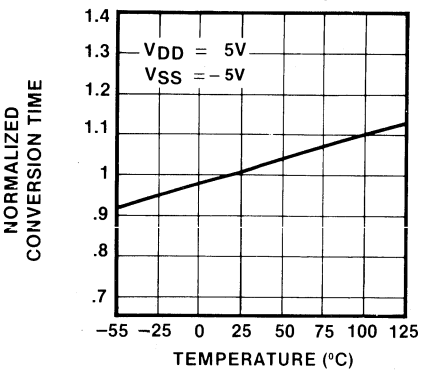


TYPICAL PERFORMANCE CURVES

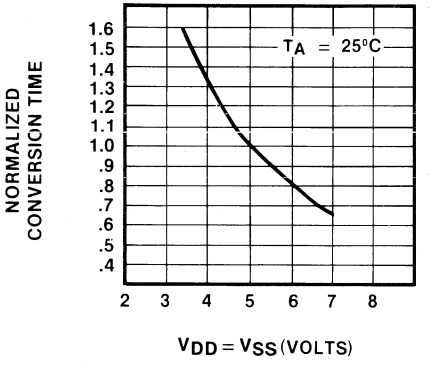
CONVERSION TIME vs R_{BIAS}



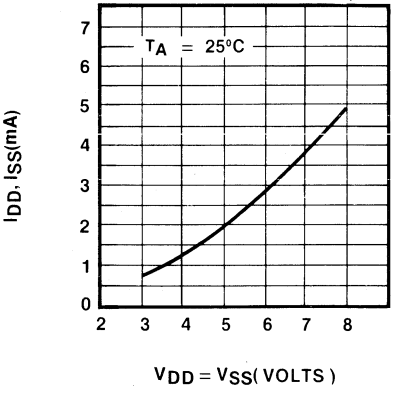
CONVERSION TIME vs TEMPERATURE



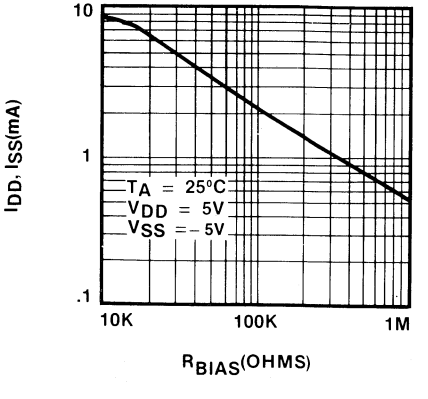
CONVERSION TIME vs SUPPLY VOLTAGE



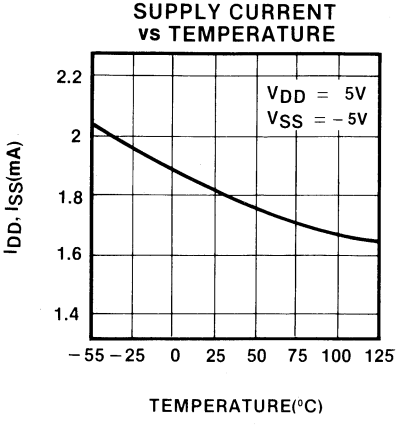
SUPPLY CURRENT vs SUPPLY VOLTAGE



SUPPLY CURRENT vs R_{BIAS}

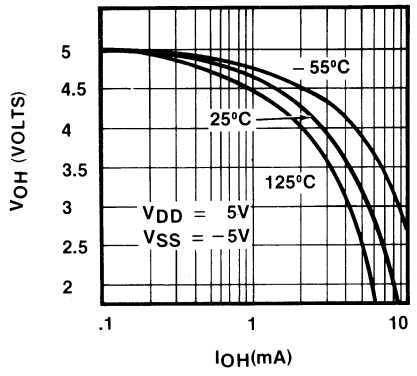


SUPPLY CURRENT vs TEMPERATURE

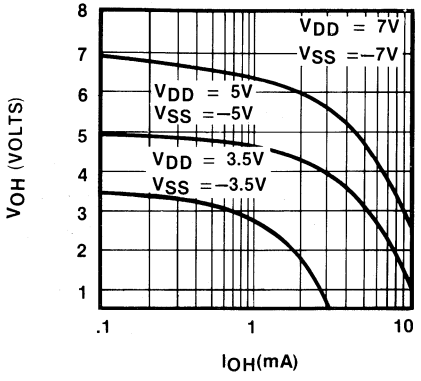


TYPICAL PERFORMANCE CURVES

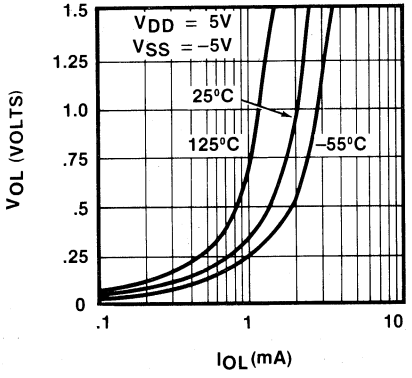
OUTPUT SOURCE CURRENT vs TEMPERATURE



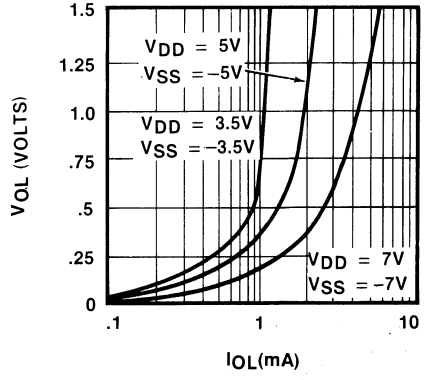
OUTPUT SOURCE CURRENT vs SUPPLY VOLTAGE



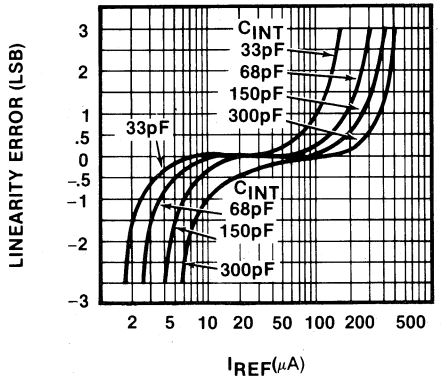
OUTPUT SINK CURRENT vs TEMPERATURE



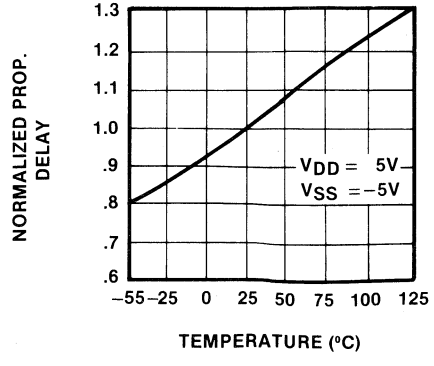
OUTPUT SINK CURRENT vs SUPPLY VOLTAGE



LINEARITY vs I_{REF}

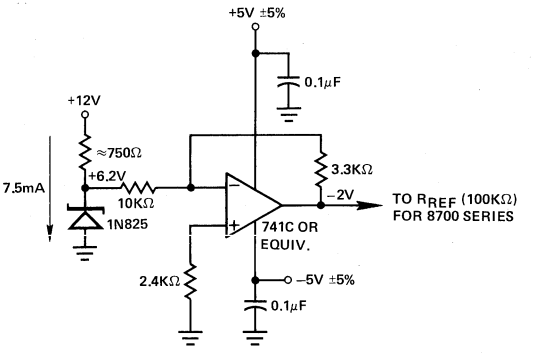


TRI-STATE PROPAGATION DELAY



Application/Design Circuits (Cont.)

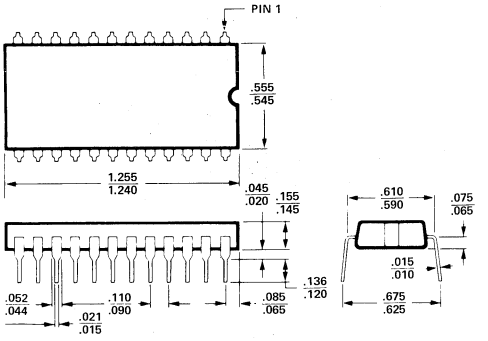
Reference Voltage Supply



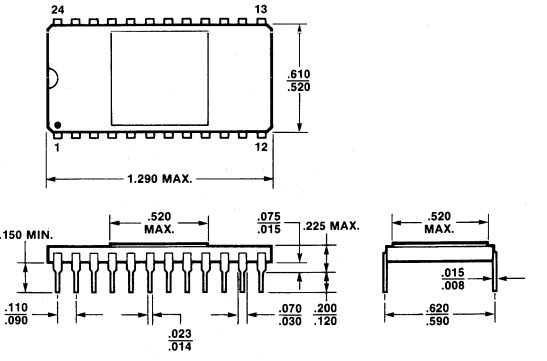
2 V Reference Voltage Using Voltages Derived from 8080A μP.

Package Information

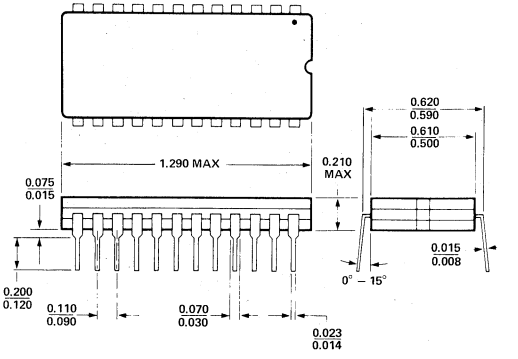
24-Pin Plastic Dip (J Package)
(Package #12)

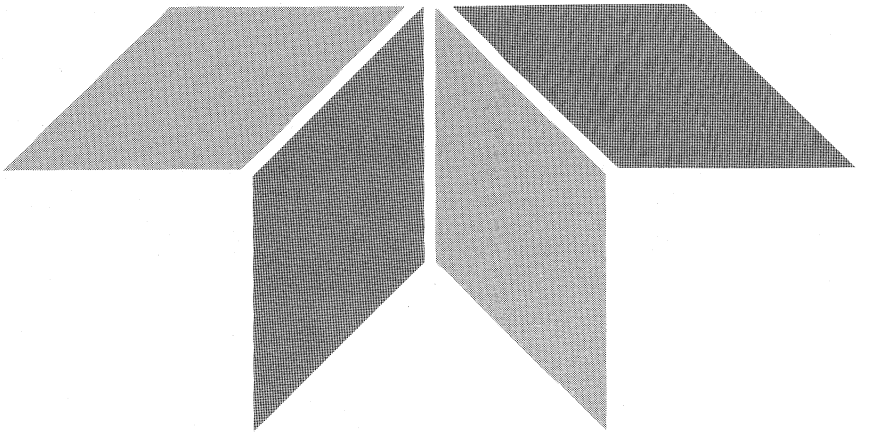


24-Pin Ceramic Dip (N Package)
(Package #13)



24-Pin CerDIP (L Package)
(Package #14)





SECTION 9

V/F, F/V Converters

Section 9
Voltage to Frequency/Frequency to Voltage Converters 9-1

TSC9400 (0.05% Linearity) 9-3
TSC9401 (0.01% Linearity) 9-3
TSC9402 (0.25% Linearity) 9-3

TELEDYNE SEMICONDUCTOR

TSC9400 (0.05%)
TSC9401 (0.01%)
TSC9402 (0.25%)
Voltage to Frequency/ Frequency to Voltage Converters

General Description

The TSC9400/9401/9402 are low cost Voltage-to-Frequency converters combining Bipolar and CMOS technology on the same substrate. The converters accept a variable analog input signal and generate an output pulse train whose frequency is linearly proportional to the input voltage.
The devices can also be used as highly accurate Frequency-to-Voltage converters, accepting virtually any input frequency waveform and providing a linearly proportional voltage output.
A complete V/F or F/V system requires the addition of two capacitors , three resistors and reference voltage.

Applications

• Voltage-to-Frequency

- — Temperature Sensing and Control
- — μP Data Acquisition
- — Instrumentation
- — 13-Bit A/D Converters
- — Digital Panel Meters
- — Analog Data Transmission and Recording
- — Phase Locked Loops
- — Medical Isolation
- — Transducer Encoding
- — Alternate to 555 Astable Timer

• Frequency-to-Voltage

- — Frequency Meters/Tachometer
- — Speedometers
- — Analog Data Transmission and Recording
- — Medical Isolation
- — Motor Control
- — RPM Indicator
- — FM Demodulation
- — Frequency Multiplier/Divider
- — Flow Measurement and Control

Features

• Voltage-to-Frequency

- — 1Hz to 100kHz Operation
- — Choice of Guaranteed Linearity:
  TSC9401 .01%
  TSC9400 .05%
  TSC9402 .25%
- — ±25ppm/° C Typ. Gain Temperature Stability
- — Open Collector Output
- — Output can Interface with any Form of Logic
- — Pulse and Square Wave Outputs
- — Programmable Scale Factor
- — Low Power Dissipation (27mW Typ.)
- — Single Supply Operation (8V to 15V)
- — Dual Supply Operation (±4V to ±7.5V)
- — Current or Voltage Input

• Frequency-to-Voltage

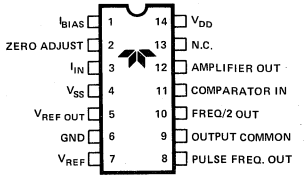
- — DC to 100kHz Operation
- — Choice of Guaranteed Linearity:
  TSC9401 0.02%
  TSC9400 0.05%
  TSC9402 0.25%
- — Op Amp Output
- — Programmable Scale Factor
- — High Input Impedance (>10MΩ)
- — Accepts any Voltage Wave Shape

HANDLING PRECAUTIONS: The 9400 Series are CMOS Bipolar devices and must be handled correctly to prevent damage. Package and store only in conductive foam, antistatic tubes or other conductive material. Use proper antistatic handling procedures. Do not connect in circuits under "power on" conditions, as high transients may cause permanent damage.

Ordering Information

Part No.	Linearity (V/F)	Package	Temperature Range
TSC9400CJ	0.05%	14-Pin Plastic Dip	0° C to +70° C
TSC9400CL	0.05%	14-Pin CerDIP	-40° C to +85° C
TSC9401CJ	0.01%	14-Pin Plastic Dip	0° C to +70° C
TSC9401CL	0.01%	14-Pin CerDIP	-40° C to +85° C
TSC9402CJ	0.25%	14-Pin Plastic Dip	0° C to +70° C
TSC9402CL	0.25%	14-Pin CerDIP	-40° C to +85° C

Pin Configuration



NOTE: PIN 1 INDICATED BY ADJACENT DOT (N PACKAGE), INDENT OR END NOTCH (J PACKAGE).

Absolute Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Operating Temperature
J Package ..... 0°C to 70°C
L Package ..... -40°C to +85°C
$V_{DD} - V_{SS}$ ..... 18 V

I_{IN} ..... 10 mA
V_{OUT} Max — V_{OUT} Common ..... 25 V
$V_{REF} - V_{SS}$ ..... -1.5 V
Package Dissipation ..... 500 mW
Lead Temperature (Soldering, 10 sec) ..... 300°C

Electrical Characteristics, V/F Mode

Unless otherwise specified, V_{DD} = +5V, V_{SS} = —5V, V_{GND} = 0, V_{REF} = —5V, R_{BIAS} = 100KΩ, Full Scale = 10KHz. T_A = 25°C unless Full Temp. Range is specified (—40°C to +85°C for L package, 0°C to 70°C for J package).

VOLTAGE-TO-FREQUENCY		TSC9401			TSC9400			TSC9402				
Parameter	**Definition**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**	**Notes**
Accuracy Linearity (10KHz)	Output Deviation from Straight Line between Normalized Zero and Full Scale Input		0.004	**0.01**		0.01	**0.05**		0.05	**0.25**	% Full Scale	
Linearity (100KHz)			0.04	0.08		0.1	0.25		0.25	0.50	% Full Scale	
Gain Temperature Drift	Variation in Gain (A) due to Temperature Change		±25	±40		±25	±40		±50	±100	ppm/°C Full Scale	1
Gain Variance	Variation from Exact A (Compensate by Trimming R_{IN}, V_{REF}, or C_{REF})		±10			±10			±10		% of Nominal	
Zero Offset	Correction at Zero Adjust for Zero Output When Input is Zero		±10	±50		±10	±50		±20	±100	mV	2
Zero Temperature Drift	Variation in Zero Offset Due to Temperature Change		±25	±50		±25	±50		±50	±100	μV/°C	1
Analog Inputs I_{IN} Full Scale	Full Scale Analog Input Current to Achieve Specified Accuracy		10			10			10		μA	
I_{IN} Overrange	Overrange Current			50			50			50	μA	
Response Time	Settling Time to 0.01% Full Scale		2			2			2		Cycles	
Digital Outputs V_{SAT} @ I_{OL}=10μA	Logical "0" Output Voltage			0.4			0.4			0.4	V	3
V_{OUT} Max. — V_{OUT} Common	Voltage Range between Output and Common			18.0			18.0			18.0	V	4
Pulse Frequency Output Width			3.0			3.0			3.0		μsec	
Supply Current I_{DD} Quiescent (L Package) (J Package)	Current Required from Positive Supply During Operation		2.0 2.0	4.0 6.0		2.0 2.0	4.0 6.0		3.0	10.0	mA mA	9
I_{SS} Quiescent (L Package) (J Package)	Current Required from Negative Supply During Operation		-1.5 -1.5	-4.0 -6.0		-1.5 -1.5	-4.0 -6.0		-3.0	-10.0	mA mA	10
V_{DD} Supply	Operating Range of Positive Supply	4.0		7.5	4.0		7.5	4.0		7.5	V	
V_{SS} Supply	Operating Range of Negative Supply	-4.0		-7.5	-4.0		-7.5	-4.0		-7.5	V	
Reference Voltage V_{REF}—V_{SS}	Range of Voltage Reference Input	-1.0			-1.0			-1.0			V	

NOTES:
1. Full temperature range.
2. I_{IN} = 0.
3. Full temperature range, I_{OUT} = 10mA.
4. I_{OUT} = 10μA.
5. 10Hz to 100KHz.
6. 5μs min. positive pulse width and 0.5μs min. negative pulse width.
7. $T_r = t_f$ = 20ns.
8. $R_L \geq 2K\Omega$.
9. Full temperature range, V_{IN} = -0.1V.
10. V_{IN} = -0.1V.
11. I_{IN} connects the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors.

V/F Circuit Description

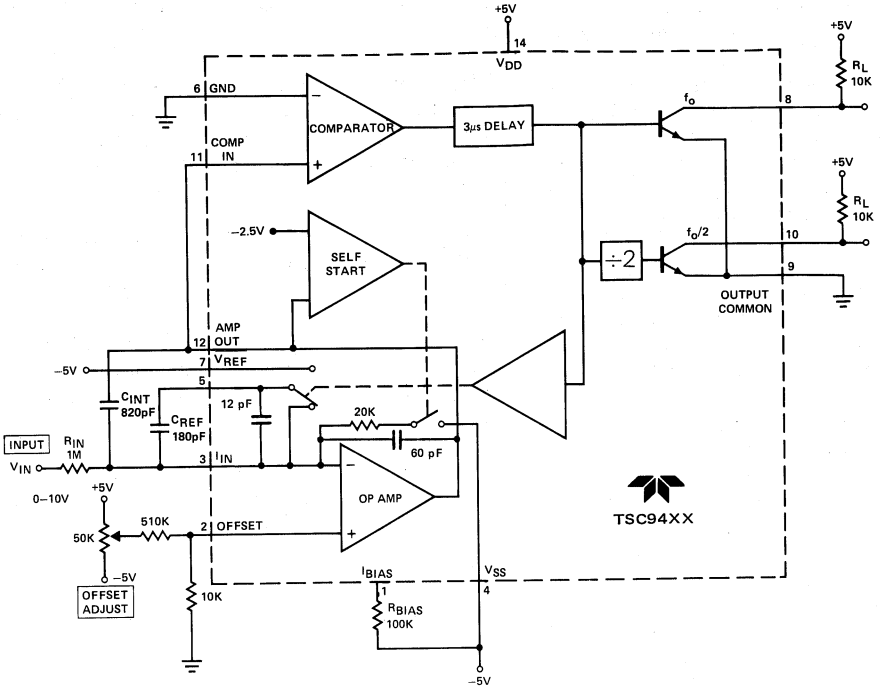
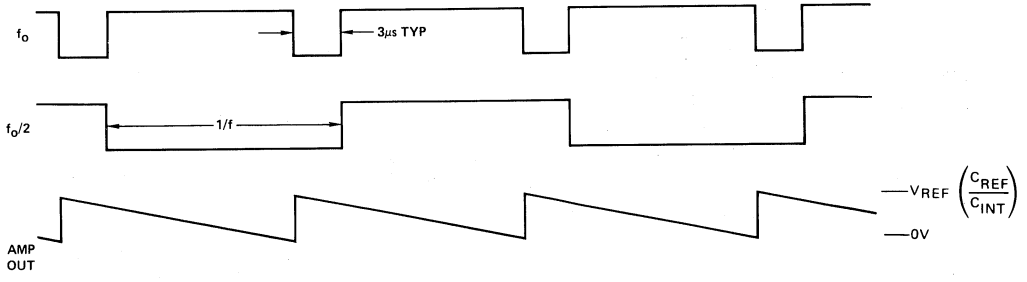


Figure 1. 10Hz to 10KHz V/F Converter



1. To adjust f_{min}, set V_{IN}=10mV and adjust the 50K offset for 10Hz out.
2. To adjust f_{max}, set V_{IN} =10V and adjust R_{IN} or V_{REF} for 10KHz out.
3. To increase f_{OUT}MAX to 100KHz change C_{REF} to 27pF and C_{INT} to 75pF.
4. For high performance applications use high stability components for R_{IN}, C_{REF}, V_{REF} (metal film resistors and glass film capacitors). Also separate the output ground (Pin 9) from the input ground (Pin 6).

Figure 2. Output Waveforms

V/F Circuit Description (Contd.)

The Teledyne 9400 V/F Converter operates on the principal of charge balancing. The input voltage (V_{IN}) is converted to a current (I_{IN}) by the input resistor. This current is then converted to a charge by the integrating capacitor and shows up as a linearly decreasing voltage at the output of the op amp. The zero crossing of the output is sensed by the comparator causing the reference voltage to be applied to the reference capacitor for a time period long enough to virtually charge the capacitor to the reference voltage. This action reduces the charge on the integrating capacitor by a fixed amount ($q = C_{REF} \times V_{REF}$) causing the op amp output to step up a finite amount.

At the end of the charging period, C_{REF} is shorted out dissipating the stored reference charge so that when the output again crosses zero, the system is ready to recycle. In this manner, the continued discharging of the integrating capacitor by the input is balanced out by fixed charges from the reference voltage. As the input voltage is increased, the number of reference pulses required to maintain balance increases causing the output frequency to also increase. Since each charge increment is fixed the increase in frequency with voltage is linear. In addition, the accuracy of the output pulses does not directly effect the linearity of the V/F. It must simply be long enough for full charge transfer to take place.

The 9400 contains a "self-start" circuit to assure that the V/F will always operate properly when power is first applied. In the event that during "Power-on" the op amp output is below the comparator threshold and C_{REF} is already charged, a positive voltage step will not occur. The op amp output will continue to decrease until it crosses the −2.5 volt threshold of the "self-start" comparator. When this happens a resistor is connected to the op amp input causing the output to quickly go positive until the 9400 is once again in its normal operating mode.

The 9400 utilizes both bipolar and MOS transistors on the same substrate, taking advantage of the best features of each. MOS transistors are used at the inputs to reduce offset and bias currents. Bipolar transistors are used in the op amp, for high gain, and on all outputs for excellent current driving capabilities. CMOS logic is used throughout to minimize power consumption.

Pin Functions

Comparator Input — In the V/F mode, this input is connected to the amplifier output (pin 12) and triggers the 3μsec pulse delay when the input voltage passes its threshold. In the F/V mode, the input frequency is applied to the comparator input.

Pulse Freq Out — This output is an open-collector bipolar transistor providing a pulse waveform whose frequency is proportional to the input voltage. This output requires a pull up resistor and interfaces directly with MOS, CMOS and TTL logic.

Freq/2 Out — This output is an open-collector bipolar transistor providing a square wave that is one-half the frequency of the pulse frequency output. This output requires a pull up resistor and interfaces directly with MOS, CMOS, and TTL logic.

Output Common — The emitters of both the freq/2 out and the pulse freq out are connected to this pin. An output level swing from the collector voltage to ground or to the V_{SS} supply may be obtained by connecting to the appropriate point.

R_{BIAS} — Specifications for the 9400 are based on R_{BIAS} = 100K ±10% unless otherwise noted. R_{BIAS} may be varied between the range of $82K \leq R_{BIAS} \leq 120K$.

Amplifier Out — The output stage of the operational amplifier. A negative going ramp signal is available at this pin in the V/F mode. In the F/V mode a voltage proportional to the frequency input is generated.

Zero Adjust — The non-inverting input of the operational amplifier. The low frequency set point is detemined by adjusting the voltage at this pin.

I_{IN} — The inverting input of the operational amplifier and the summing junction when connected in the V/F mode. An input current of 10μA is specified for nominal full scale but an over range current up to 50μA can be used without detrimental effect to the circuit operation.

V_{REF} — A reference voltage from either a precision source or the V_{SS} supply may be applied to this pin. Accuracy will be dependent on the voltage regulation and temperature characteristics of the circuitry.

V_{REF} OUT — The charging current for C_{REF} is derived from the internal circuitry and switched by the break-before-make switch to this pin.

V/F Design Information

Input/Output Relationships — The output frequency is related to the analog input voltage (V_{IN}) by the transfer equation:

$$\text{Frequency Out} = \frac{V_{IN}}{R_{IN}} \times \frac{1}{(V_{REF})(C_{REF})} = f_o$$

External Component Selection

R_{IN} — The value of this component is chosen to give a full scale input current of approximately 10μA.

$$R_{IN} \cong \frac{V_{IN\ FULL\ SCALE}}{10\mu A}$$

Example:

$$R_{IN} \cong \frac{10V}{10\mu A} = 1M\Omega$$

V/F Design Information (Contd.)

Note that the value is an approximation, and the exact relationship is defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed to obtain full scale frequency at V_{IN} FULL SCALE (see adjustment procedure). Metal film resistors with 1% tolerance or better are recommended for high accuracy applications because of their thermal stability and low noise generation.

C_{INT} – Exact value not critical but is related to C_{REF} by the relationship:

$$3C_{REF} \leq C_{INT} \leq 10C_{REF}$$

Improved stability and linearity is obtained when $C_{INT} \geq 4C_{REF}$. Low leakage types are recommended although mica and ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 12 and 3.

C_{REF} – Exact value not critical and may be used to trim the full scale frequency (see input/output relation). Glass film or air trimmer capacitors are recommended because of their stability and low leakage. Locate as close as possible to pins 5 and 3.

V_{DD}, V_{SS} – Power supplies of ±5V are recommended. For high accuracy requirements 0.05% line and load regulation and 0.1μF disc decoupling capacitors located near the pins are recommended.

Adjustment Procedure – Figure 1 shows a circuit for trimming the zero location. Full scale may be trimmed by adjusting R_{IN}, V_{REF}, or C_{REF}. Recommended procedure is as follows for a 10KHz full scale frequency.

1. Set V_{IN} to 10mV and trim the zero adjust circuit to obtain a 10Hz output frequency.
2. Set V_{IN} to 10.000V and trim either R_{IN}, V_{REF}, or C_{REF} to obtain a 10KHz output frequency.

If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

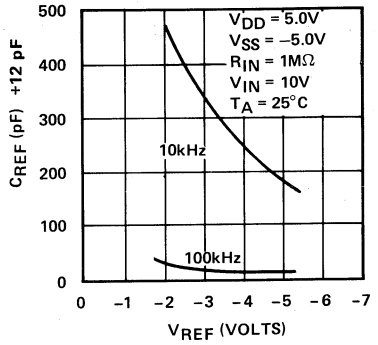


Figure 3. Recommended C_{REF} vs V_{REF}

V/F Single Supply Operation

NOTE:
See Also the TSC7660
Data Sheet;

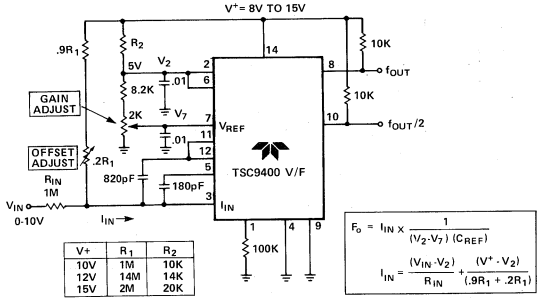


Figure 4. Fixed Voltage–Single Supply Operation

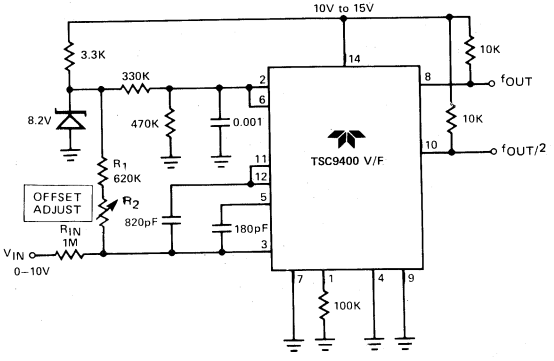


Figure 5. Variable Voltage–Single Supply Operation

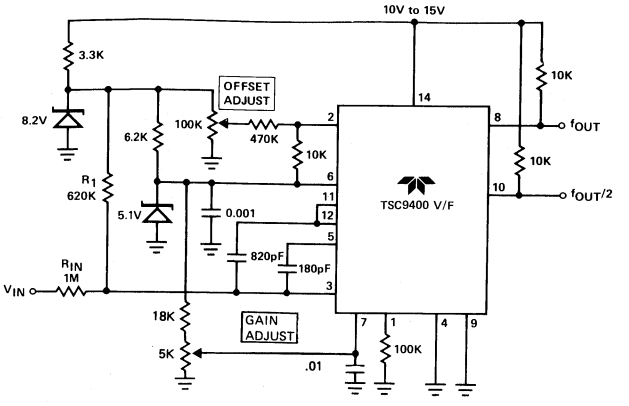


Figure 6. Single Variable Supply Voltage with Offset and Gain Adjust

Electrical Characteristics, F/V Mode

Unless otherwise specified, V_{DD} = +5V, V_{SS} = —5V, V_{GND} = 0, V_{REF} = —5V, R_{BIAS} = 100KΩ, Full Scale = 10KHz. T_A = 25°C unless Full Temp. Range is specified (—40°C to +85°C for L package, 0°C to 70°C for J package).

FREQUENCY-TO-VOLTAGE		TSC9401			TSC9400			TSC9402				
Parameter	**Definition**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Units**	**Notes**
Accuracy Non-Linearity	Deviation from Ideal Transfer Function as a Percentage of Full Scale Voltage		0.01	**0.02**		0.02	**0.05**		0.05	**0.25**	% Full Scale	5
Input Frequency Range	Frequency Range for Specified Non-Linearity	10		100K	10		100K	10		100K	Hz	6
Frequency Inputs Positive Excursion	Voltage Required to Turn Comparator On	0.4		V_{DD}	0.4		V_{DD}	0.4		V_{DD}	V	7
Negative Excursion	Voltage Required to Turn Comparator Off	-0.4		-2V	-0.4		-2V	-0.4		-2V	V	7
Min. Positive Pulse Width	Time between Threshold Crossings		5.0			5.0			5.0		μs	7
Min. Negative Pulse Width	Time between Threshold Crossings		0.5			0.5			0.5		μs	7
Input Impedance		10			10			10			MΩ	
Analog Outputs Output Voltage	Voltage Range of Op Amp Output for Specified Non-Linearity		V_{DD}-1			V_{DD}-1			V_{DD}-1		V	8
Output Loading	Resistive Loading at Output of Op Amp	2K			2K			2K			Ω	
Supply Current I_{DD} Quiescent (L Package) (J Package)	Current Required from Positive Supply During Operation		2.0 2.0	4.0 6.0		2.0 2.0	4.0 6.0		3.0	10.0	mA mA	9
I_{SS} Quiescent (L Package) (J Package)	Current Required from Negative Supply During Operation		-1.5 -1.5	-4.0 -6.0		-1.5 -1.5	-4.0 -6.0		-3.0	-10.0	mA mA	10
V_{DD} Supply	Operating Range of Positive Supply	4.0		7.5	4.0		7.5	4.0		7.5	V	
V_{SS} Supply	Operating Range of Negative Supply	-4.0		-7.5	-4.0		-7.5	-4.0		-7.5	V	
Reference Voltage V_{REF}—V_{SS}	Range of Voltage Reference Input	-1.0			-1.0			-1.0			V	

NOTES:
1. Full temperature range.
2. I_{IN} = 0.
3. Full temperature range, I_{OUT} = 10mA.
4. I_{OUT} = 10μA.
5. 10Hz to 100KHz.
6. 5μs min. positive pulse width and 0.5μs min. negative pulse width.
7. $T_r = t_f$ = 20ns.
8. $R_L \geq 2K\Omega$.
9. Full temperature range, V_{IN} = -0.1V.
10. V_{IN} = -0.1V.
11. I_{IN} connects the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors.

F/V Circuit Description

The 9400, when used as a frequency to voltage converter, generates an output voltage which is linearly proportional to the input frequency waveform.

Each zero crossing at the comparator's input causes a precise amount of charge ($q = C_{REF} \times V_{REF}$) to be dispensed into the op amp's summing junction. This charge in turn flows through the feedback resistor generating voltage pulses at the output of the op amp. A capacitor (C_{INT}) across R_{INT} averages these pulses into a DC voltage which is linearly proportional to the input frequency.

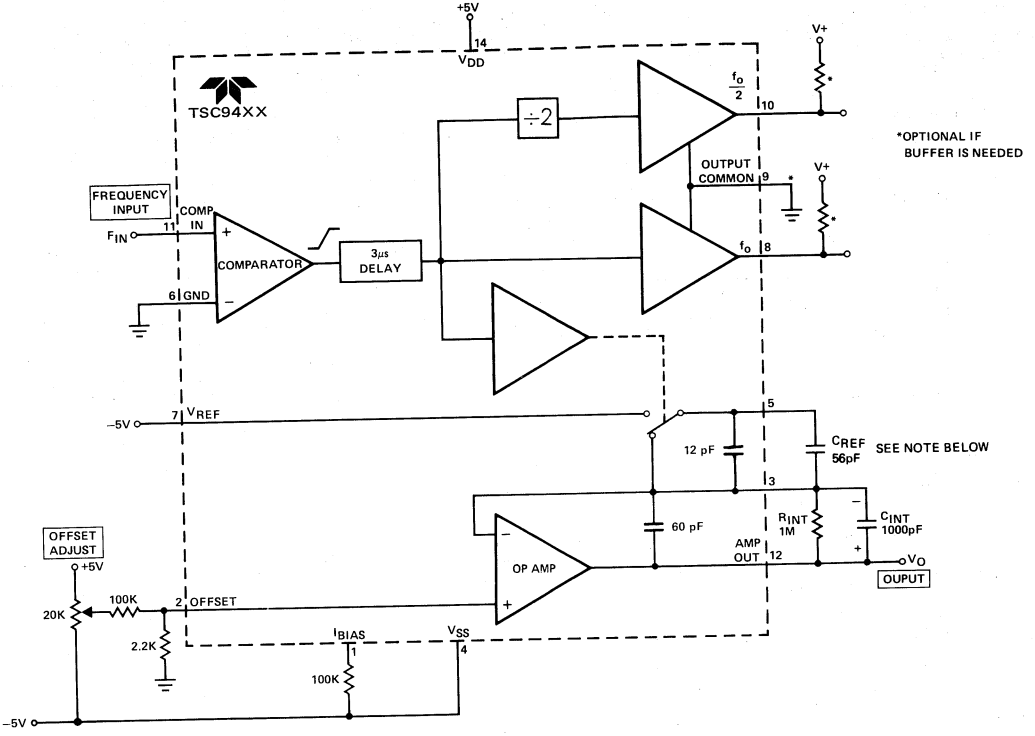


Figure 7. DC — 10KHz F/V Converter

F/V Design Information

Input/Output Relationships — The output voltage is related to the input frequency (F_{IN}) by the transfer equation:

$$V_{OUT} = \left[V_{REF}\, C_{REF}\, R_{INT}\right] F_{IN}$$

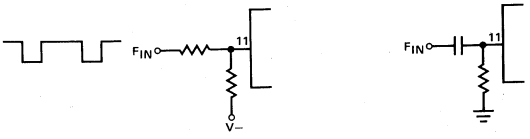
The response time to a change in F_{IN} is equal to $(R_{INT}\, C_{INT})$. The amount of ripple on V_{OUT} is inversely proportional to C_{INT} and the Input Frequency.

C_{INT} can be increased to lower the ripple. 1μF to 100μF are perfectly acceptable values for low frequencies.

When 9400 is used in the single supply mode, V_{REF} is defined as the voltage difference between Pin 7 and Pin 2.

Input Voltage Levels — The input signal must cross through zero in order to trip the comparator. In order to overcome the hysteresis the amplitude must be greater than ±200mV.

If only a unipolar input signal (F_{IN}) is available, it is recommended that either an offset circuit using resistor be used or that the signal be coupled in via a capacitor.



Note: C_{REF} should be increased for lower F_{IN} max. Adjust C_{REF} so that V_O is approximately 2.5 to 3.0 volts for the maximum input frequency. When F_{IN} max is less than 1 kHz, the duty cycle should be greater than 20% to insure that C_{REF} is fully charged and discharged.

F/V Design Information (Contd.)

For 100KHz maximum input R_{INT} should be decreased to 100KΩ.

Input Buffer – f_o and $f_o/2$ are not used in the F/V mode. However, these outputs may be useful for some applications, such as a buffer to feed additional circuitry. f_o will then follow the input frequency waveform; except that f_o will go high 3μs after F_{IN} goes high. $f_o/2$ will be square wave with a frequency of one half f_o.

If these outputs are not used, then Pins 8, 9 and 10 may be left floating or connected to ground.

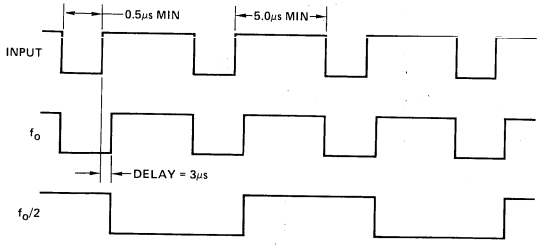
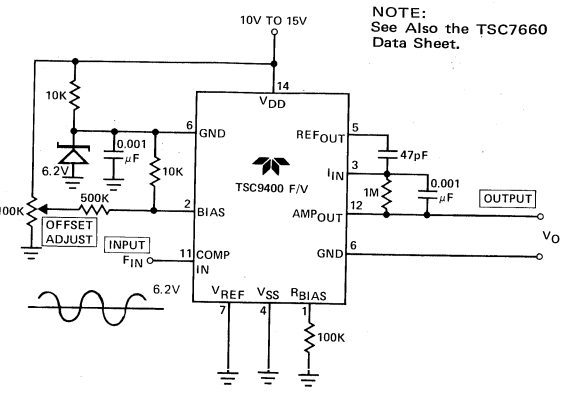


Figure 8. F/V Digital Outputs

The sawtooth ripple which is on the output of an F/V can be eliminated without affecting the F/V's response time by using the circuit in Figure 10. The circuit has a DC gain of +1. Any AC components such as a ripple are amplified both positively, via the lower path, and negatively, via the upper path. When both paths have the same gain, the AC ripple is cancelled. The amount of cancellation is directly proportional to gain matching. If the two paths are matched within 10%, then the ripple will be lowered by 1/10. For 1% matching, the ripple is lowered by 1/100. The 10K potentiometer is used to make the gain equal in both paths. This circuit is insensitive to both frequency changes and to signal wave shape.



1. The input is now referenced to 6.2 V (Pin 6). The input signal must therefore be restricted to be greater than 4 volts (Pin 6 –2V) and less than 10 to 15V (V_{DD}).

If the signal is AC coupled then a resistor (100K to 10MΩ) must be placed between the input (Pin 11) and Pin 6.

2. The output will now be referenced to Pin 6 which is at 6.2 V(V_Z). For frequency meter applications a 1mA meter with a series scaling resistor can be placed across Pins 6 and 12.

Figure 9. F/V Single Supply

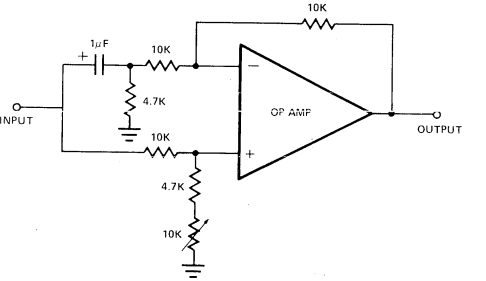
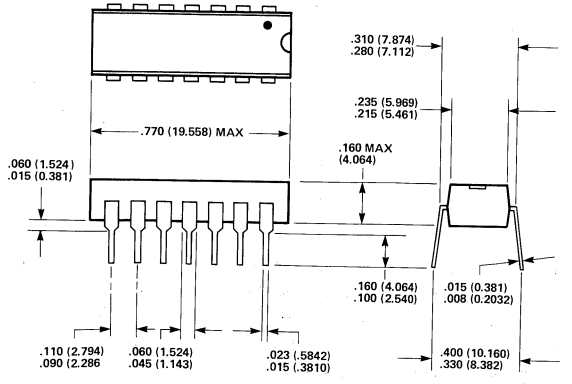


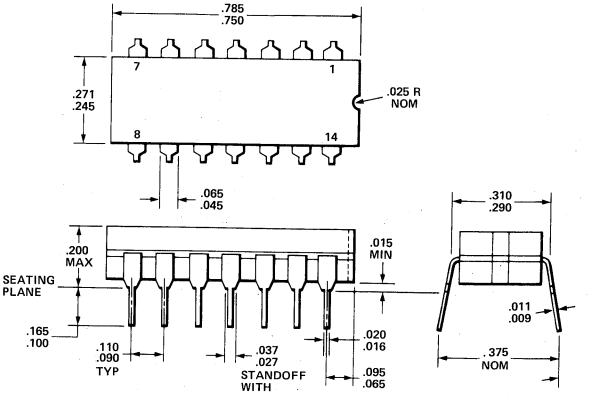
Figure 10. F/V Ripple Eliminator

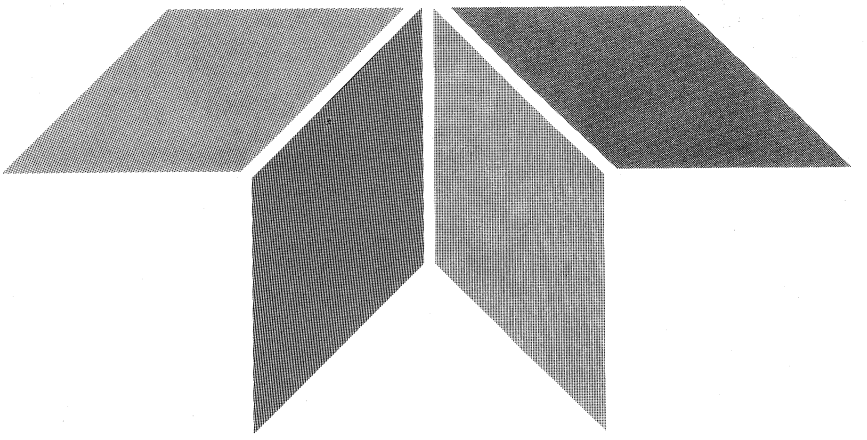
Package Information

(Package #6)
14-Pin Plastic Dip (J Package)



(Package #7)
14-Pin CerDIP (L Package)





SECTION 10

Display Drivers

Section 10
Display Drivers 10-1

TSC700A	High Current Four Digit LED Driver	10-3
TSC701AM	High Current Bus Compatible Four Digit LED Driver	10-11
TSC7211A	Four Digit LCD Driver	10-19
TSC7212A	Four Digit LED Driver	10-19
TSC7211AM	Bus Compatible Four Digit LCD Driver	10-31
TSC7212AM	Bus Compatible Four Digit LED Driver	10-31

TSC700A
Four Digit LED Display Decoder and Driver
High Segment Drive Current

General Description

The TSC700A drives common anode LED displays with 28 high current, open-drain N channel output transistors. Four seven segment LED displays may be driven. Drive current is guaranteed to be 11 mA minimum. This is twice the minimum drive current available from comparable devices and will provide high LED luminance. High luminous intensity is an important factor when a dark contrasting background is unavailable or the LED is viewed at a distance. The TSC700A current capability makes it an ideal large character LED driver.

Four data bit inputs and four digit select signals permit interfacing to multiplexed BCD or binary output devices. The four bit data input is decoded into the seven segment alphanumeric code known as "Code B". A 0 to 9, —, E, H, L, P or "blank" reading may be displayed.

An added feature includes a brightness control input that adjusts segment drive current. The control pin may also be used as a digital display enable. The TSC700A is an improved pin compatible and functional equivalent to the ICM7212A and TSC7212A.

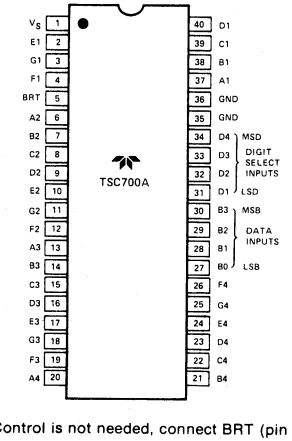
Ordering Information

Part No.	Package	Temp. Range	LED Segment Current	Output Code
TSC700AMJL	40 Pin CerDIP	-55°C to +125°C	14 mA	Code B
TSC700AIJL	40 Pin CerDIP	-25°C to +85°C	14 mA	Code B
TSC700 AMJL/883	40 Pin CerDIP	-55°C to +125°C	14 mA	Code B
TSC700A/Y	CHIP	25°C	14 mA	Code B

Features

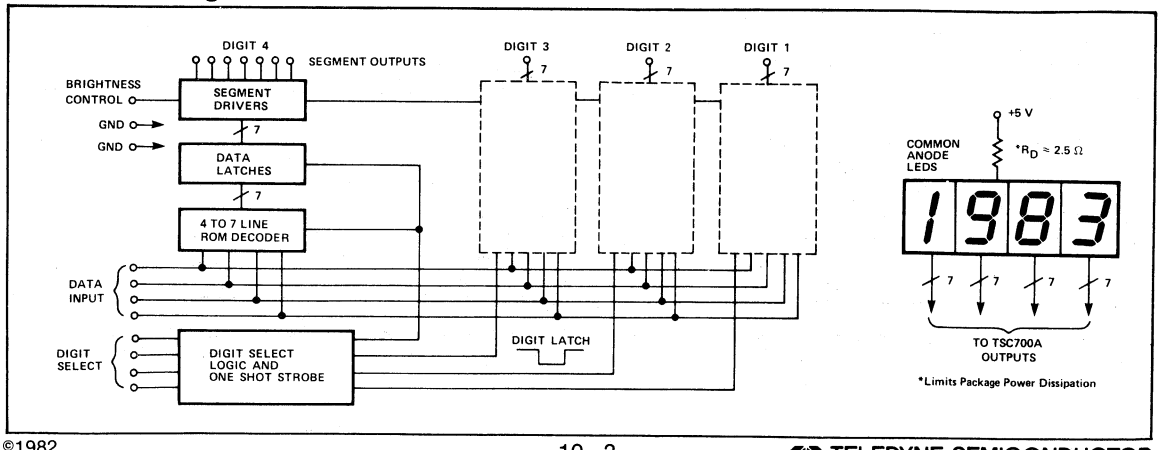
- High Drive Current for High Luminance LED Display
- Guaranteed High LED Segment Current 11 mA Minimum
- 28 Common Anode LED Drivers (4 Digits)
- Code B Output Format ... 0 to 9, —, E, H, L, P, "blank"
- BCD/Binary Input to Seven Segment LED Code
- Four Separate Digit Selects for Multiplexed Input
- Digital or Analog Brightness Control
- Digital Display Enable
- Low Thermal Resistance Package
- Military Temperature Range Devices Available
- Pin Compatible With TSC7212A, ICM7212A

Pin Configuration



If Brightness Control is not needed, connect BRT (pin 5) to Vs.

Functional Diagram



Absolute Maximum Ratings (Notes 1, 2)

Power Dissipation ..... *1.0 W
Supply Voltage ..... 6.5 V
Input Voltage (Any Terminal) V_S + 0.3 V to Ground -0.3 V
Operating Temperature
M Version ..... -55° C to +125° C
I Version ..... -25° C to +85° C

Maximum Chip Temperature ..... +150° C
Storage Temperature ..... -55° C to +150° C
Lead Temperature (10 Sec) ..... 300° C

* To 85° C, See Derating Curve on Page 4 for operation above 85° C.

Electrical Characteristics: Specifications measured with V_S = 5.0 V at T_A = 25° C.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC700A MIN	TYP	MAX	UNIT
LED DRIVER	1	I_{SEG}	Segment ON Current	Test Circuit	11	14	18	mA
	2	I_{SLK}	Segment Leakage		—	±0.01	±1.0	μA
INPUT	3	V_{IH}	Logic "1" Input Voltage		3.0	—	—	V
	4	V_{IL}	Logic "0" Input Voltage		—	—	1.0	V
	5	I_{IN}	Input Current	Pins 27-34	—	±0.01	±1.0	μA
	6	C_{IN}	Digital Input Capacitance	Pins 27-34	—	5	—	pF
	7	C_{BR}	Brightness Input Capacitance		—	200	—	pF
TIMING	8	t_{pw}	Digit Select Pulse Width	See Timing Diagram	1.0	—	—	μs
	9	t_{DS}	Data Setup Time	See Timing Diagram	—	—	100	ns
	10	t_{DH}	Data Hold Time	See Timing Diagram	—	0	—	ns
	11	t_{IDS}	Inter-Digit Select Time	See Timing Diagram	2.0	—	—	μs
POWER	12	V_S	Operating Supply Voltage Range		4	5	6	V
	13	I_S	Supply Current	Display OFF	—	—	50	μA
	14	I_{op}	Operating Current	Pin 5, 27-34 at GND, Display all "8's"	—	440	—	mA

Notes:
1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static Sensitive device. Unused devices must be stored in conductive material to protect devices from static discharge and static fields.

Output Pin Description and Function

OUTPUT	TERMINAL		FUNCTION	OUTPUT	TERMINAL		FUNCTION
A1	37	A	Segment Dr. Digit 1 (LSD)	A3	13	A	Segment Dr. Digit 3
B1	38	B		B3	14	B	
C1	39	C		C3	15	C	
D1	40	D		D3	16	D	
E1	2	E		E3	17	E	
F1	4	F		F3	19	F	
G1	3	G		G3	18	G	
A2	6	A	Segment Dr. Digit 2	A4	20	A	Segment Dr. Digit 4 (MSD)
B2	7	B		B4	21	B	
C2	8	C		C4	22	C	
D2	9	D		D4	23	D	
E2	10	E		E4	24	E	
F2	12	F		F4	26	F	
G2	11	G		G4	25	G	

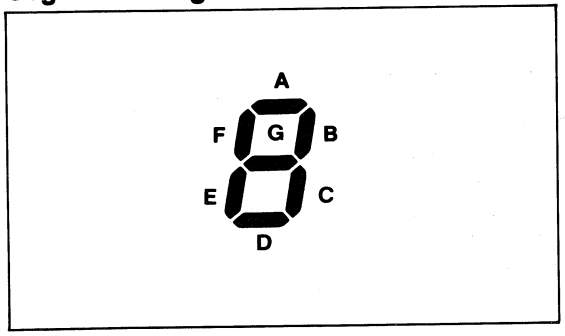
Input Pin Description and Function

INPUT	TERMINAL	FUNCTION
B0	27	Ones (Least Significant)
B1	28	Twos
B2	29	Fours
B3	30	Eights (Most Significant)
D1	31	D1 (Least Significant) Digit Select
D2	32	D2 Digit Select
D3	33	D3 Digit Select
D4	34	D4 (Most Significant) Digit Select
BRT	5	Brightness Control: Logic 1 = ON Logic 0 = OFF See Typical Characteristic Curve for I_{SEG} Vs Brightness Control Voltage

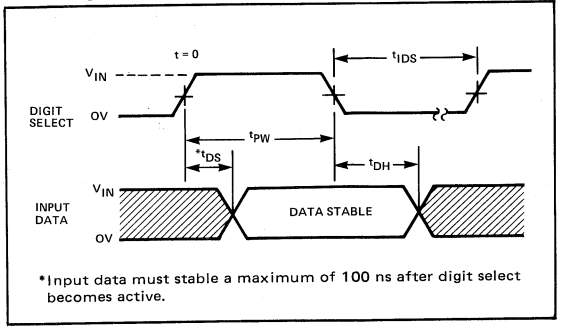
DATA INPUTS BITS

10

Segment Assignment



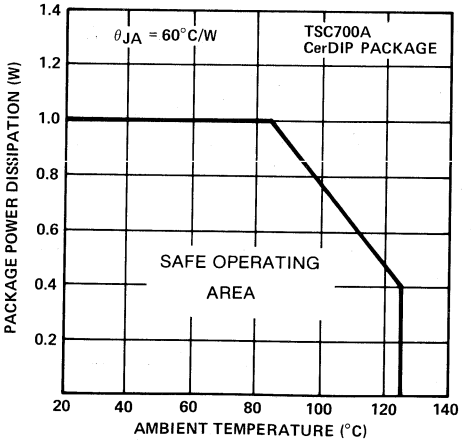
Timing Diagram



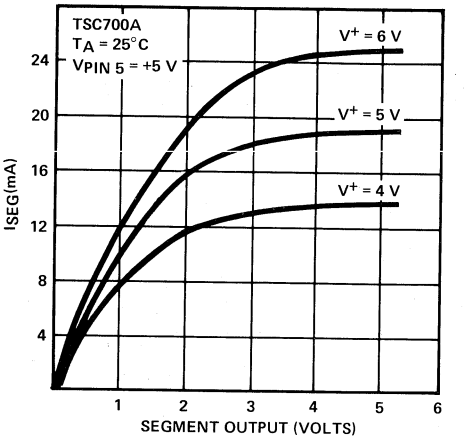
*Input data must stable a maximum of 100 ns after digit select becomes active.

Electrical Operating Characteristics

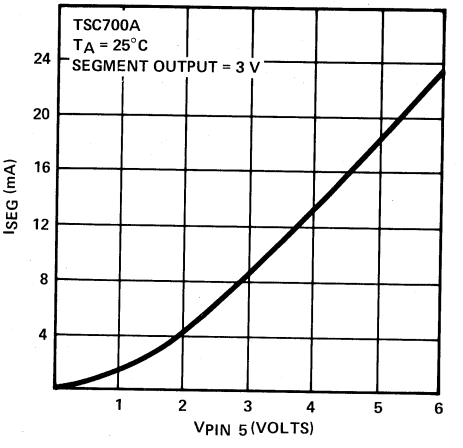
Maximum Power Dissipation



LED Segment Current vs Output Voltage



LED Segment Current vs Brightness Control Voltage



Operation Description

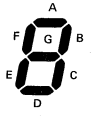
Output Format

The TSC700A accepts four bit binary information at pins 27 (LSB) through 30 (MSB). The binary input is decoded to the seven segment output in a format known as "Code B". The display format is 0 to 9, —, E, H, L, P and "blank".

Output Code

BINARY INPUT				TSC700A Output "Code B"
B3	B2	B1	B0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	-
1	0	1	1	E
1	1	0	0	H
1	1	0	1	L
1	1	1	0	P
1	1	1	1	(Blank)

Segment Assignment



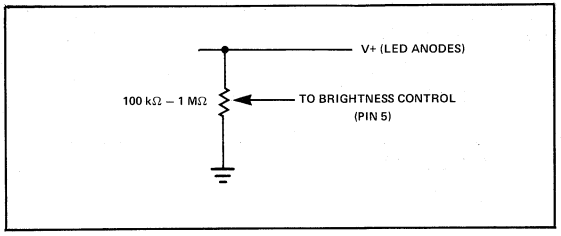
Special Order Output Format

The TSC700A is mask programmed to give 16 combinations of seven segment output codes. For large volume orders (50 K minimum pieces) custom decoder options are available. Contact factory for details.

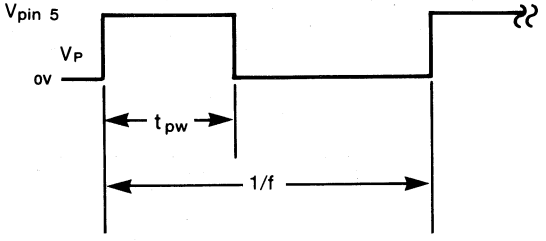
Brightness Control Operation

The voltage at the brightness control input is transferred to the output transistor gate for "ON" segments. The brightness voltage directly modulates the segment driver "ON" resistance. A brightness input (pin 5) can be used in two ways to control output transistor drain current. A variable brightness control may be implemented with a single potentiometer. A high value potentiometer (100 KΩ to 1 MΩ) will minimize power consumption.

Brightness Control



A logic signal of varying duty cycle will also control display brightness.



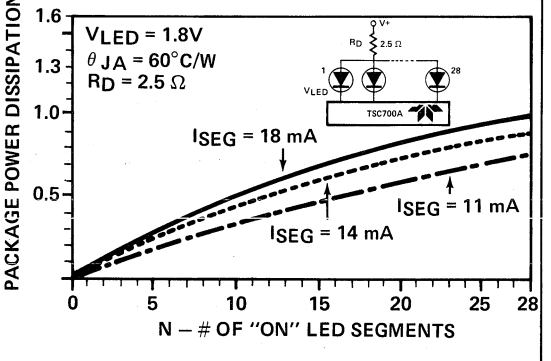
$$V_{pin\ 5} = \left(\frac{1}{(1/f)}\right) \int_{o}^{(1/f)} (V_{pin\ 5})\, dt = f\, V_p\, t_{pw} = V_p\ [\text{Duty Cycle}]$$

The display may be blanked (all segments OFF) by applying the input code 1111 or by driving the brightness pin with a logic 0. If brightness control is not needed, pin 5 should be tied to 5.0 V.

10

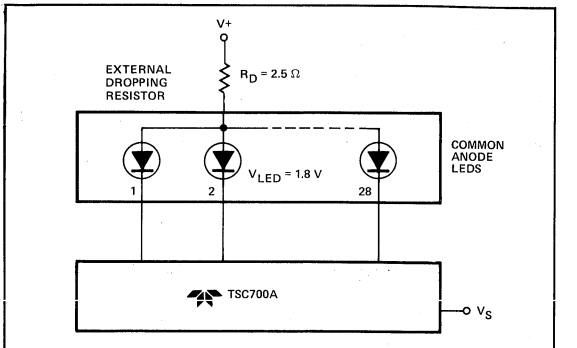
Package Power Dissipation Minimization

The TSC700A high LED current drive capability requires package power dissipation be limited and that a low thermal resistance package be used. The cerDIP package thermal resistance (θjc = 30° C/W, θja = 60° C/W) permits operation over the full −25° C to +85° C industrial operating temperature range. Power dissipation is easily controlled by reducing the applied voltage at the segment driver outputs. A 2.5 Ω voltage dropping resistor placed in series with the common anode LED display voltage will maintain dissipation under 1 watt with a worst case continuous 8888 display. Figure 1 gives the package power dissipation vs the number of "ON" LED segments for the operating circuit in Figure 2. Driver outputs should be maintained above 1.85 V for constant current operation.



Character Displayed	No of "ON" Segments
0	6
1	2
2	5
3	5
4	4
5	5
6	6
7	3
8	7
9	6
—	1
E	5
H	5
L	3
P	5

Figure 1: Package Power Dissipation



$$P_D = V_S I_S + I_{SEG}(N)\,[V^+ - V_{LED} - N(I_{SEG})\,R_D]$$

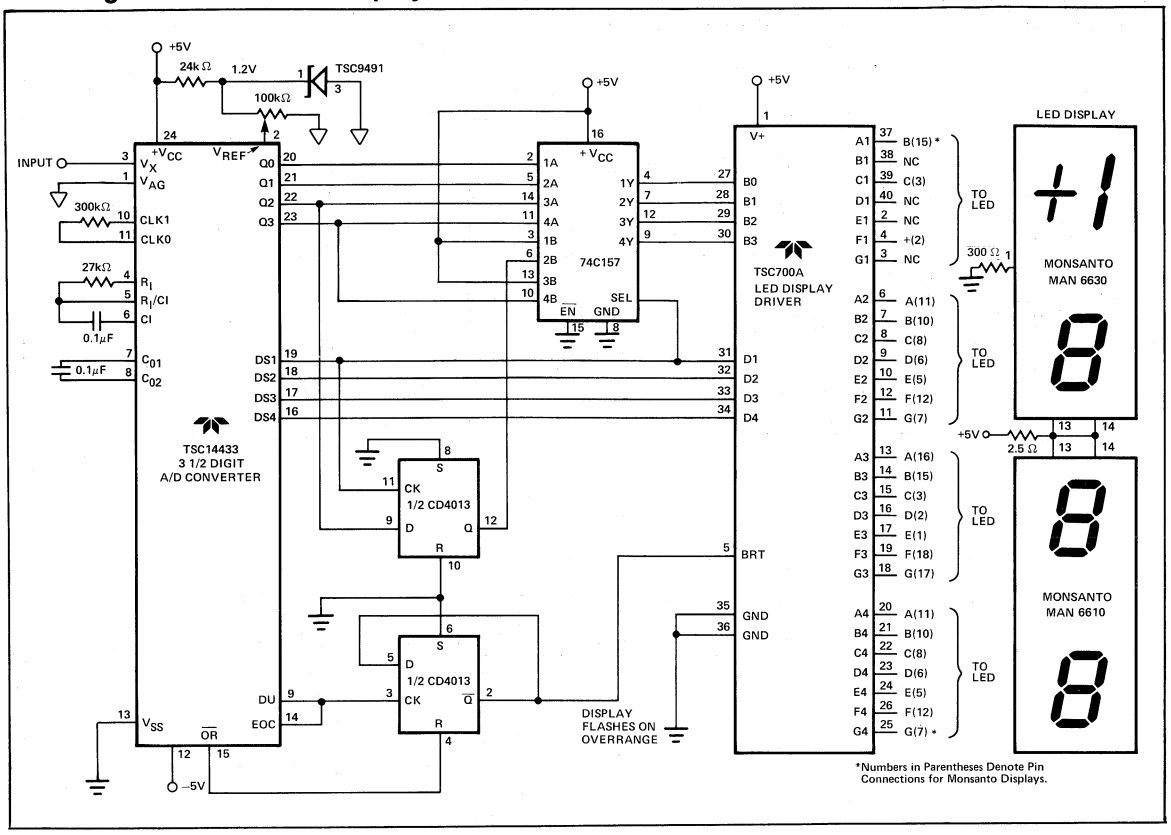
$$\approx I_{SEG}(N)\,[V^+ - V_{LED} - N(I_{SEG})\,R_D]$$

Where:
I_{SEG} = LED Segment Current
N = Number of ON Segments
V_{LED} = Voltage Across on LED
P_D = Max. Package Power Dissipation
V_S = TSC700A Power Supply Voltage (5 V)
I_S = TSC700A Quiescent Current (≈ 50 μA)

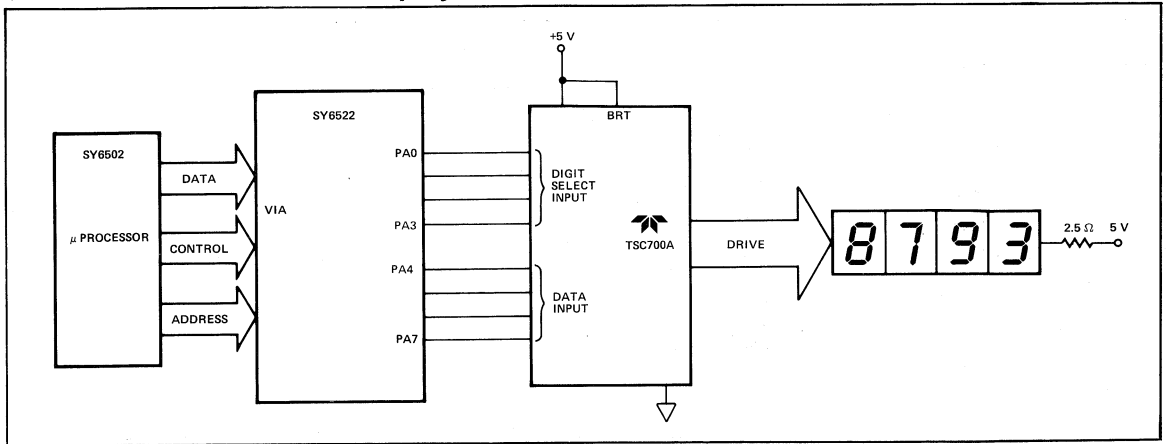
Figure 2: Operating Circuit

Applications Information:

3 1/2 Digit ADC with LED Display

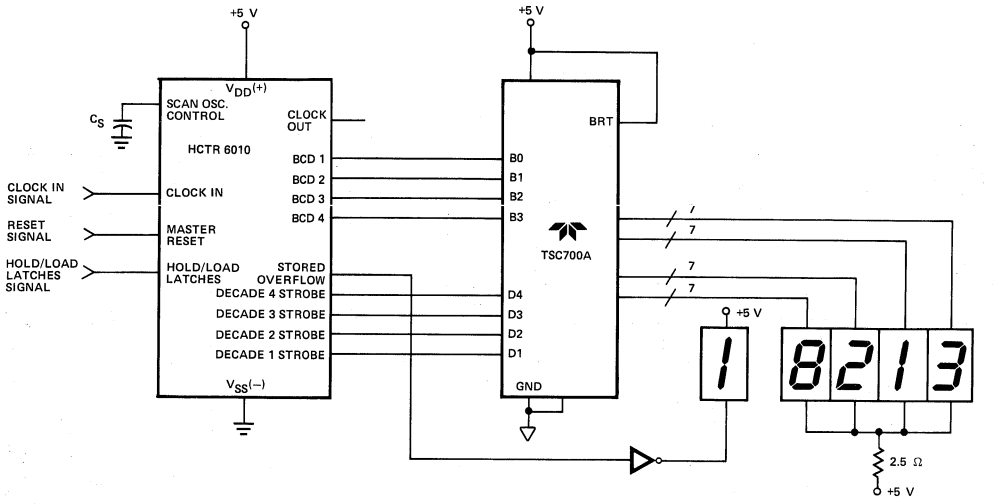


μ - Processor Controlled Display



Applications Information (continued)

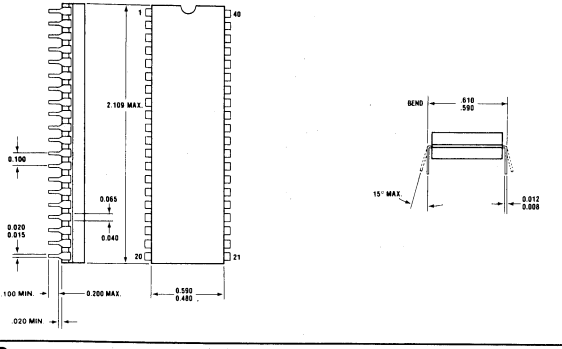
4 1/2 Digit Counter



INPUTS			INTERNAL	BCD & STORED OVERFLOW
MASTER RET	CLOCK IN	HOLD/LOAD LATCHES	COUNTER RESPONSE	OUTPUT RESPONSE
0	↓	0	Advances 1 Count	Indicates New Count
0	↑	0	No Change	No Change
0	↓	1	Advances 1 Count	Retains Prior Count
1	x	0	Resets entire Counter	Outputs go to Zero
1	x	1	Resets entire Counter	Retains Prior Count

Package Information

40-Pin CerDIP
J Package
(Package #20)



TELEDYNE SEMICONDUCTOR

TSC701AM
Bus Compatible Four Digit LED Display Driver
• High Segment Drive Current
• Input Data Latches

General Description

The TSC701AM is a CMOS direct drive, four digit, seven segment LED display decoder and driver. The device is bus compatible making microprocessor controlled displays possible. Two chip select signals control data and digit select code latching prior to decoding and display. External data latches are unnecessary.

The TSC701AM drives common anode LED displays with 28 high current, open-drain N channel output transistors. Four seven segment LED displays may be driven. Drive current is guaranteed to be 11 mA minimum (18 mA TYP). This is twice the minimum drive current available from comparable devices and will provide high LED luminance. High luminous intensity is an important factor when a dark contrasting background is unavailable or the LED is viewed at a distance. The TSC701AM current capability makes it an ideal large character LED driver.

Four data bit inputs and four digit select signals permit interfacing to multiplexed BCD or binary output devices. The four bit data input is decoded into the seven segment alphanumeric code known as "Code B". A 0 to 9, —, E, H, L, P or "blank" reading may be displayed.

An added feature is the brightness control input that adjusts segment drive current. The control pin may also be used as a digital display enable. The TSC701AM is an improved pin compatible and functional equivalent to the ICM7212AM.

Features

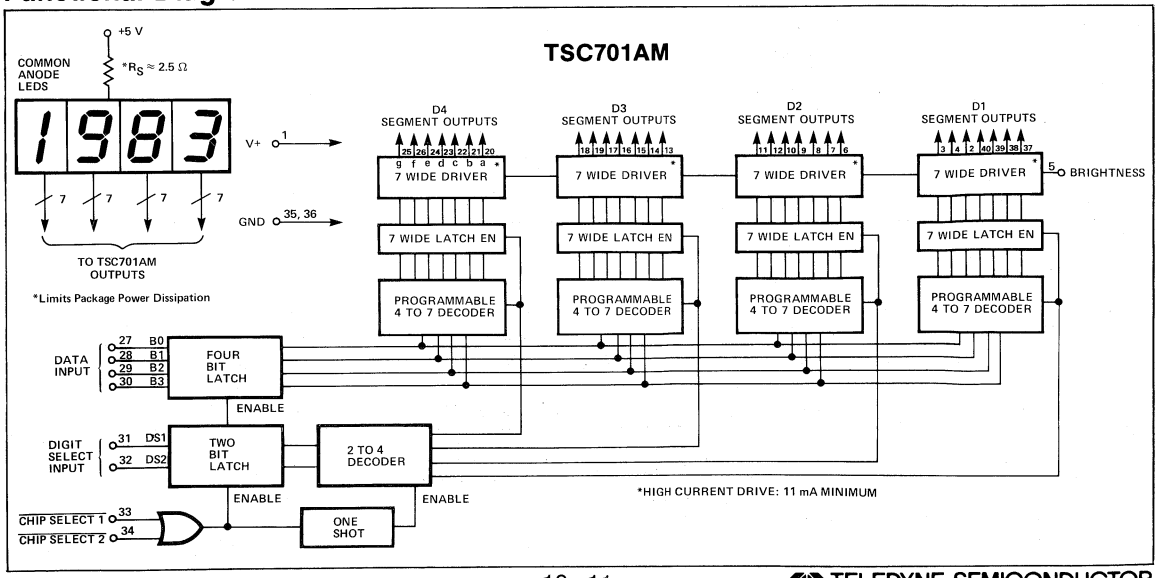
- 28 Current Limited Outputs Drive Common-Anode LEDs at 18 mA Per Segment.
- Input and Digit Select Data Latches.
- Brightness Input Allows Potentiometer Control of LED Segment Current. Pin Also Serves as Digital Display Enable.
- Input and Digit Select Data Latches.
- Pin Compatible and Functionally Equivalent to ICM7212AM.
- Input Decoded to Seven Segment Code B Output (0 to 9, —, E, H, L, P, "Blank")

Ordering Information

Part No.	Package	Temp. Range	LED Segment Current	Output Code
TSC701AMIJL	40-Pin CerDIP	-25° C to +85° C	18 mA	Code B

10

Functional Diagram



Absolute Maximum Ratings

Power Dissipation ..... 1.0 W
Supply Voltage ..... 6.5 V
Input Voltage (Any Terminal) V_S + 0.3 V to Ground -0.3 V
Operating Temperature
I Version ..... -25° C to +85° C
Maximum Chip Temperature ..... +150° C
Storage Temperature ..... -55° C to +150° C
Lead Temperature (10 Sec) ..... 300° C

Electrical Characteristics: Specifications measured with V_S = 5.0 V at T_A = 25° C.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC701AM MIN	TYP	MAX	UNIT
LED DRIVER	1	I_{SEG}	Segment ON Current	Test Circuit	11	18	20	mA
	2	I_{SLK}	Segment Leakage		—	±0.01	±1.0	μA
INPUT	3	V_{IH}	Logic "1" Input Voltage		3.0	—	—	V
	4	V_{IL}	Logic "0" Input Voltage		—	—	1.0	V
	5	I_{IN}	Input Current	Pins 27-34, 5	—	±0.01	±1.0	μA
	6	C_{IN}	Digital Input Capacitance	Pins 27-34	—	5	—	pF
	7	C_{BR}	Brightness Input Capacitance		—	200	—	pF
TIMING	8	t_{CSA}	Chip Select Active Pulse Width	Note 3	200	—	—	ns
	9	t_{DS}	Data Setup Time		100	—	—	ns
	10	t_{DH}	Data Hold Time		10	0	—	ns
	11	t_{ICS}	Inter-Chip Select Time		2	—	—	μs
POWER	12	V_S	Operating Supply Voltage Range		4	5	6	V
	13	I_S	Supply Current	Display OFF	—	—	50	μA
	14	I_{op}	Operating Current	Pin 5, at V_S^+ Display all "8's"	—	504	—	mA

Notes:

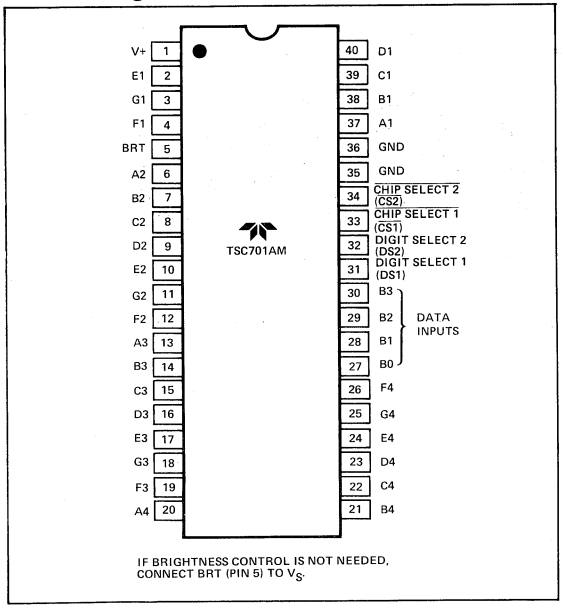
1. Functional operation above the absolute maximum stress ratings is not implied.
2. Static Sensitive device. Unused devices must be stored in conductive material to protect devices from static discharge and static fields.
3. Other chip select ($\overline{CS}$) is either held at logic zero or both $\overline{CS1}$ and $\overline{CS2}$ driven together.

Input Definitions

In this table, V + and GROUND are considered to be normal operating input logic levels. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL	CONDITION	FUNCTION	
B0	27	V + Logical One GND = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28	V+ = Logical One GND = Logical Zero	Twos	
B2	29	V+ = Logical One GND = Logical Zero	Fours	
B3	30	V+ = Logical One GND = Logical Zero	Eights (Most Significant)	
DS1	31	V+ = Logical One	Digit Select Inputs DS2, DS1 = 00 Selects D4 DS2, DS1 = 01 Selects D3 DS2, DS1 = 10 Selects D2 DS2, DS1 = 11 Selects D1	
DS2	32	GND = Logical Zero		
$\overline{CS1}$	33	V+ = Inactive	When both $\overline{CS1}$ and $\overline{CS2}$ are low the data and digit select input latches are open or enabled. On the rising of $\overline{CS1}$ or $\overline{CS2}$ data is latched, decoded and stored in the output drive latches.	
$\overline{CS2}$	34	GND = Active		

Pin Configuration



Timing Diagram

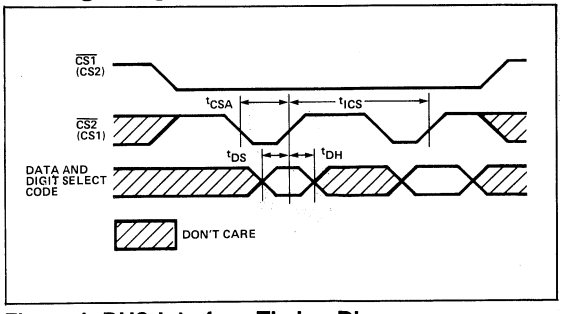


Figure 1: BUS Interface Timing Diagram

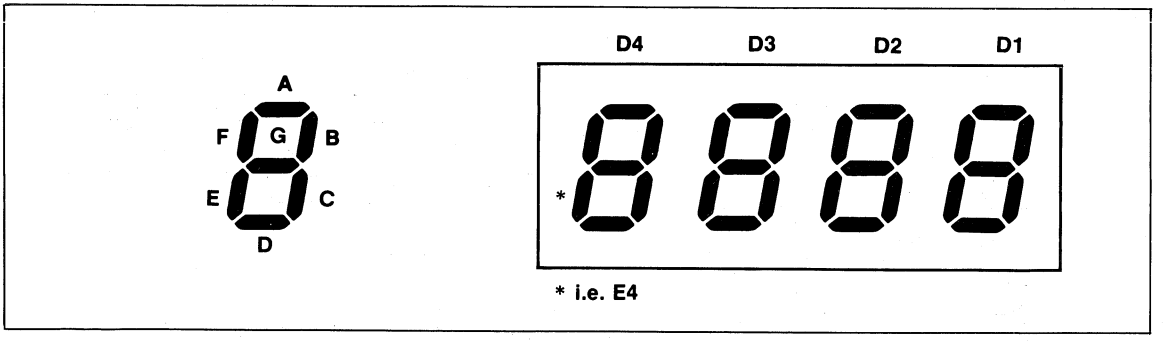
10

Output Definitions

Output pins are defined by the alphabetical segment assignment and numerical digital assignment.

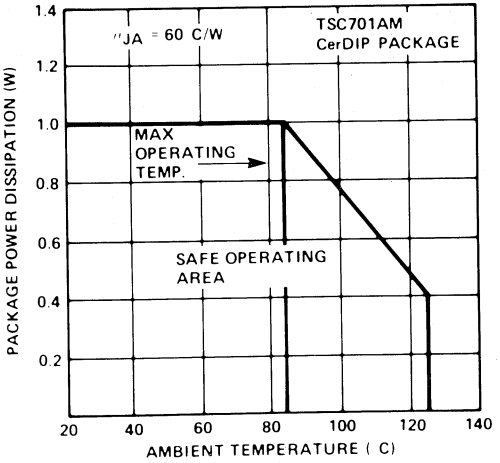
OUTPUT	TERMINAL	FUNCTION	OUTPUT	TERMINAL	FUNCTION
A1	37	A Segment Dr. Digit 1 (LSD)	A3	13	A Segment Dr. Digit 3
B1	38	B	B3	14	B
C1	39	C	C3	15	C
D1	40	D	D3	16	D
E1	2	E	E3	17	E
F1	4	F	F3	19	F
G1	3	G	G3	18	G
A2	6	A Segment Dr. Digit 2	A4	20	A Segment Dr. Digit 4 (MSD)
B2	7	B	B4	21	B
C2	8	C	C4	22	C
D2	9	D	D4	23	D
E2	10	E	E4	24	E
F2	12	F	F4	26	F
G2	11	G	G4	25	G

Digit Assignment

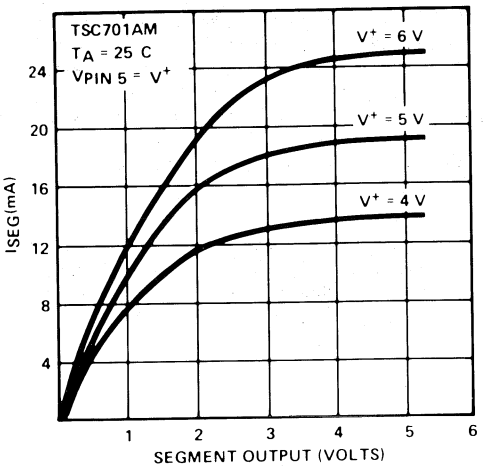


Electrical Operating Characteristics

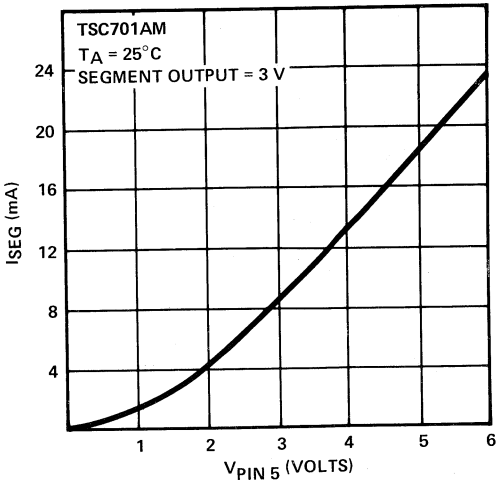
Maximum Power Dissipation



LED Segment Current vs Output Voltage



LED Segment Current vs Brightness Control Voltage



Input Configuration and Output Codes

The TSC701AM accepts a four bit, true binary (positive level = logic 1) input at pins 27 (LSB) through 30 (MSB). The output display format is 0 to 9, —, E, H, L, P and blank (see Table 1). The TSC701AM correctly decodes binary and BCD true codes to a seven segment output.

The TSC701AM is designed to interface with a data bus and display data under microprocessor control. Four data input bits (Pins 27-30) and two digit select input bits (Pins 31, 32) are written into input buffer latches. The rising edge of either chip select causes data to be latched, decoded and stored in the selected digit output data latch. The two bit digit code selects the appropriate output digit latch. The four bit display data word is decoded to the "Code B" seven segment output format.

For applications where bus compatibility is not required refer to the TSC7211A (LCD), TSC7212A (LED) and the TSC700A (LED) four digit decoder driver data sheets. These devices are designed to accept multiplexed BCD/Binary input data for display under the control of four separate digit select control signals.

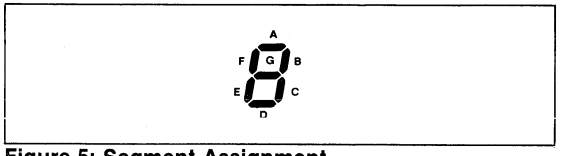


Figure 5: Segment Assignment

BINARY INPUT				CODE B TSC701AM
B3	B2	B1	B0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	—
1	0	1	1	E
1	1	0	0	H
1	1	0	1	L
1	1	1	0	P
1	1	1	1	(Blank)

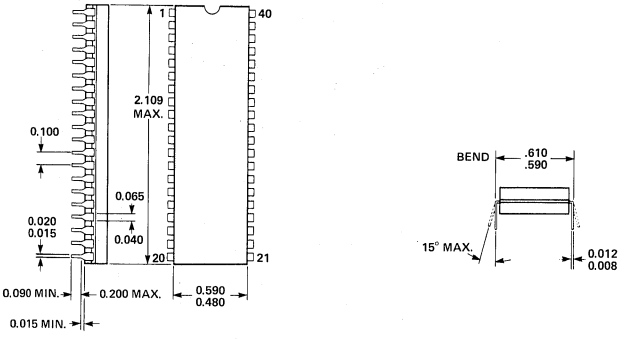
Table 1: Output Code

Applications Information

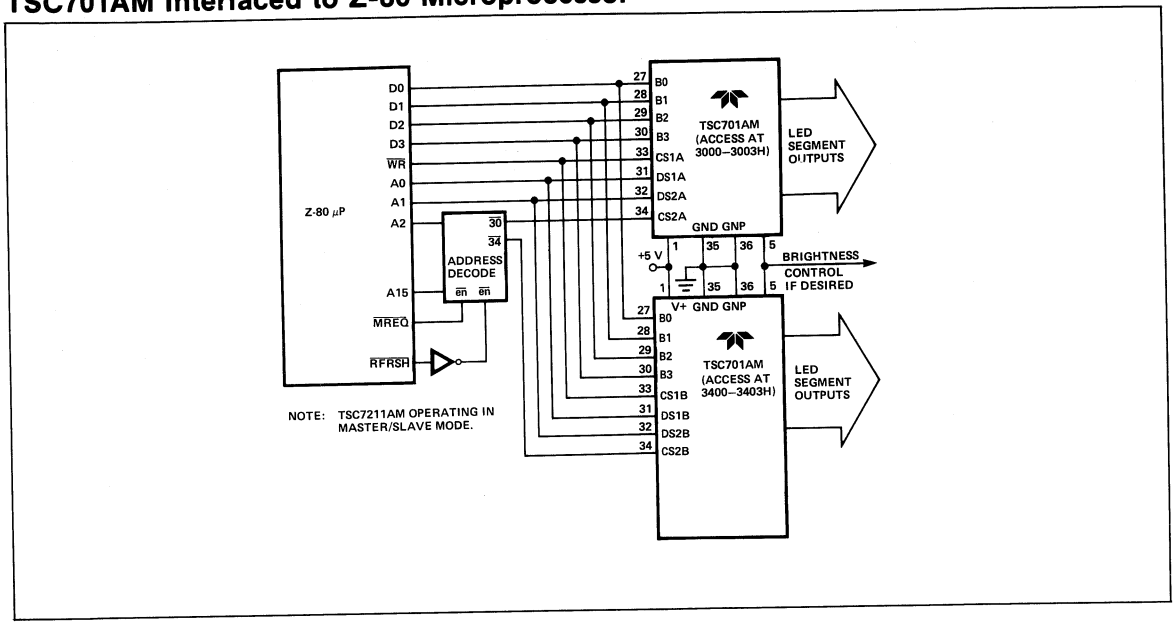
The TSC701AM has two ground pins. These pins should be connected together.

Package Information

40-Pin CerDIP
(Package #20)



TSC701AM Interfaced to Z-80 Microprocessor



10

TSC7211A (LCD)
TSC7212A (LED)
Four Digit CMOS Display Decoder and Driver

General Description

The TSC7211A (LCD Decoder/Driver) and TSC7212A (LED Decoder/Driver) are direct drive, four digit, seven segment display decoder and drivers.

The TSC7211A drives conventional LCD displays. An RC oscillator, divider chain, backplane driver, and 28 segment outputs are provided on a single CMOS chip. The segment drivers supply square waves of the same frequency as the backplane but in phase for an OFF segment and out of phase for an ON segment. The net d.c. voltage applied between driver segment and backplane is zero.

The TSC7212A drives common anode LED displays with 28 current controlled, low leakage, open drain, N-Channel output transistors. The brightness control input can be used as a digital display enable. A varying voltage at the control input will allow continuous display brightness control.

The TSC7211A (LCD) and TSC7212A (LED) require only four data bit inputs and four digit select signals to interface with multiplexed BCD or binary output devices such as the ICM7217, ICM7226, ICL7103 and TSC7135. The four bit binary input code is decoded into the seven segment alphanumeric code known as "Code B."

The "Code B" output format results in a 0 to 9, —, E, H, L, P or blank display. True BCD or binary inputs will be correctly decoded to the seven segment display format.

The CMOS TSC7211A and TSC7212A are available in a 40-pin epoxy dual-in-line package and a compact 60-pin flat package. All inputs are protected against static discharge.

TSC7211A Features (LCD Driver)

- Four Digit Non-Multiplexed Seven Segment LCD Display Outputs With Backplane Driver.
- RC Oscillator On Chip Generated Backplane Drive Signal.
- Eliminates DC Bias Which Degrade LCD Display Life.
- Backplane Input/Output Pin Permits Synchronization of Cascaded Slave Device to a Master Backplane Signal.
- Separate Digit Select Inputs to Accept Multiplexed BCD/Binary Inputs.
- Binary and BCD Inputs Decoded to Code B (0 to 9, —, E, H, L, P, Blank).
- Pin Compatible and Functionally Equivalent to ICM7211A and DF411.
- Connect to TSC7135 in Flat Package For Compact 4 1/2 Digit Meter Systems

TSC7212A Features (LED Driver)

- 28 Current Limited Outputs Drive Common Anode LEDs at Greater Than 5 mA Per Segment.
- Brightness Input Allows Potentiometer Control of LED Segment Current. Pin Also Serves as Digital Display Enable.
- Same Input Configuration and Output Decoding as the TSC7211A.
- Pin Compatible and Functionally Equivalent to ICM7212A.

10

Ordering Information

Part No.	Driver Type	Package	Output Code	Input Config.
TSC7211AIPL	LCD	40-Pin Epoxy Dip	Code B	Multiplexed 4-Bit Binary or BCD
TSC7212AIPL	LED	40-Pin Epoxy Dip	Code B	Multiplexed 4-Bit Binary or BCD
TSC7211A/Y	LCD	DICE	Code B	Multiplexed 4-Bit Binary or BCD
TSC7212A/Y	LED	DICE	Code B	Multiplexed 4-Bit Binary or BCD
TSC7211AIJL	LCD	40-Pin CerDIP	Code B	Multiplexed 4-Bit Binary or BCD
TSC7212AIJL	LED	40-Pin CerDIP	Code B	Multiplexed 4-Bit Binary or BCD
TSC7211AIBQ	LCD	60-Pin Flat Package Formed Leads	Code B	Multiplexed 4-Bit Binary or BCD
TSC7211AISQ	LCD	60-Pin Flat Package Unformed Leads	Code B	Multiplexed 4-Bit Binary or BCD
TSC7212AIBQ	LED	60-Pin Flat Package Formed Leads	Code B	Multiplexed 4-Bit Binary or BCD
TSC7212AISQ	LED	60-Pin Flat Package Unformed Leads	Code B	Multiplexed 4-Bit Binary or BCD

Absolute Maximum Ratings

Power Dissipation (Note 1) ..... 0.8 W at 70°C
Supply Voltage ..... 6.5 V
Input Voltage (Any
Terminal) (Note 2) ..... V^+ +0.3 V, GROUND -0.3 V
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... -55°C to +125°C
Lead Temperature (Soldering 10 sec.) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This limit refers to that of the package and will not be realized during normal operation.

Note 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive device latchup. For this reason it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the TSC7211A/TSC7212A be turned on first.

Table I: Operating Characteristics

Test Conditions: All parameters measured with V^+ = 5 V

TSC7211A CHARACTERISTICS (LCD DECODER/DRIVER)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range	V_{SUPP}		3	5	6	V
Operating Current	I_{OP}	Test Circuit, Display Blank	—	10	50	μA
Oscillator Input Current	I_{OSCI}	Pin 36	—	± 2	± 10	μA
Segment Rise/Fall Time	t_{rfs}	C_L = 200 pF	—	0.5	—	μA
Backplane Rise/Fall Time	t_{rfb}	C_L = 5000 pF	—	1.5	—	μs
Oscillator Frequency	f_{OSC}	Pin 36 Floating	—	16	—	kHz
Backplane Frequency	f_{bp}	Pin 36 Floating	—	125	—	Hz

TSC7212A CHARACTERISTICS (COMMON ANODE LED DECODER/DRIVER)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_{SUPP}		4	5	6	V
Operating Current Display Off	I_{OP}	Pin 5 (Brightness), Pins 27-34 — GROUND	—	10	50	μA
Operating Current	I_{OP}	Pin 5 at V+, Display all 8's	—	200	—	mA
Segment Leakage Current	I_{SLK}	Segment Off	—	± 0.01	± 1	μA
Segment On Current	I_{SEG}	Segment On, V_O = +3 V	5	8	—	mA

INPUT CHARACTERISTICS (LCD AND LED DECODER/DRIVER)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Logical "1" Input Voltage	V_{IH}		3	—	—	V
Logical "0" Input Voltage	V_{IL}		—	—	1	V
Input Leakage Current	I_{ILK}	Pins 27-34	—	± 0.01	± 1	μA
Input Capacitance	C_{IN}	Pins 27-34	—	5	—	pF
BP/Brightness Input Leakage	I_{BPLK}	Measured at Pin 5 with Pin 36 at GND	—	± 0.01	± 1	μA
BP/Brightness Input Capacitance	C_{BPI}	All Devices	—	200	—	pF

AC CHARACTERISTICS (LCD AND LED DECODER/DRIVER)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Digit Select Active Pulse Width	t_{sa}	Refer to Timing Diagrams	1	—	—	μs
Data Valid Time	t_{ds}	Refer to Timing Diagrams	—	—	100	ns
Data Hold Time	t_{dh}	Refer to Timing Diagrams	200	—	—	ns
Inter-Digit Select Time	t_{ids}	Refer to Timing Diagrams	2	—	—	μs

Timing Diagrams

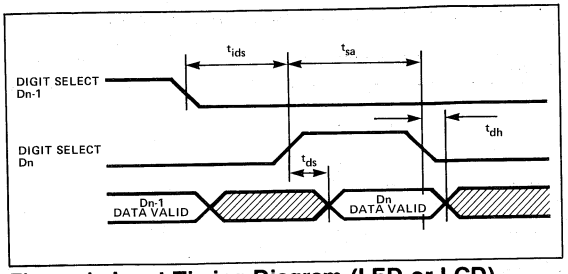


Figure 1: Input Timing Diagram (LED or LCD)

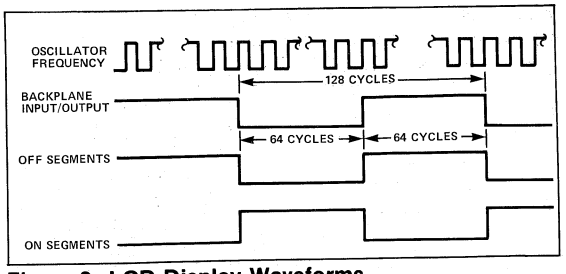


Figure 2: LCD Display Waveforms

Test Circuit

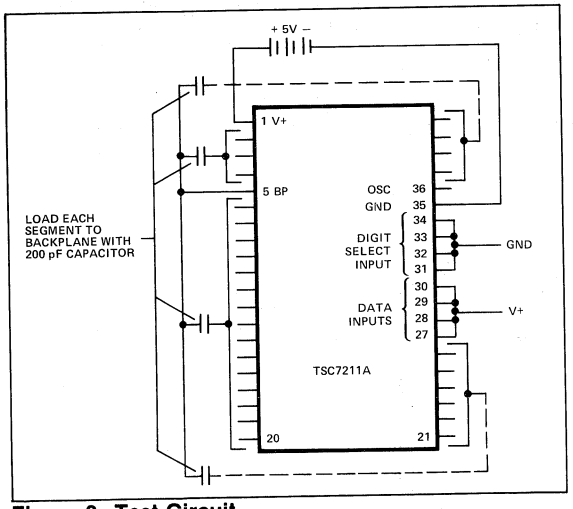
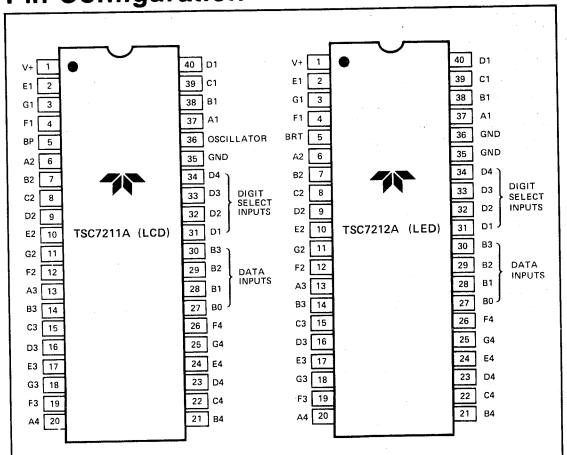


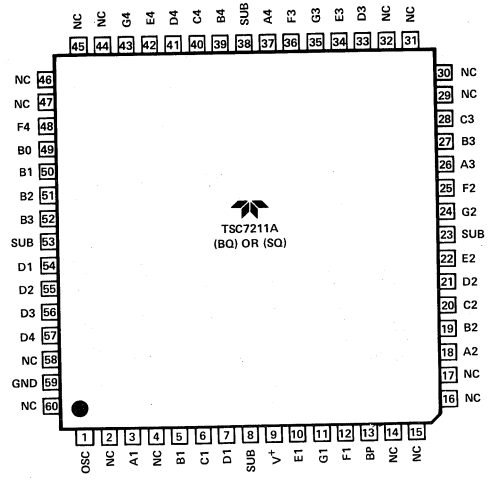
Figure 3: Test Circuit

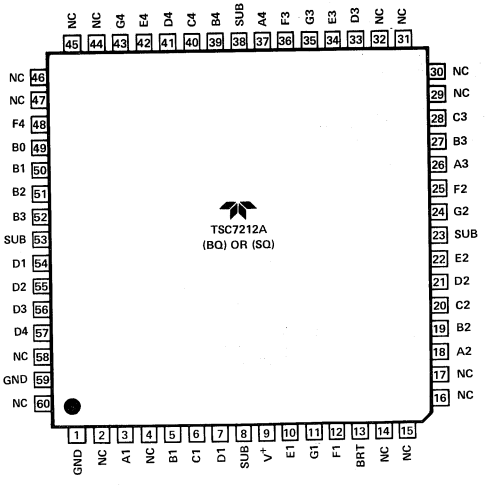
Pin Configuration



Flat Package

NOTES:
1. NC = NO INTERNAL CONNECTION
2. PINS 8, 23, 38 AND 53 ARE CONNECTED TO THE DIE SUBSTRATE. THE POTENTIAL AT THESE PINS IS APPROXIMATELY V^+. NO EXTERNAL CONNECTIONS SHOULD BE MADE.





Input Definitions

In this table, V+ and GROUND are considered to be normal operating input logic levels. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL*	CONDITION	FUNCTION	
B0	27 (49)	V+ = Logical One GND = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28 (50)	V+ = Logical One GND = Logical Zero	Twos	
B2	29 (51)	V+ = Logical One GND = Logical Zero	Fours	
B3	30 (52)	V+ = Logical One GND = Logical Zero	Eights (Most Significant)	
OSC (LCD Devices only)	36 (1)	Floating or with external capacitor GROUND	Oscillator Input	
			Disables BP output devices, allowing segments to be synchronized to an external signal input at the BP terminal (Pin 5)	
D1	31 (54)		D1 (Least significant) Digit Select	
D2	32 (55)	V+ = Active	D2 Digit Select	
D3	33 (56)	GND = Inactive	D3 Digit Select	
D4	34 (57)		D4 (Most significant) Digit Select	

* 60-Pin Flat Package Pin # in ( ).

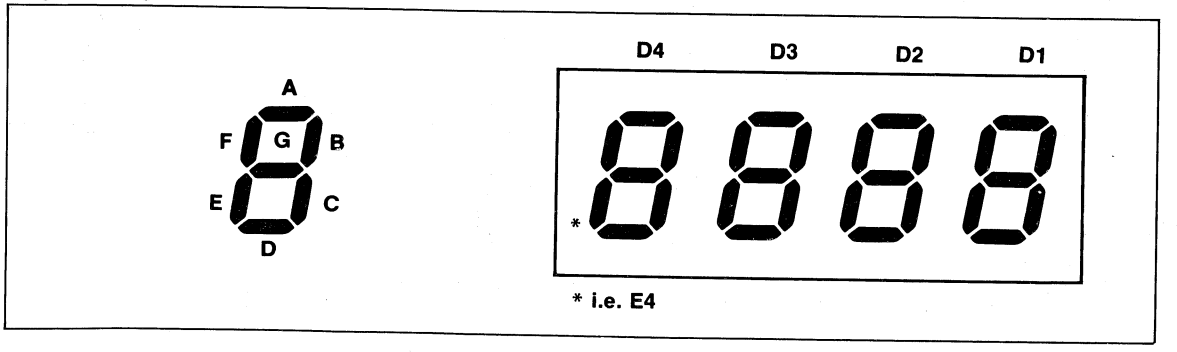
Output Definitions

Output pins are defined by the alphabetical segment assignment and numerical digital assignment.

OUTPUT	TERMINAL*	FUNCTION			OUTPUT	TERMINAL*	FUNCTION		
A1	37 (3) A	Segment Dr.	Digit 1	(LSD)	A3	13 (26) A	Segment Dr.	Digit 3	
B1	38 (5) B				B3	14 (27) B			
C1	39 (6) C				C3	15 (28) C			
D1	40 (7) D				D3	16 (33) D			
E1	2 (10) E				E3	17 (34) E			
F1	4 (12) F				F3	19 (36) F			
G1	3 (11) G				G3	18 (35) G			
A2	6 (18) A	Segment Dr.	Digit 2		A4	20 (37) A	Segment Dr.	Digit 4	(MSD)
B2	7 (19) B				B4	21 (39) B			
C2	8 (20) C				C4	22 (40) C			
D2	9 (21) D				D4	23 (41) D			
E2	10 (22) E				E4	24 (42) E			
F2	12 (25) F				F4	26 (48) F			
G2	11 (24) G				G4	25 (43) G			

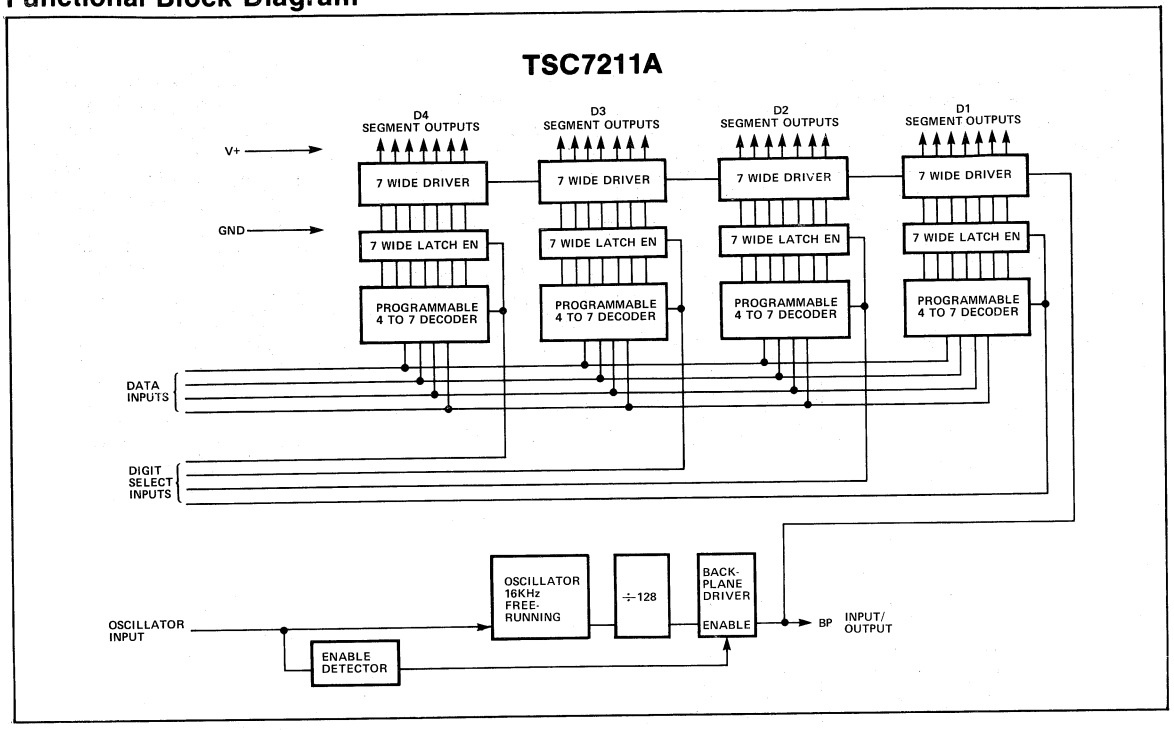
* 60-Pin Flat Package Pin # in ( ).

Digit Assignment



Functional Block Diagram

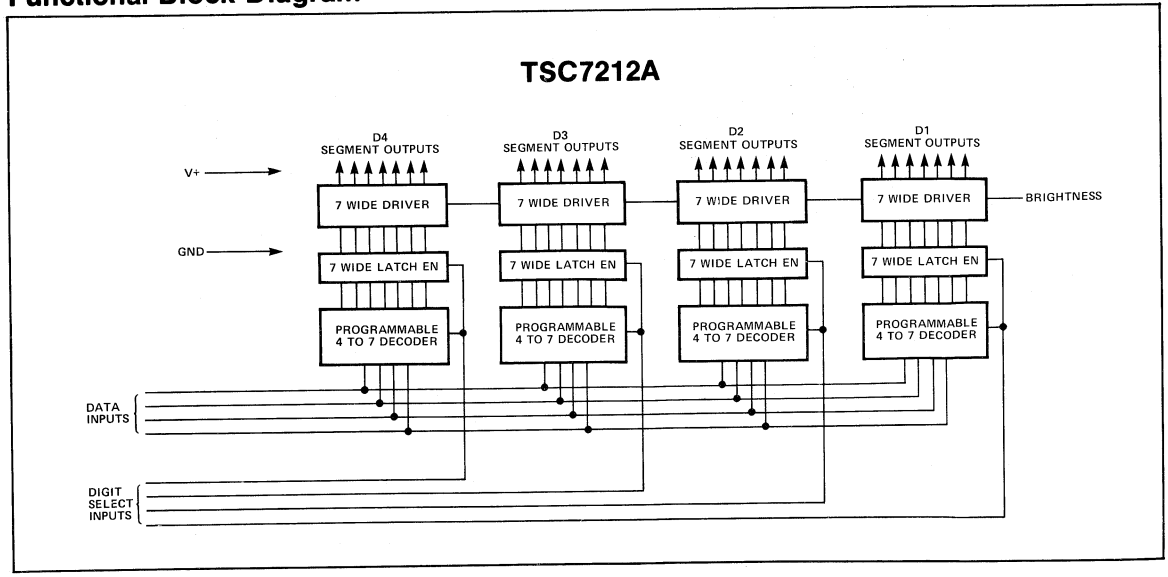
TSC7211A



10

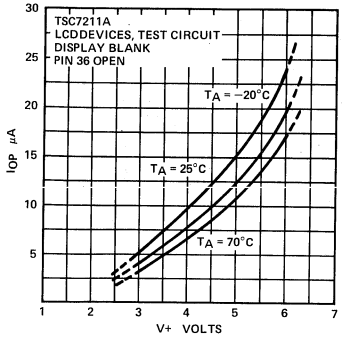
Functional Block Diagram

TSC7212A

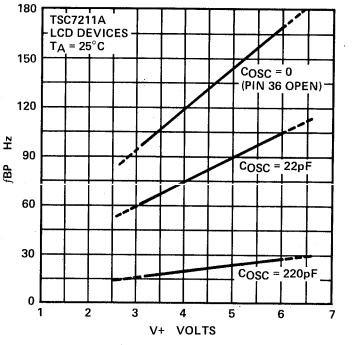


Typical Operating Characteristics

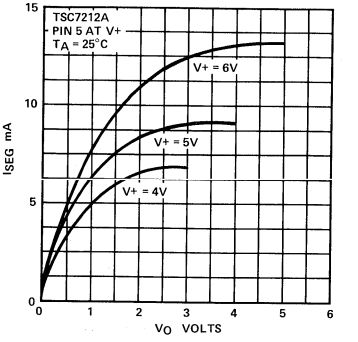
TSC7211A Operating Supply Current as a Function of Supply Voltage



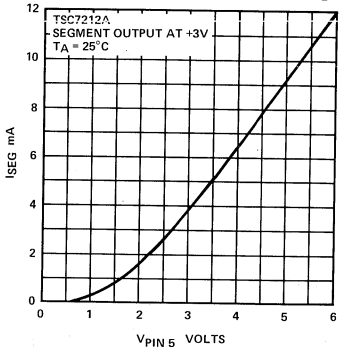
TSC7211A Backplane Frequency as a Function of Supply Voltage



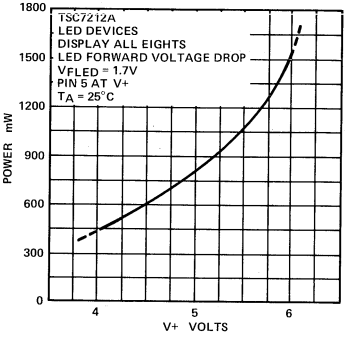
TSC7212A LED Segment Current as a Function of Output Voltage



TSC7212A LED Segment Current as a Function of Brightness Control Voltage



TSC7212A Operating Power (LED Display) as a Function of Supply Voltage



Basic Operation

Basic Operation
TSC7211A (LCD) Decoder/Driver

The TSC7211A drives four digit by seven segment LCD displays. The device contains 28 individual segment drivers, a backplane driver, an on chip oscillator and a divider chain to generate the backplane signal.

The 28 CMOS segment drivers and backplane driver contain ratioed N and P channel transistors for identical "ON" resistance. The equal resistances eliminate the d.c. output driver component resulting from unequal rise and fall times. This ensures maximum LCD display life.

The backplane output driver can be disabled by grounding the oscillator input (pin 36). The 28 output segment drivers can therefore be synchronized directly to an input signal at the backplane terminal (pin 5). Several slave devices may be cascaded to the backplane output of a master device. The backplane signal may also be derived from an external source. These features permit interfacing to single backplane LCD displays with characters in multiples of four.

Each slave's backplane input represents only a 200 pF capacitive load to the master backplane driver (comparable to one additional segment). The number of slave devices driveable by a master device is therefore set by the larger display backplane capacitive load. The master backplane output will drive the display backplane of 16 one-half inch characters with rise and fall times under 5 μsec. This represents a system with 3 slave devices and a fourth master TSC7211A driving the backplane.

If more than four devices are slaved together, the backplane signal should be derived externally and all TSC7211A devices slaved to it. The external drive signal must drive a high capacitive load with 1-2 μsec rise and fall times. The backplane frequency is normally 125 Hz. At lower display ambient temperatures the frequency may be reduced to compensate for display response time.

The on chip RC oscillator free runs at approximately 16 kHz. A divide by 128 circuit provides the 125 Hz backplane frequency. The oscillator frequency may be reduced by connecting an external capacitor between the oscillator terminal (pin 36) and V+ (see typical operating characteristic curve).

The free running oscillator may be overriden, if desired, by an external clock. The backplane driver, however, must not be disabled during the external clock's negative or low portion as this will result in a d.c. drive component being applied to the LCD display. This would limit the LCD's display's life. To prevent backplane driver disabling, the oscillator input should be driven from the positive supply to no less than one-fifth the supply voltage above ground. A backplane disable signal will not be sensed if the driving signal remains above ground by one-fifth the supply voltage. An alternate method for externally driving the oscillator permits the oscillator input to swing the full supply voltage range. The oscillator input signal duty cycle is skewed so the low portion duration is less than 1 μsec. The backplane disable sensing circuit will not respond to such a short signal.

10

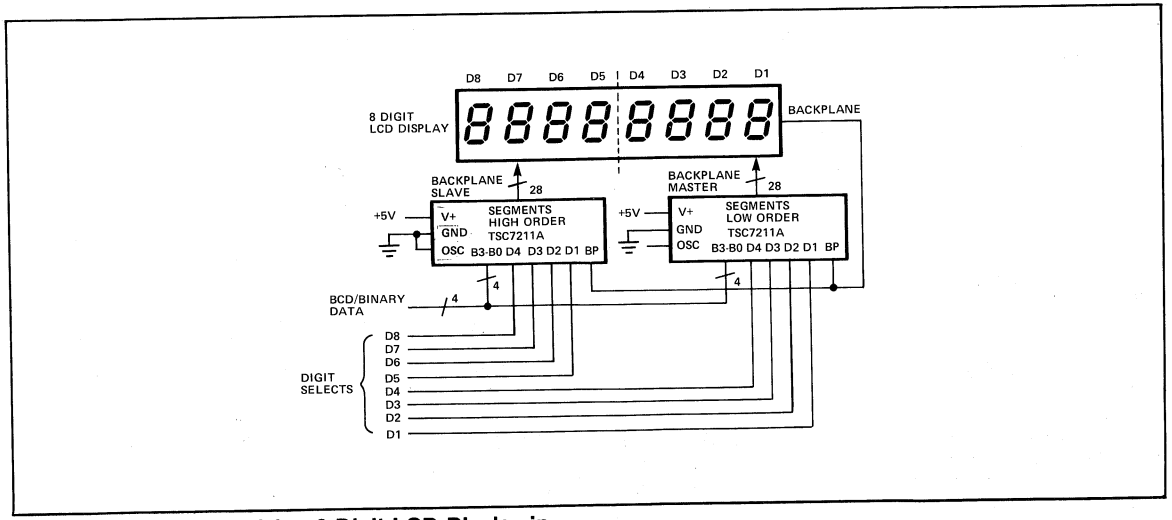


Figure 4: TSC7211A Driving 8 Digit LCD Display in Master Slave Configuration.

TSC7212A LED Decoder/Driver

The TSC7212A directly drives four digit, seven segment, common anode LED displays. The 28 segment drivers are low leakage, current controlled, open drain N-channel MOS transistors.

A brightness input (pin 5) can be used in two ways to control output transistor drain current. The voltage at the brightness control input is transferred to the output transistor gate for "ON" segments. The brightness voltage directly modulates the segment drivers "ON" resistance. A variable brightness control may be implemented with a single potentiometer (Figure 4). A high value potentiometer (100 kΩ to 1 mΩ) will minimize power consumption.

The brightness input may also be operated digitally as a display enable. At a logic 1 the display is fully "ON" and at a logic 0 fully "OFF." The display brightness may be controlled by a logic signal of varying duty cycle also. When operating with LEDs at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperature rise. The maximum power dissipation is 1 watt at 25°C. Derated linearly above 35°C to 500 mW at 70°C (-15 mW/°C above 35°C). Power dissipation for the device is given by:

$$P = (V^+ - V_{FLED})\ (I_{SEG})\ \ (n_{SEG})$$

where V_{FLED} is the LED forward voltage drop, I_{SEG} is segment current, and n_{SEG} is the number of "ON" segments. If the device is operated at elevated temperatures, the segment current can be limited through the brightness input to keep power dissipation within the limits described above.

For applications requiring brighter LED displays see the TSC700A data sheet.

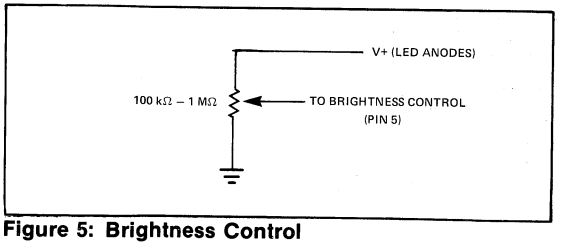


Figure 5: Brightness Control

Input Configuration and Output Codes

The TSC7211A/TSC7212A accept a four-bit, true binary (positive level = logic 1) input at pins 27 (LSB) through 30 (MSB). The binary input is decoded to the seven segment output known as "Code B." The output display format is 0-9, dash, E, H, L.,P and blank (see Table 1). The TSC7211A and TSC7212A will correctly decode binary and BCD true codes to a seven-segment output.

The TSC7211A/TSC7212A accept multiplexed binary or BCD input data at pins 27 (LSB) through pin 30 (MSB). Pins 31 (LSD) through 34 (MSD) are the digit select lines. When the digit select line is taken to a logic 1 level the input data is decoded and stored in the enabled output latch of the selected digit. More than one digit select line may be activated simultaneously. The same character will be written into all selected digits. See Figure 5 for decoder segment assignments.

BINARY INPUT				CODE B TSC7211A TSC7212A
B3	B2	B1	B0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	-
1	0	1	1	E
1	1	0	0	H
1	1	0	1	L
1	1	1	0	P
1	1	1	1	(Blank)

Table I: Output Code

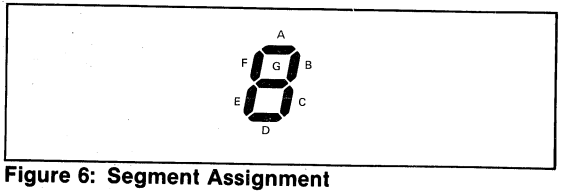


Figure 6: Segment Assignment

Special Order Decoder Option

The TSC7211A and TSC7212A are mask programmed to give the 16 combinations of seven segment output codes. For large volume orders (50 k pieces minimum) custom decoder options are available. Contact factory for details.

Applications Information

The TSC7212A has two ground pins. These pins should be connected together.

Applications Information (Continued)

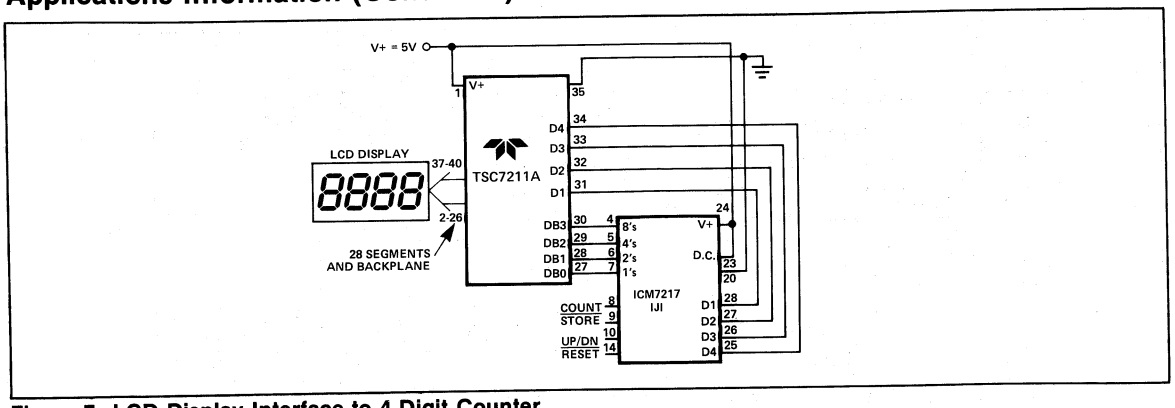


Figure 7: LCD Display Interface to 4 Digit Counter

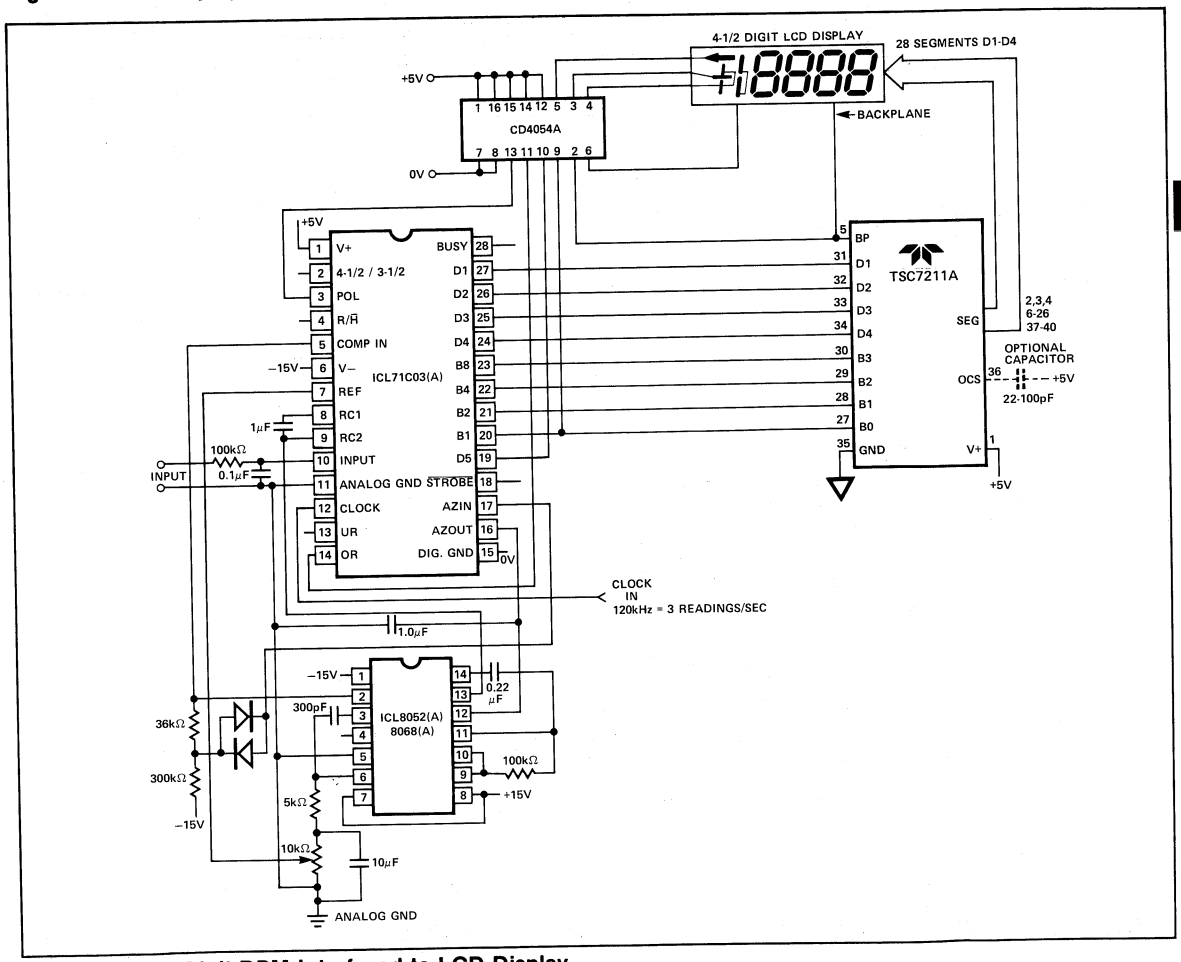


Figure 8: 4 1/2 Digit DPM Interfaced to LCD Display

Typical Applications

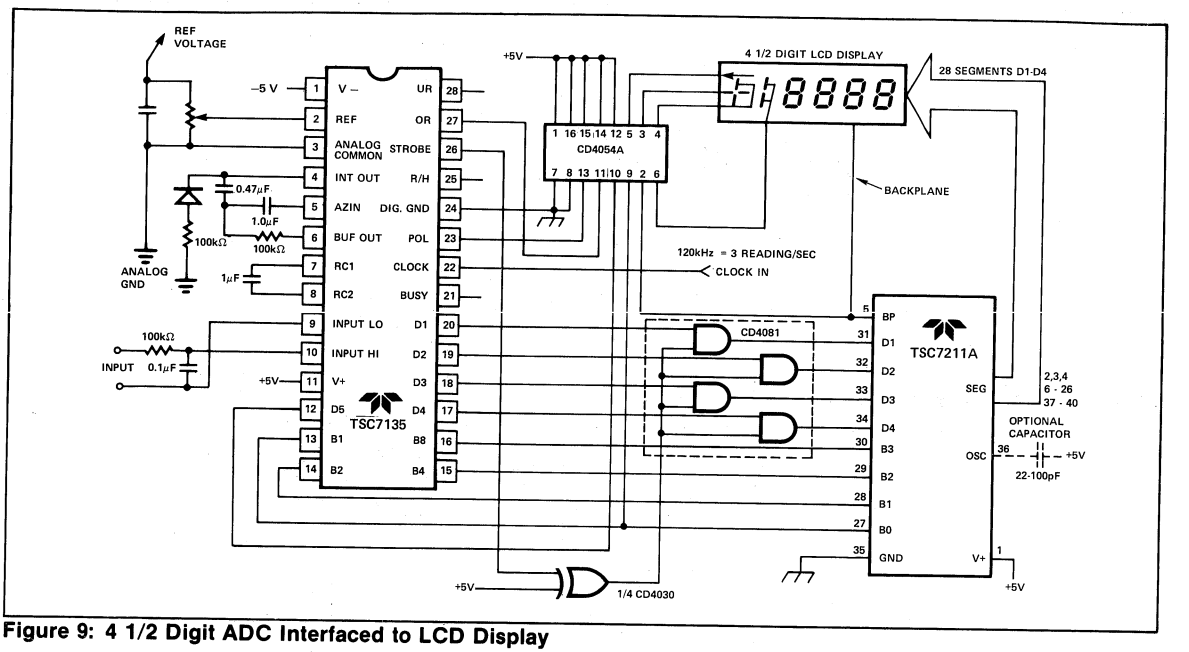


Figure 9: 4 1/2 Digit ADC Interfaced to LCD Display

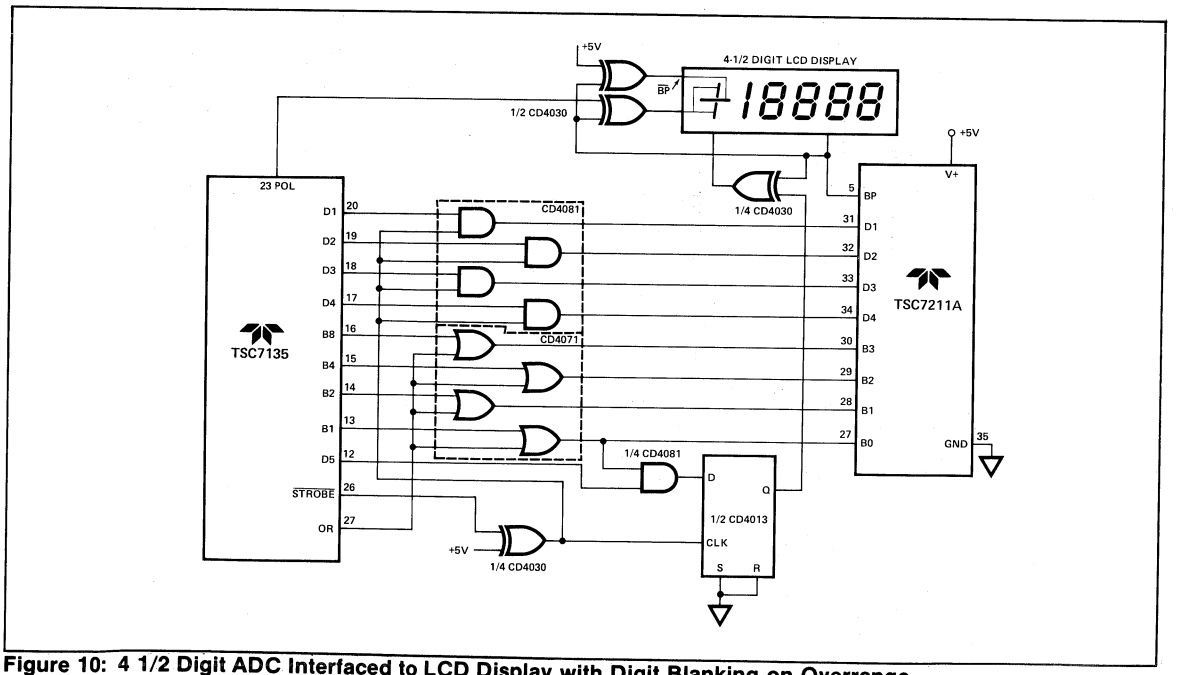


Figure 10: 4 1/2 Digit ADC Interfaced to LCD Display with Digit Blanking on Overrange

Typical Applications (continued)

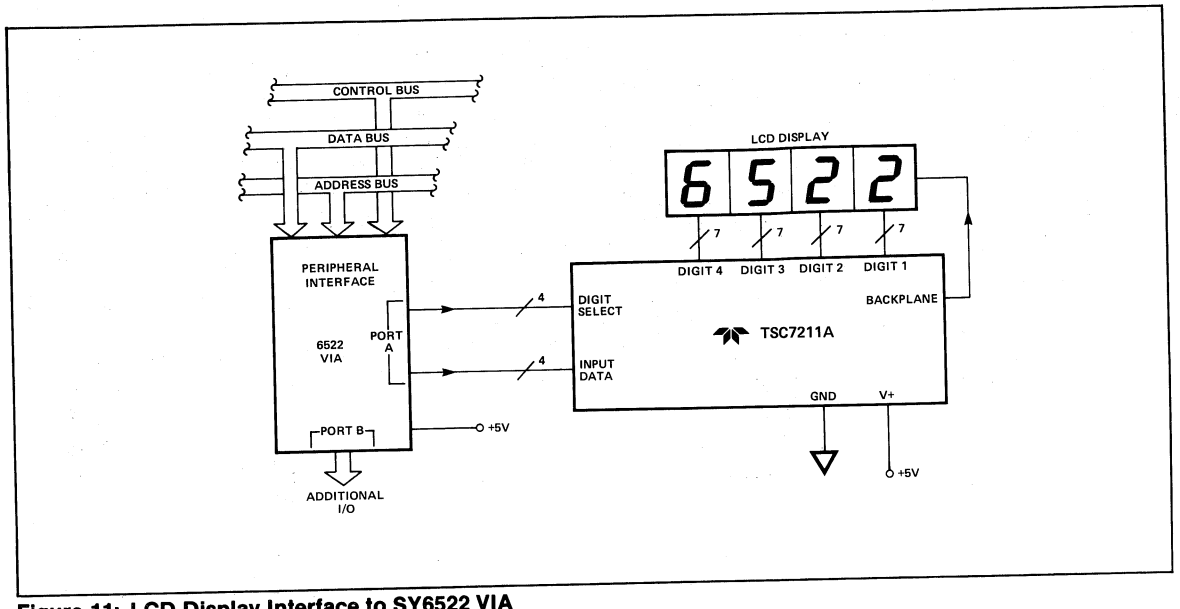


Figure 11: LCD Display Interface to SY6522 VIA

10

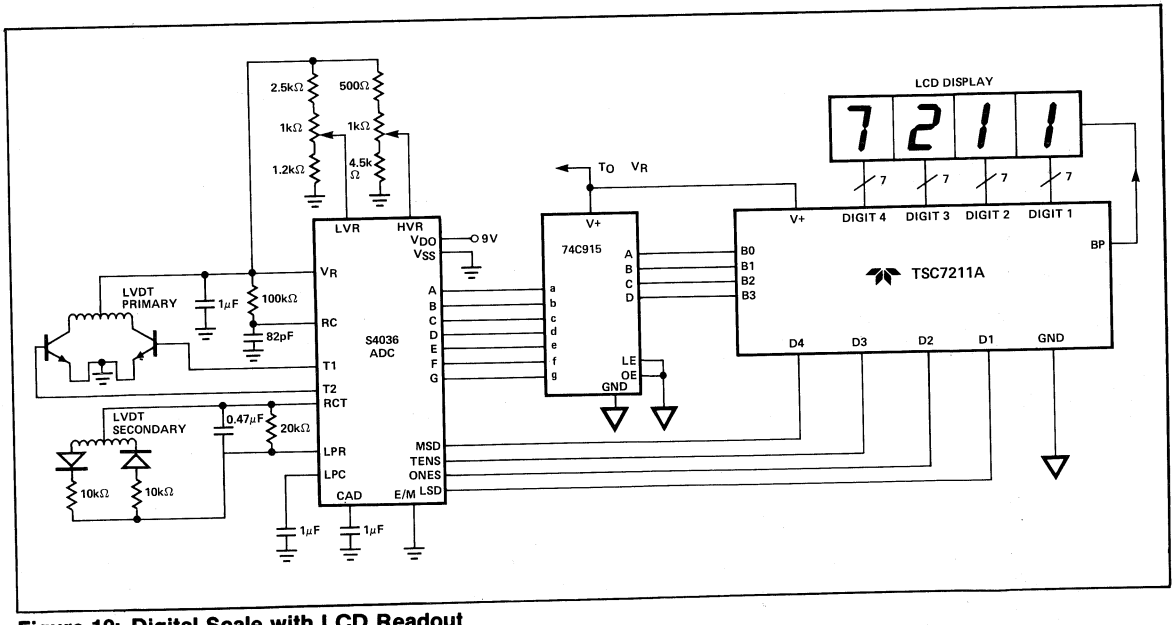


Figure 12: Digital Scale with LCD Readout

Typical Applications (continued)

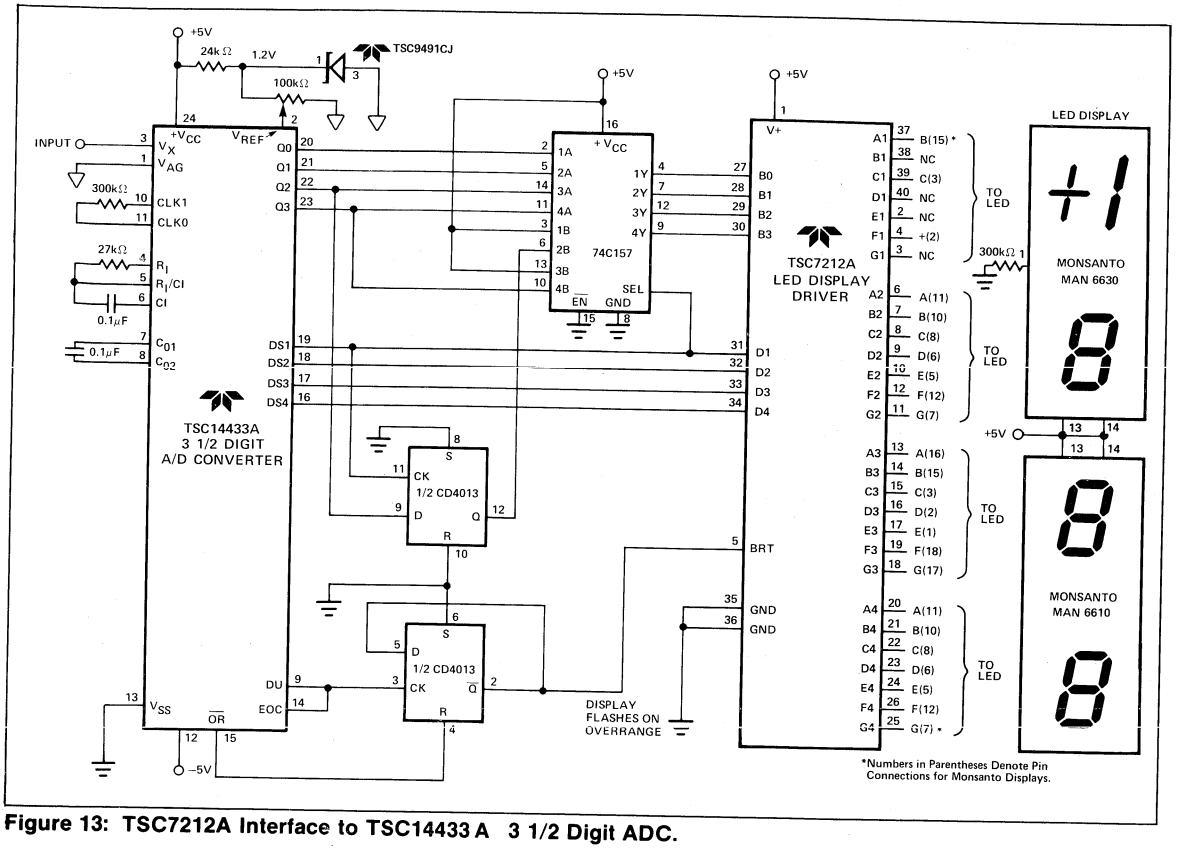
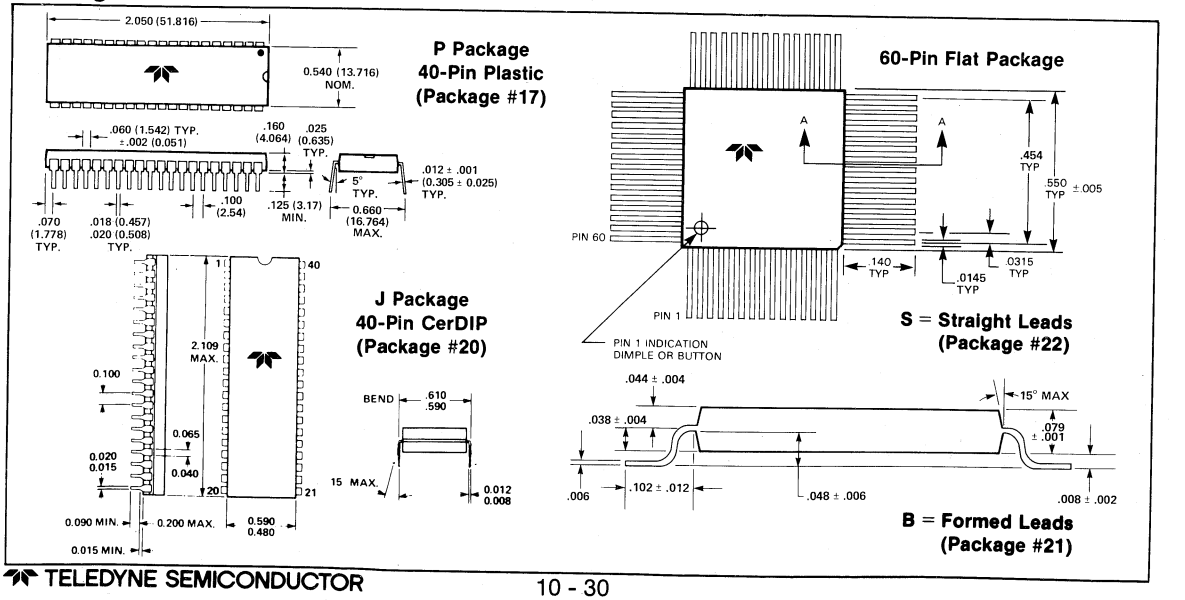


Figure 13: TSC7212A Interface to TSC14433A 3 1/2 Digit ADC.

Package Dimensions



TSC7211AM (LCD)
TSC7212AM (LED)
BUS Compatible Four Digit CMOS Decoder/Driver
• Input Data Latches

General Description

The TSC7211AM (LCD Decoder/Driver) and TSC7212AM (LED Decoder/Driver) are CMOS direct drive, four digit, seven segment display decoder and drivers. The devices are bus compatible making microprocessor controlled displays possible. Two chip select signals control data and digit select code latching prior to decoding and display. External data latches are unnecessary.

The TSC7211AM drives conventional LCD displays. An RC oscillator, divider chain, backplane driver, and 28 segment outputs are provided on a single CMOS chip. The segment drivers supply square waves of the same frequency as the backplane but in phase for an OFF segment and out of phase for an ON segment. The net d.c. voltage applied between driver segment and backplane is near zero maximizing display lifetime.

The TSC7212AM drives common-anode LED displays with 28 current controlled, low leakage, open drain, N-Channel output transistors. The brightness control input can be used as a digital display enable. A varying voltage at the control input will allow continuous display brightness control.

The four bit binary input code is decoded into the seven segment alphanumeric code known as "Code B." The "Code B" output format results in a 0 to 9, —, E, H, L, P or blank display. True BCD or binary inputs will be correctly decoded to the seven segment display format.

Ordering Information

Part No.	Driver Type	Package	Output Code	Input Config.
TSC7211AMIPL	LCD	40-Pin Plastic	Code B	Data and Digit Select Latches
TSC7212AMIPL	LED	40-Pin Plastic	Code B	Data and Digit Select Latches
TSC7211AM/Y	LCD	DICE	Code B	Data and Digit Select Latches
TSC7212AM/Y	LED	DICE	Code B	Data and Digit Select Latches

TSC7211AM Features (LCD Driver)

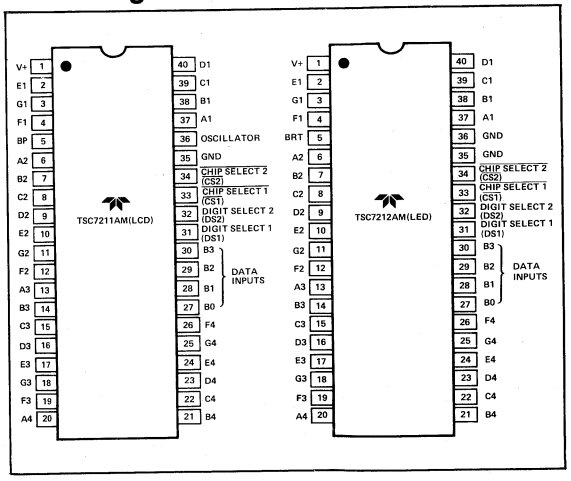
- Four digit non-multiplexed seven segment LCD display outputs with backplane driver.
- Input and digit select data latches.
- RC oscillator on-chip generates backplane drive signal.
- Eliminates d.c. bias which degrade LCD display life.
- Backplane input/output pin permits synchronization of cascaded slave device to master backplane signal.
- Binary and BCD inputs decoded to code B (0 to 9, —, E, H, L, P, blank).
- Pin compatible and functionally equivalent to ICM7211AM.

TSC7212AM Features (LED Driver)

- 28 current limited outputs drive common-anode LEDs at 8 mA per segment.
- Input and digit select data latches.
- Brightness input allows potentiometer control of LED segment current. Pin also serves as digital display enable.
- Same input configuration and output decoding as the TSC7211AM.
- Pin compatible and functionally equivalent to ICM7212AM.

10

Pin Configuration



Absolute Maximum Ratings

Power Dissipation (Note 1) ..... 1.0 W at 70°C
Supply Voltage ..... 6.5 V
Input Voltage (Any
Terminal) (Note 2) ..... V^+ +0.3 V, GROUND -0.3 V
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... -55°C to +125°C
Lead Temperature (Soldering 10 sec.) ..... 300°C

Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This limit refers to that of the package and will not be realized during normal operation.

Note 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive device latchup. For this reason it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the TSC7211AM/TSC7212AM be turned on first.

Table I: Operating Characteristics

Test Conditions: All parameters measured with V+ = 5 V.

TSC7211AM Characteristics (LCD Decoder/Driver)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range	V_{SUPP}		3	5	6	V
Operating Current	I_{OP}	Display Blank	—	10	50	μA
Oscillator Input Current	I_{OSCI}	Pin 36	—	±2	±10	μA
Segment Rise/Fall Time	t_{RFS}	C_L = 200 pF	—	0.5	—	μA
Backplane Rise/Fall Time	t_{RFB}	C_L = 5000 pF	—	1.5	—	μs
Oscillator Frequency	f_{OSC}	Pin 36 Floating	—	16	—	kHz
Backplane Frequency	f_{BP}	Pin 36 Floating	—	125	—	Hz

TSC7212AM Characteristics (Common-Anode LED Decoder/Driver)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_{SUPP}		4	5	6	V
Operating Current Display Off	I_{OP}	Pin 5 (Brightness), Pins 27-34 = GROUND	—	10	50	μA
Operating Current	I_{OP}	Pin 5 at V+, Display all 8's	—	200	—	mA
Segment Leakage Current	I_{SLK}	Segment Off	—	±0.01	±1	μA
Segment On Current	I_{SEG}	Segment On, V_O = +3 V	5	8	—	mA

Input Characteristics (LCD and LED Decoder/Driver)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Logical "1" Input Voltage	V_{IH}		3	—	—	V
Logical "0" Input Voltage	V_{IL}		—	—	1	V
Input Leakage Current	I_{ILK}	Pins 27 - 34	—	±0.01	±1	μA
Input Capacitance	C_{IN}	Pins 27 - 34	—	5	—	pF
BP/Brightness Input Leakage	I_{BPLK}	Measured at Pin 5 with Pin 36 at GND	—	±0.01	±1	μA
BP/Brightness Input Capacitance	C_{BPI}	All Devices	—	200	—	pF

AC Characteristics (LCD and LED Decoder/Driver)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Chip Select Active Pulse Width	t_{CSA}	Note 1	200	—	—	ns
Data Setup Time	t_{DS}		100	—	—	ns
Data Hold Time	t_{DH}		10	0	—	ns
Inter-Chip Select Time	t_{ICS}		2	—	—	μs

Note:
1. Other Chip Select ($\overline{CS}$) is either held at logic zero or both $\overline{CS1}$ and $\overline{CS2}$ driven together.

Timing Diagrams

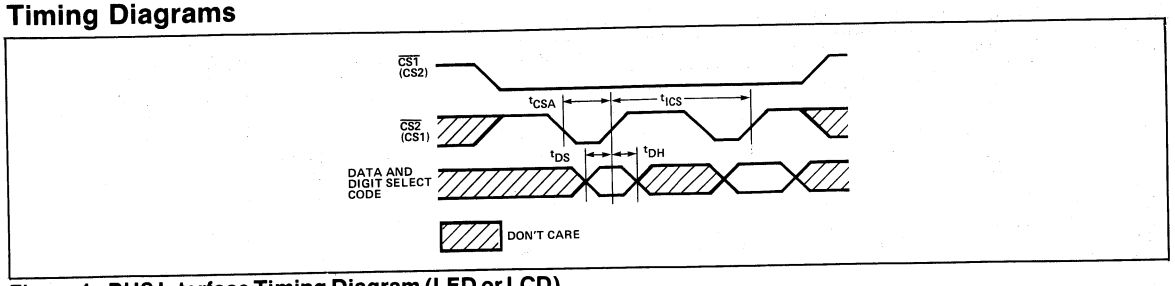


Figure 1: BUS Interface Timing Diagram (LED or LCD)

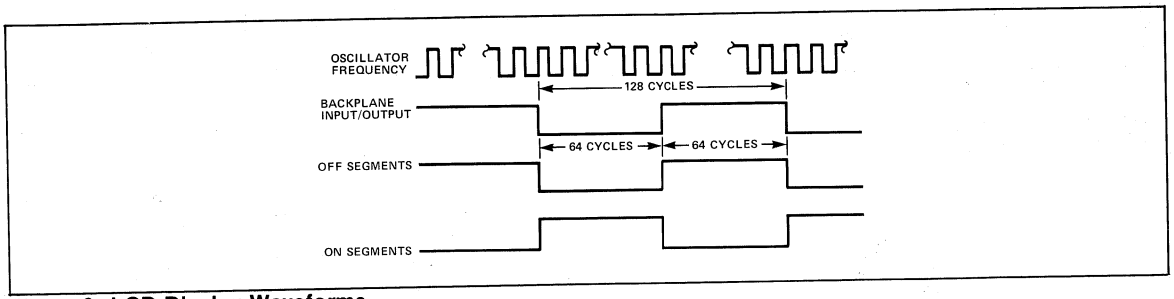


Figure 2: LCD Display Waveforms

10

Input Definitions

In this table, V + and GROUND are considered to be normal operating input logic levels. For lowest power consumption, input signals should swing over the full supply.

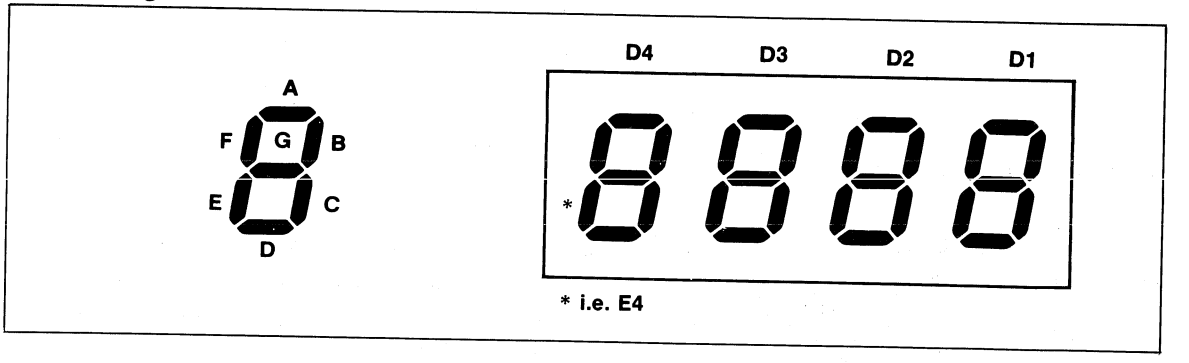
INPUT	TERMINAL	CONDITION	FUNCTION	
B0	27	V + Logical One GND = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28	V+ = Logical One GND = Logical Zero	Twos	
B2	29	V+ = Logical One GND = Logical Zero	Fours	
B3	30	V+ = Logical One GND = Logical Zero	Eights (Most Significant)	
OSC (LCD Devices only)	36	Floating or with external capacitor GROUND	Oscillator Input Disables BP output devices, allowing segments to be synchronized to an external signal input at the BP terminal (Pin 5)	
DS1	31	V+ = Logical One	Digit Select Inputs DS2, DS1 = 00 Selects D4 DS2, DS1 = 01 Selects D3 DS2, DS1 = 10 Selects D2 DS2, DS1 = 11 Selects D1	
DS2	32	GND = Logical Zero		
$\overline{CS1}$	33	V+ = Inactive	When both $\overline{CS1}$ and $\overline{CS2}$ are low the data and digit select input latches are open or enabled. On the rising of $\overline{CS1}$ or $\overline{CS2}$ data is latched, decoded and stored in the output drive latches.	
$\overline{CS2}$	34	GND = Active		

Output Definitions

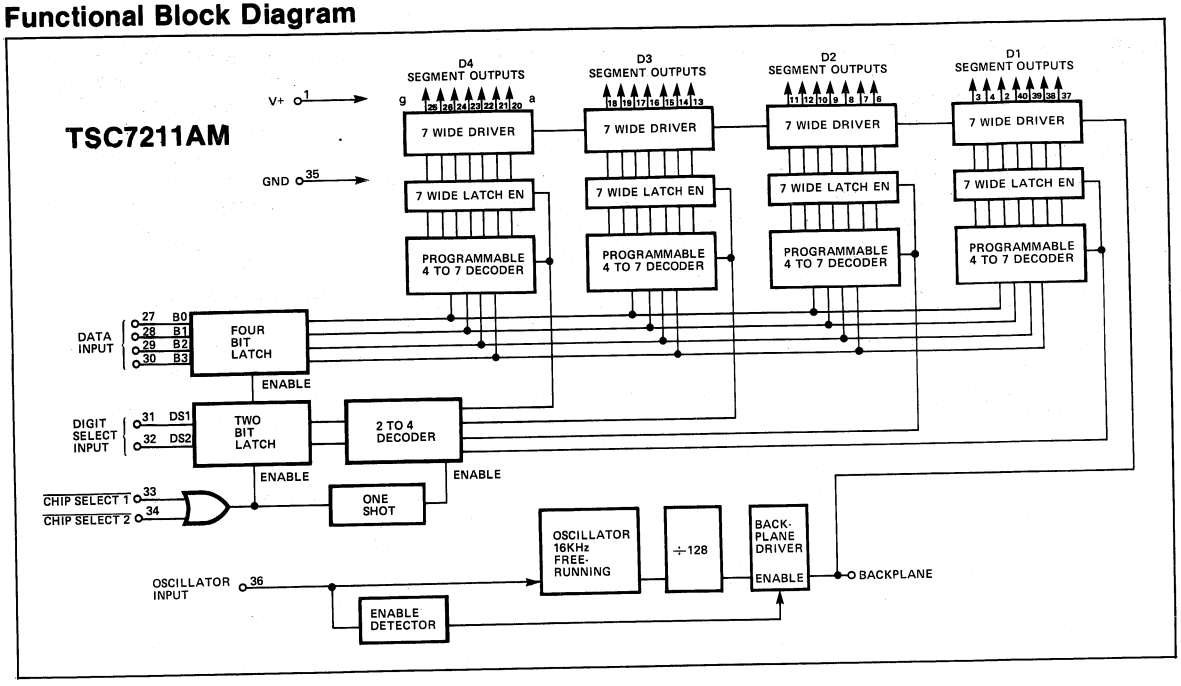
Output pins are defined by the alphabetical segment assignment and numerical digital assignment.

OUTPUT	TERMINAL	FUNCTION	OUTPUT	TERMINAL	FUNCTION
A1	37	A Segment Dr. Digit 1 (LSD)	A3	13	A Segment Dr. Digit 3
B1	38	B	B3	14	B
C1	39	C	C3	15	C
D1	40	D	D3	16	D
E1	2	E	E3	17	E
F1	4	F	F3	19	F
G1	3	G	G3	18	G
A2	6	A Segment Dr. Digit 2	A4	20	A Segment Dr. Digit 4 (MSD)
B2	7	B	B4	21	B
C2	8	C	C4	22	C
D2	9	D	D4	23	D
E2	10	E	E4	24	E
F2	12	F	F4	26	F
G2	11	G	G4	25	G

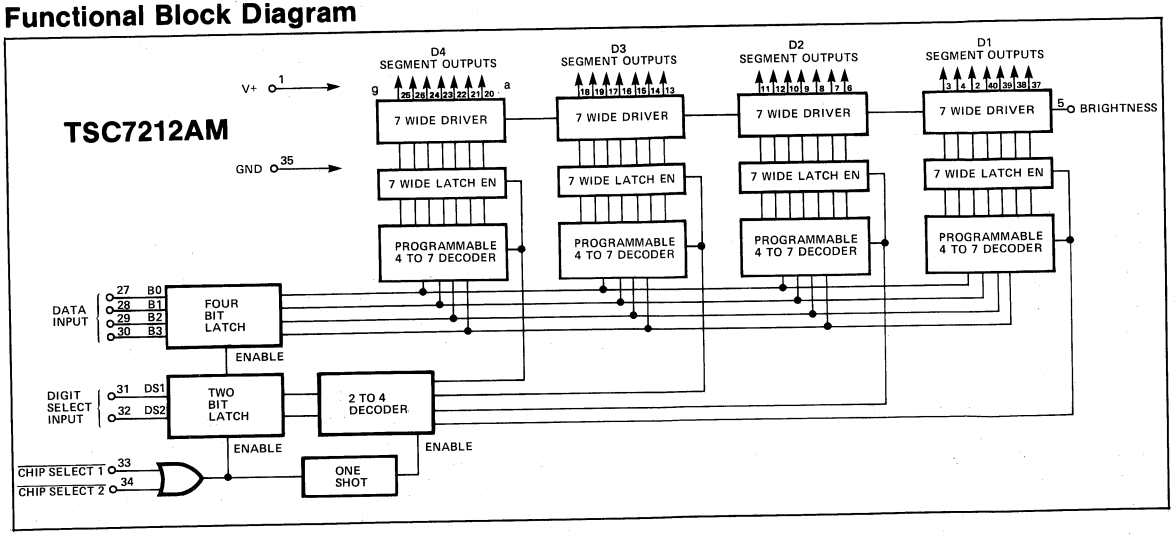
Digit Assignment



Functional Block Diagram



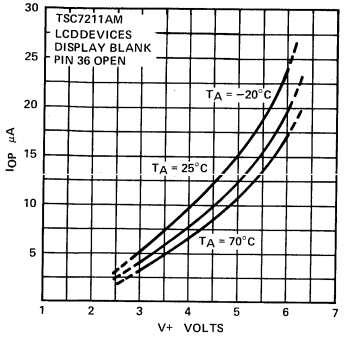
Functional Block Diagram



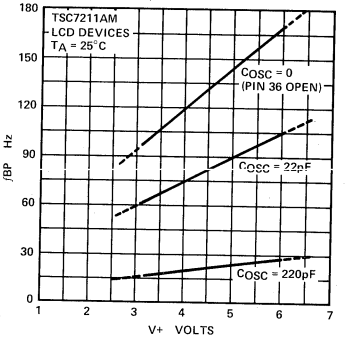
10

Typical Operating Characteristics

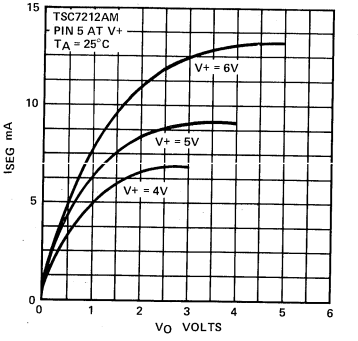
TSC7211AM Operating Supply Current as a Function of Supply Voltage



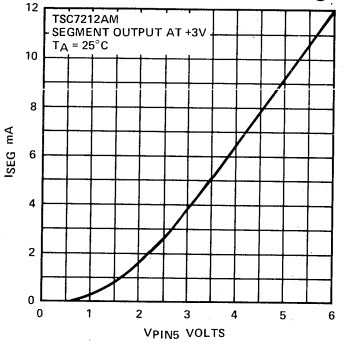
TSC7211AM Backplane Frequency as a Function of Supply Voltage



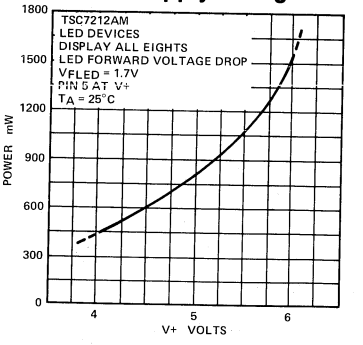
TSC7212AM LED Segment Current as a Function of Output Voltage



TSC7212AM LED Segment Current as a Function of Brightness Control Voltage



TSC7212AM Operating Power (LED Display) as a Function of Supply Voltage



Basic Operation
TSC7211AM (LCD) Decoder/Driver

The TSC7211AM drives four digit, seven segment LCD displays. The device contains 28 individual segment drivers, a backplane driver, a self contained oscillator and a divider chain to generate the backplane signal.

The 28 CMOS segment drivers and backplane driver contain ratioed N and P channel transistors for identical "ON" resistance. The equal resistances eliminate the d.c. output driver component resulting from unequal rise and fall times. This ensures maximum LCD display life.

The backplane output driver can be disabled by grounding the oscillator input (pin 36). The 28 output segment drivers can therefore be synchronized directly to an input signal at the backplane terminal (pin 5). Several slave devices may be cascaded to the backplane output of a master device. The backplane signal may also be derived from an external source. These features permit interfacing to single backplane LCD displays with characters in multiples of four.

Each slave's backplane input represents only a 200 pF capacitive load to the master backplane driver (comparable to one additional segment). The number of slave devices driveable by a master device is therefore set by the larger display backplane capacitive load. The master backplane output will drive the display backplane of 16 one-half inch characters with rise and fall times under 5 µsec. This represents a system with 3 slave devices and a fourth master TSC7211AM driving the backplane (Figure 3).

If more than four devices are slaved together, the backplane signal should be derived externally and all TSC7211AM devices slaved to it. The external drive signal must drive a high capacitive load with 1-2 µsec rise and fall times. The backplane frequency is normally 125 Hz. At lower display ambient temperatures the frequency may be reduced to compensate for display response time.

The on chip RC oscillator free runs at approximately 16 kHz. A divide by 128 circuit provides the 125 Hz backplane frequency. The oscillator frequency may be reduced by connecting an external capacitor between the oscillator terminal (pin 36) and V+ (see typical operating characteristic curve).

The free running oscillator may be overriden, if desired, by an external clock. The backplane driver, however, must not be disabled during the external clock's negative or low portion as this will result in a d.c. drive component being applied to the LCD display. This would limit the LCD's display's life. To prevent backplane driver disabling, the oscillator input should be driven from the positive supply to no less than one-fifth the supply voltage above ground. A backplane disable signal will not be sensed if the driving signal remains above ground by one-fifth the supply voltage. An alternate method for externally driving the oscillator permits the oscillator input to swing the full supply voltage range. The oscillator input signal duty cycle is skewed so the low portion duration is less than 1 μsec. The backplane disable sensing circuit will not respond to such a short signal.

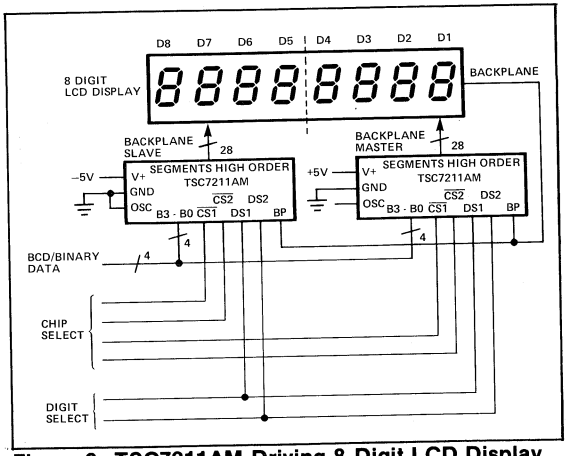


Figure 3: TSC7211AM Driving 8-Digit LCD Display in Master Slave Configuration.

TSC7212AM LED Decoder/Driver

The TSC7212AM directly drives four digit, seven segment, common-anode LED displays. The 28 segment drivers are low leakage, current controlled, open drain N-channel MOS transistors.

A brightness input (pin 5) can be used in two ways to control output transistor drain current. The voltage at the brightness control input is transferred to the output transistor gate for "ON" segments. The brightness voltage directly modulates the segment drivers "ON" resistance. A variable brightness control may be implemented with a single potentiometer (Figure 4). A high value potentiometer (100 kΩ to 1 MΩ) will minimize power consumption.

The brightness input may also be operated digitally as a display enable. At a logic 1 the display is fully "ON" and at a logic 0 fully "OFF." The display brightness may be controlled by a logic signal of varying duty cycle also. When operating with LEDs at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperature rise. The maximum power dissipation is 1 watt at 25° C. Derate linearly above 35° C to 500 mW at 70° C (-15 mW/° C above 35° C). Power dissipation for the device is given by:

$$P = (V^+ - V_{FLED})\ (I_{SEG})\ (n_{SEG})$$

where V_{FLED} is the LED forward voltage drop, I_{SEG} is segment current, and n_{SEG} is the number of "ON" segments. If the device is operated at elevated temperatures, the segment current can be limited through the brightness input to keep power dissipation within the limits described above.

The display may be blanked (all segments OFF) by applying the input code 1111 or by driving the brightness pin with a logic 0. If brightness control is not needed, pin 5 should be tied to 5.0 V.

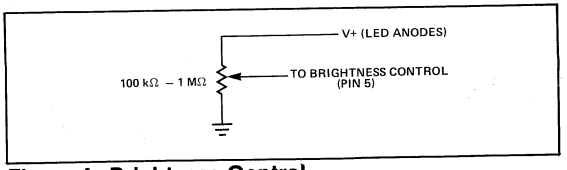


Figure 4: Brightness Control

Input Configuration and Output Codes

The TSC7211AM/TSC7212AM accept a four bit, true binary (positive level = logic 1) input at pins 27 (LSB) through 30 (MSB). The output display format is 0 to 9, —, E, H, L,P and blank (see Table 1). Segment assignments are shown in Figure 5. The TSC7211AM and TSC7212AM will correctly decode binary and BCD true codes to a seven segment output.

The TSC7211AM and TSC7212AM are designed to interface with a data bus and display data under microprocessor control. Four data input bits (Pins 27-30) and two digit select input bits (Pins 31, 32) are written into input buffer latches. The rising edge of either chip select causes data to be latched, decoded and stored in the selected digit output data latch. The two bit digit code selects the appropriate output digit latch. The four bit display data word is decoded to the "Code B" seven segment output format.

For applications where bus compatibility is not required refer to the TSC7211A (LCD), TSC7212A (LED) and TSC700A (LED) four digit decoder driver data sheets. These devices are designed to accept multiplexed BCD/Binary input data for display under the control of four separate digit select control signals.

BINARY INPUT				CODE B TSC7211AM TSC7212AM
B3	B2	B1	B0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	—
1	0	1	1	E
1	1	0	0	H
1	1	0	1	L
1	1	1	0	P
1	1	1	1	(Blank)

Table 1: Output Code

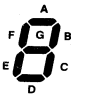


Figure 5: Segment Assignment

Special Order Decoder Option

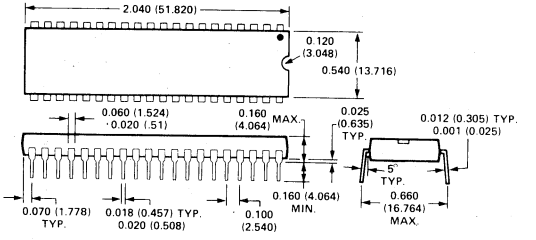
The TSC7211AM and TSC7212AM are mask programmed to give the 16 seven segment output codes. For large volume orders (25 k pieces minimum) custom decoder options are available. Contact factory for details.

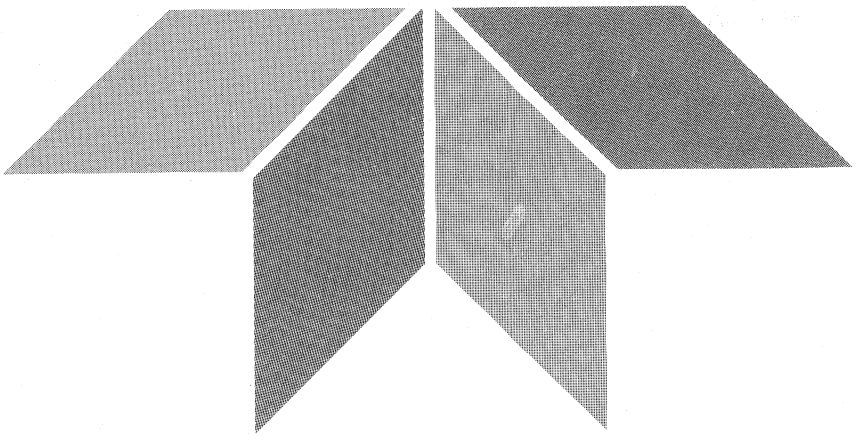
Applications Information

The TSC7212AM has two ground pins. These pins should be connected together.

Package Outline

40-Pin Plastic Dual-In-Line Package
P Package
(Package #17)





SECTION 11

Interface IC's

Section 11
Interface IC's 11-1

TSC450	Dual Power MOSFET Driver	11-3
TSC7660	DC to DC Voltage Converter	11-7
TSC9403	Serial Input/16-Bit Parallel Output Peripheral Driver	11-17
TSC9404	Serial Input/16-Bit Parallel Output Peripheral Driver	11-17

TSC450
Dual Power MOSFET Driver

General Description

The TSC450 is a low cost dual driver with TTL compatible inputs and high voltage outputs. Each device may be configured in an inverting or non-inverting configuration. The active pullup, high voltage outputs will drive power MOSFET gates.

The TSC450 also serves as a logic level translator and discrete analog switch driver.

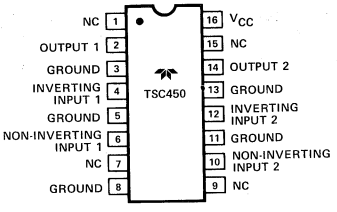
Features

- Dual Device for High Packing Density
- User Selectable Inverting or Non-Inverting Operation
- Single Supply Operation
- TTL Compatible Inputs
- High Output Sink Current ..... 12 mA
- High Output Source Current ..... 6 mA
- Fast Switching ..... 125 ns
- Available with Mil-STD-883B Processing

Ordering Information

Part No.	Supply Voltage	Temp. Range	Package
TSC450AIJE	15 V	-25°C to +85°C	16 Pin CerDIP
TSC450ACPE	15 V	0°C to +70°C	16 Pin Epoxy
TSC450BIJE	12 V	-25°C to +85°C	16 Pin CerDIP
TSC450BCPE	12 V	0°C to +70°C	16 Pin Epoxy
TSC450AMJE	15 V	-55°C to +125°C	16 Pin CerDIP
TSC450BMJE	12 V	-55°C to +125°C	16 Pin CerDIP
TSC450 AMJE/883	15 V	MIL-STD-883B Processing -55°C to +125°C	16 Pin CerDIP
TSC450 BMJE/883	12 V	MIL-STD-883B Processing -55°C to +125°C	16 Pin CerDIP

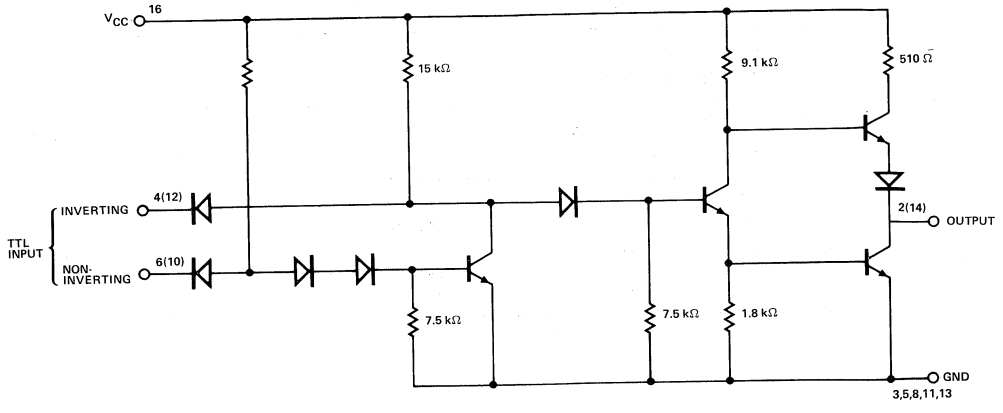
Pin Configuration



NC = No Connection

11

Functional Diagram (1/2 Circuit)



Absolute Maximum Ratings

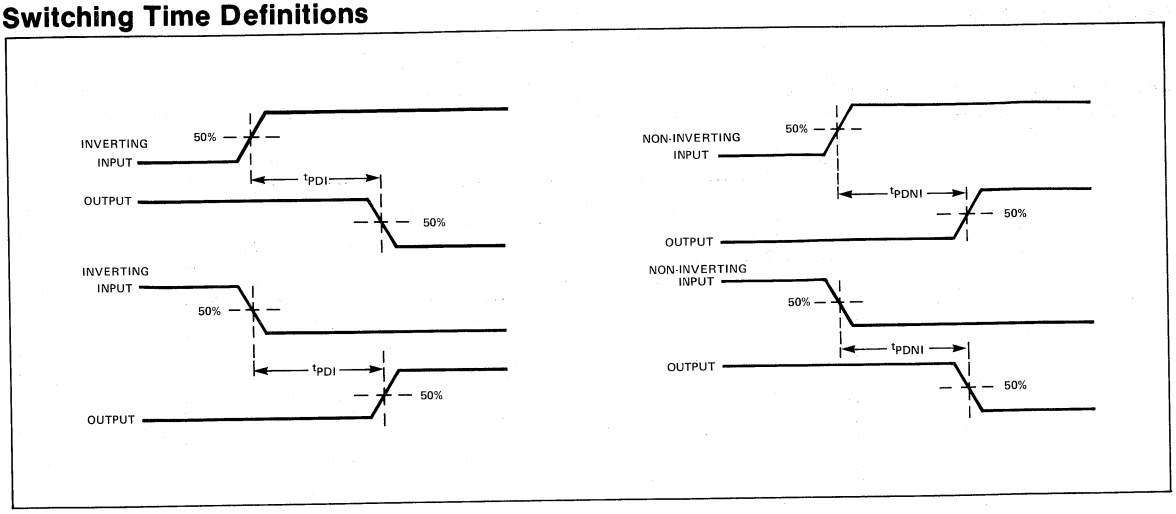
	J Package, CerDIP	P Package, Plastic
Storage Temperature	-65°C to +150°C	-55°C to +100°C
Lead Temperature (1/16 inch from case, 10 sec max)	300°C	300°C
Continuous Supply Voltage		
Type B Device	+15.0 V	+15.0 V
Type A Device	+16.5 V	+16.5 V
Pulsed Supply Voltage (less than 100 msec)	+18.0 V	+18.0 V
Input Voltage (any input)		
Type B Device	-0.5 to +15 V	-0.5 to +15 V
Type A Device	-0.5 to +18 V	-0.5 to +18 V
Surge Sink Current (less than 100 msec at $T_A = 25°C$)	20 mA	20 mA

Note: Exceeding the absolute maximum ratings may cause permanent damage. Operation at the absolute maximum ratings or beyond the conditions guaranteed is not implied.

Electrical Characteristics: Specifications apply over full operating temperature range. V_{CC} = +15 V for type A devices and V_{CC} = 12 V for type B devices unless otherwise indicated.

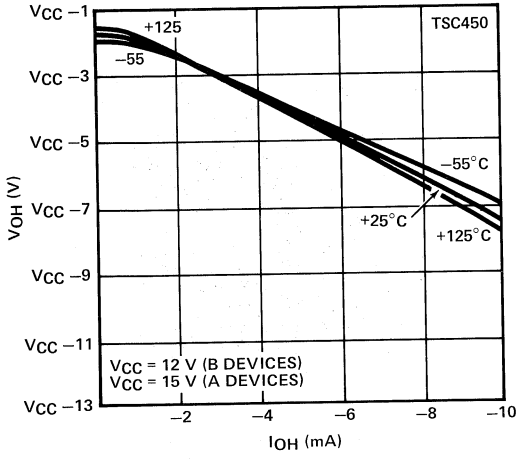
TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC450 MIN	TSC450 TYP	TSC450 MAX	UNIT
INPUT	1	V_{INH}	Input High Voltage	$I_{IN} \leq 40\ \mu A$	2.0	—	—	V
	2	V_{INL}	Input Low Voltage		—	—	0.8	V
	3	I_{INH}	Input High Current		—	—	10	μA
	4	I_{INL}	Input Low Current	$V_{IN} = 0.4$ V	—	—	1.6	mA
OUTPUT	5	V_{OHL}	Loaded Output High Voltage	$V_{CC} = 12$ V, $I_{OH} = 5$ mA (Type B Device)	6.0	—	—	V
	6	V_{OH}	Output High Voltage	$V_{CC} = 11$ V (Type B Device)	9.0	—	—	V
	7	V_{OHL}	Loaded Output High Voltage	$V_{CC} = 15$ V, $I_{OH} = 5$ mA (Type A Device)	9.0	—	—	V
	8	V_{OH}	Output High Voltage	$V_{CC} = 14$ V (Type A Device)	12.0	—	—	V
	9	V_{OL}	Output Low Voltage	$I_{OL} \leq 10$ mA	—	—	0.4	V
SYSTEM	10	t_{PDI}	Inverting Input to Output Propagation Delay		—	—	235	ns
	11	t_{PDNI}	Non-Inverting Input to Output Propagation Delay		—	—	125	ns
SUPPLY	12	I_{CC}	Supply Current	Type A Device $V_{CC} = 16$ V	—	—	13	mA
	13	I_{CC}	Supply Current	Type B Device $V_{CC} = 13$ V	—	—	10	mA

Switching Time Definitions

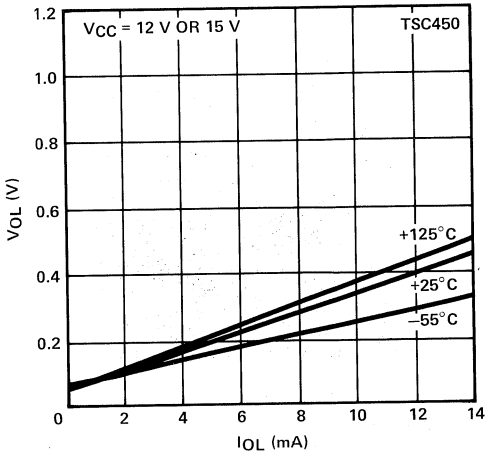


Operating Characteristics

Output High Voltage
TSC450



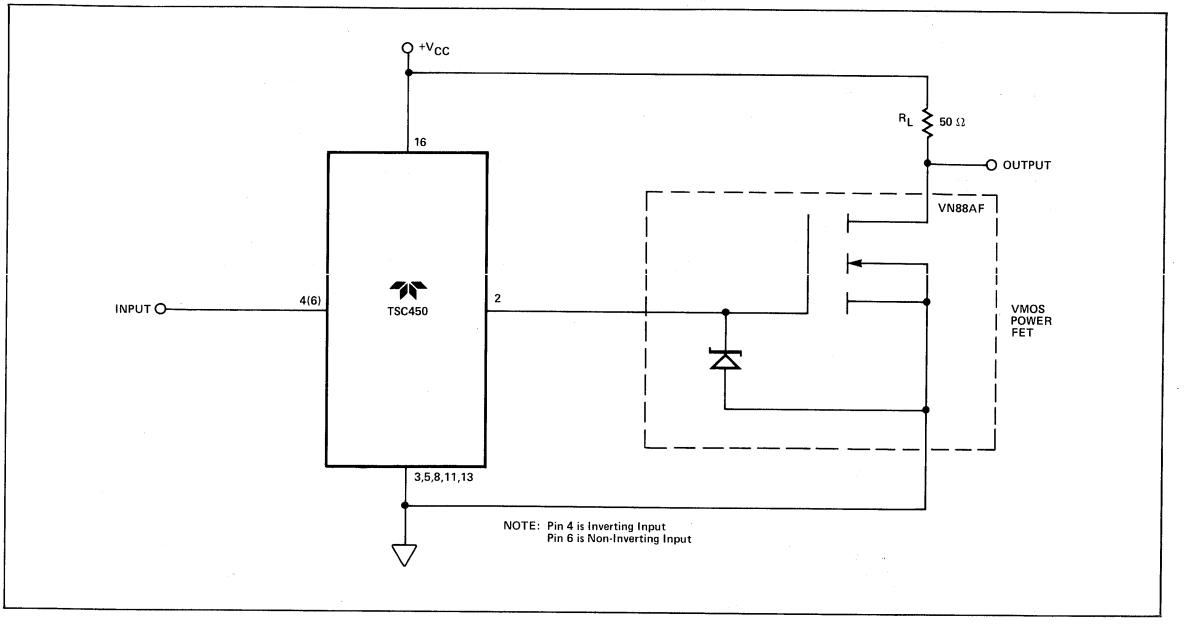
Output Low Voltage
TSC450



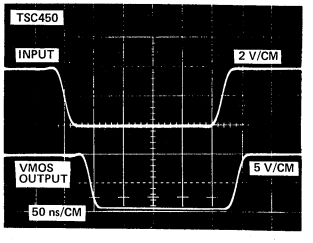
11

Application Information

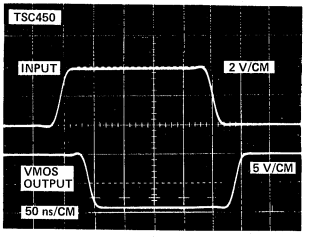
TSC450 Drives Power MOS FET



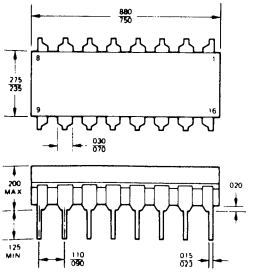
TSC450 Driving VMOS FET in Inverting Mode (Pin 4)



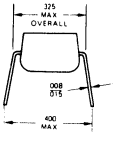
TSC450 Driving VMOS FET in Non-Inverting Mode (Pin 2)

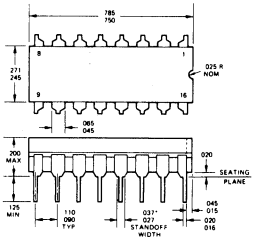


Package Outlines

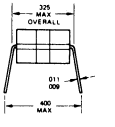


P Package
Epoxy DIP
(Package #8)





J Package
CerDIP
(Package #9)



ALL DIMENSIONS IN INCHES (MILLIMETERS)

Preliminary

TSC7660 DC to DC Voltage Converter

General Description

The TSC7660 DC to DC converter will generate a negative voltage from a positive source. With two external capacitors the TSC7660 will convert a 1.5 V to 10.0 V input signal to -1.5 V to -10.0 V level. The TSC7660 easily generates -5 V in +5 V digital systems.

Many analog to digital converters, digital to analog converters, operational amplifiers, and multiplexers require negative supply voltages. The TSC7660 allows +5 V digital logic systems to incorporate these analog components without adding an additional main power source. The TSC7660 can lower total system cost, ease engineering development and save space, power and weight.

The TSC7660 charges a capacitor to the applied supply voltage. Internal analog gates connect the capacitor across the output. Charge is transferred to an output storage capacitor completing the voltage conversion. Operation requires only two external capacitors for supply voltage <6.5 V.

Contained on-chip are a series DC power supply regulator, RC oscillator, voltage level translator, four output power MOS switches, and a unique logic element which senses the most negative voltage in the device and ensures that the output N-channel switches are not forward biased. This assures latch-up free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10 kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be overdriven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+3.5 to +10.0 volts), the LV pin is left floating to prevent device latchup.

Features

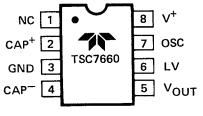
- Converts +5 V Logic Supply to ±5 V System
- Wide Input Voltage Range ..... 1.5 V to 10.0 V
- Efficient Voltage Conversion 99.9%
- Excellent Power Efficiency 98%
- Low Supply Current ..... 500 μA Max.
- Cascade for Output Voltage Multiplication
- Low Cost and Easy to Use
  - — Only 2 External Capacitors Required

Ordering Information

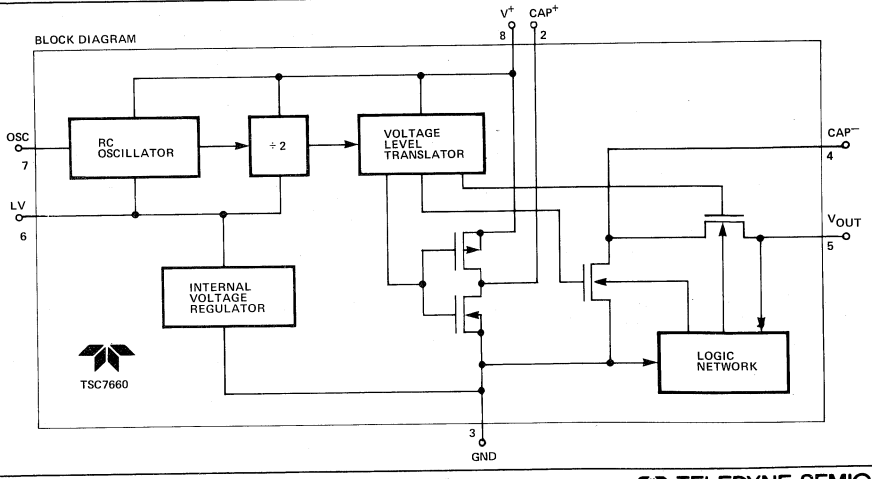
Part No.	Package	Temperature Range
TSC7660CPA	8-Pin Plastic Dip	0° C to +70° C
TSC7660IJA	8-Pin CerDIP	-40° C to +85° C
TSC7660MJA	8-Pin CerDIP	-55° C to +125° C
TSC7660/Y	Chip	25° C
Devices with MIL-STD-883 Processing		
TSC7660MJA/883	8-Pin CerDIP	-55° C to +125° C

The TSC7660 open circuit output voltage is equal to the input voltage to within 0.1%. The TSC7660 has a 98% power conversion efficiency for a 2 -5 mA load currents.

Pin Configuration



Block Diagram



Absolute Maximum Ratings

Supply Voltage ..... 10.5 V
LV and OSC Input Voltage
(Note 1) ..... -0.3 V to (V^+ +0.3 V) for V^+ < 5.5 V
(V^+ -5.5 V) to (V^+ +0.3 V) for V^+ > 5.5 V
Current into LV (Note 1) ..... 20 μA for V^+ > 3.5 V
Output Short Duration ($V_{SUPPLY} \leq 5.5$ V) .... Continuous
Power Dissipation (Note 2)
CerDIP Package ..... 500 mW
Plastic Package ..... 375 mW
Operating Temperature Range
TSC7660I ..... -40° C to +85° C
TSC7660M ..... -55° C to +125° C
TSC7660C ..... 0° C to 70° C
Storage Temperature Range ..... -65° C to 150° C
(Soldering, 10 sec.) ..... 300° C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

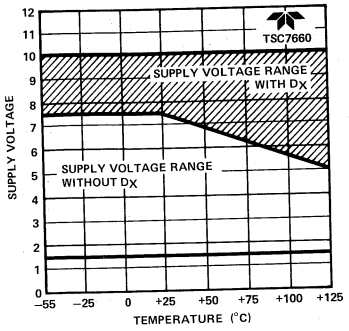
Operating Characteristics $V^+ = 5$ V, $T_A = 25°C$, $C_{OSC} = 0$, Test Circuit Figure 1 (unless otherwise specified)

NO.	SYMBOL	PARAMETER	CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
1	I^+	Supply Current	$R_L = \infty$	—	170	500	μA
2	V^+_{H1}	Supply Voltage Range - Hi	0° C ≤ T_A ≤ 70° C, R_L = 10 kΩ, LV Open	3.0	—	6.5	V
		(Dx Out of Circuit) (Note 3)	-55° C ≤ T_A ≤ 125° C, 10 kΩ, LV to GROUND	3.0	—	5.0	V
3	V^+_{L1}	Supply voltage Range - Lo (Dx Out of Circuit)	MIN ≤ T_A ≤ MAX, R_L = 10 kΩ, LV to GROUND	1.5	—	3.5	V
4	V^+_{H2}	Supply Voltage Range - Hi (Dx In Circuit)	MIN ≤ T_A ≤ MAX, R_L = 10 kΩ, LV Open	3.0	—	10.0	V
5	V^+_{L2}	Supply Voltage Range - Lo (Dx In Circuit)	MIN ≤ T_A ≤ MAX, R_L = 10 kΩ, LV to GROUND	1.5	—	3.5	V
6	R_{OUT}	Output Source Resistance	I_{OUT} = 20 mA, T_A = 25° C	—	55	100	Ω
			I_{OUT} = 20 mA, -40° C ≤ T_A ≤ +85° C [I Device]	—	—	130	Ω
			I_{OUT} = 20 mA, -20° C ≤ T_A ≤ +70° C [C Device]	—	—	120	Ω
			I_{OUT} = 20 mA, -55° C ≤ T_A ≤ +125° C (Note 3)	—	—	150	Ω
			V^+ = 2 V, I_{OUT} = 3 mA, LV to GROUND -20° C ≤ T_A ≤ +70° C	—	—	300	Ω
			V^+ = 2 V, I_{OUT} = 3 mA, LV to GROUND, -55° C ≤ T_A ≤ +125° C, Dx In Circuit (Note 3)	—	—	600	Ω
7	f_{OSC}	Oscillator Frequency		—	10	—	kHz
8	P_{EF}	Power Efficiency	R_L = 5 kΩ	95	98	—	%
9	$V_{OUT\ EF}$	Voltage Conversion Efficiency	$R_L = \infty$	97	99.9	—	%
10	Z_{OSC}	Oscillator Impedance	V^+ = 2 Volts	—	1.0	—	M Ω
			V^+ = 5 Volts	—	100	—	k Ω

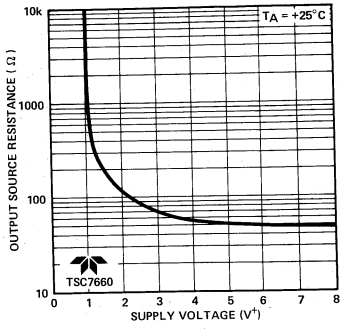
Notes:
1. Connecting any input terminal to voltages greater than C+ or less than GROUND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the TSC7660.
2. Derate linearly above 50° C by 5.5 mW/° C.
3. TSC7660M only.

Typical Performance Characteristics (Circuit of Figure 1)

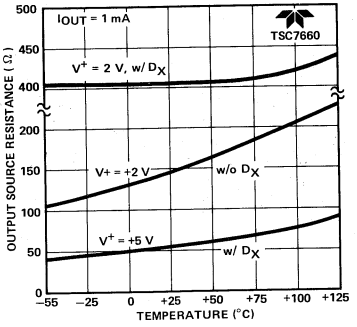
Operating Voltage as a Function of Temperature



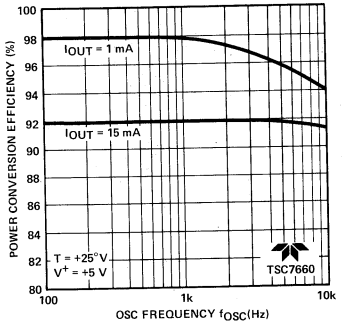
Output Source Resistance as a Function of Supply Voltage



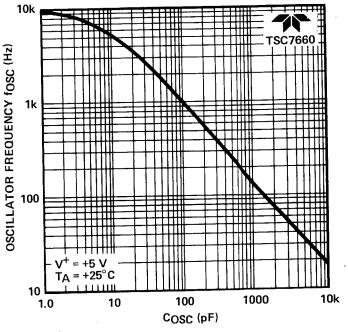
Output Source Resistance as a Function of Temperature



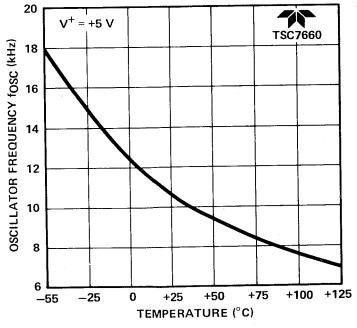
Power Conversion Efficiency as a Function of Osc. Frequency



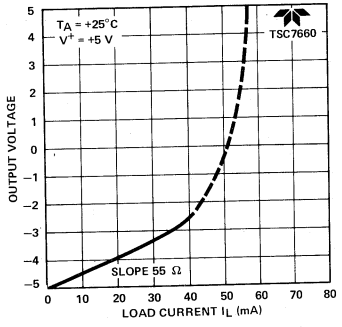
Frequency of Oscillation as a Function of External Osc. Capacitance



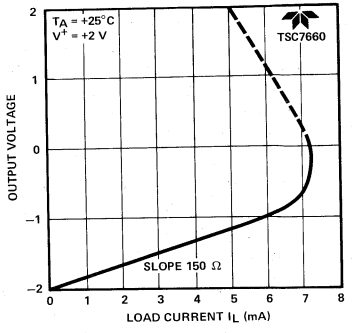
Unloaded Oscillator Frequency as a Function of Temperature



Output Voltage as a Function of Output Current



Output Voltage as a Function of Output Current

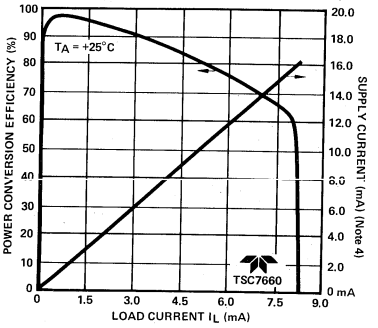


11

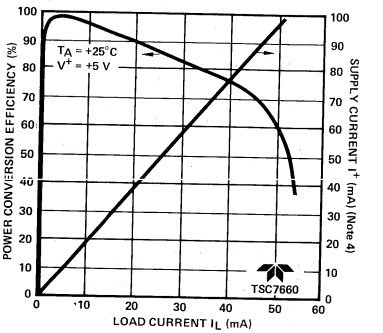
Typical Performance Characteristics (Circuit of Figure 1)

Note 4.
Note that the curves on the right include in the supply current that current fed directly into the load (R_L) from V^+ (see Figure 1). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the TSC7660, to the negative side of the load. Ideally, $V_{OUT} = 2\ V_{IN}$, $I_S \approx 2\ I_L$, so $V_{IN} \cdot I_S \approx V_{OUT} \cdot I_L$.

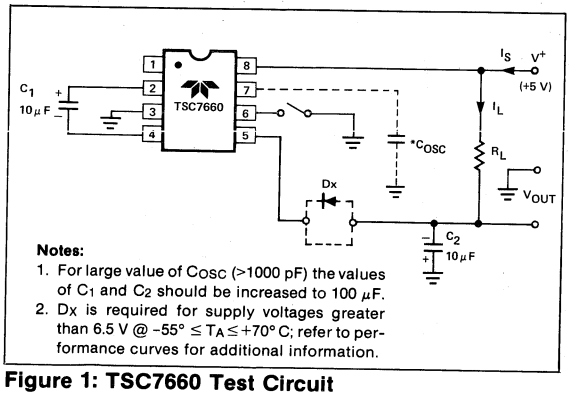
Supply Current & Power Conversion Efficiency as a Function of Load Current



Supply Current Power Conversion Efficiency as a Function of Load Current



Test Circuit



Notes:
1. For large value of Cosc (>1000 pF) the values of C_1 and C_2 should be increased to 100 µF.
2. Dx is required for supply voltages greater than 6.5 V @ $-55° \le T_A \le +70°$ C; refer to performance curves for additional information.

Figure 1: TSC7660 Test Circuit

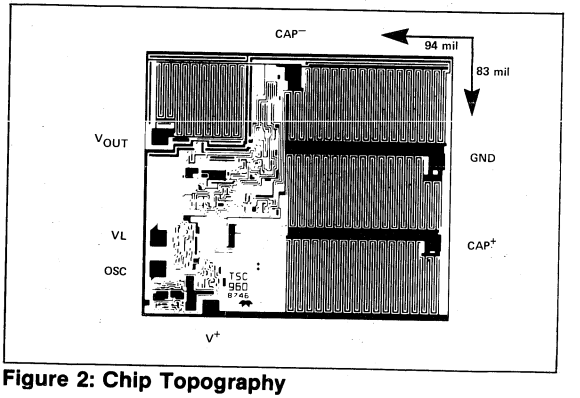


Figure 2: Chip Topography

Circuit Description

The TSC7660 contains all the necessary circuitry to complete a voltage doubler, with the exception of two external capacitors which may be inexpensive 10 µF polarized electrolytic capacitors. Operation is best understood by considering Figure 3, which shows an idealized voltage doubler. Capacitor C_1 is charged to a voltage, V^+, for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V^+, assuming ideal switches and no load on C_2.

The 4 switches in Figure 3 are MOS power switches; S_1 is a P-channel device and S_2, S_3 and S_4 are N-channel devices. The main difficulty with this approach is that in integrating

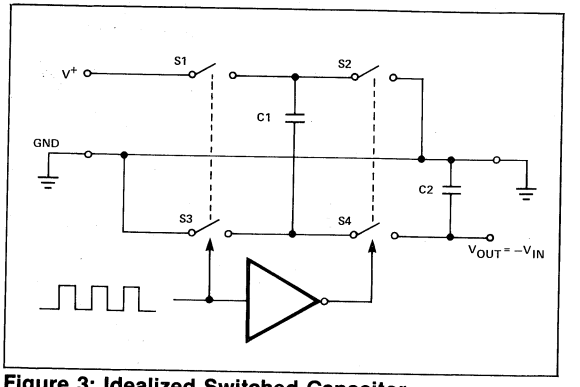


Figure 3: Idealized Switched Capacitor

the switches, the substrates of S_3 and S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit startup, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the TSC7660 by a logic network which senses the output voltage (V_{OUT}) together with the level translators and switches the substrates or S_3 and S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the TSC7660 is an integral part of the anti-latchup circuitry. It's inherent voltage drop can, however, degrade operation at low voltages. To improve low voltage operation the "LV" pin should be connected to GND, disabling the regulator. For supply voltages greater than 3.5 volts the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

Theoretical Power Efficiency Considerations

In theory a voltage multiplier can approach 100% efficiency if certain conditions are met:

- The drive circuitry consumes minimal power
- The output switches have extremely low ON resistance and virtually no offset.
- The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The TSC7660 approaches these conditions for negative voltage multiplication if large values of C_1 and C_2 are used. **Energy is lost only in the transfer of charge between capacitors if a change in voltage occurs.** The energy lost is defined by:

$$E = 1/2\ C_1\ (V_1^2 - V_2^2)$$

V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 3) compared to the value of R_L, there will be a substantial difference in the voltages V_1 and V_2. Therefore, it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

Do's And Don'ts

- Do not exceed maximum supply voltages.
- Do not connect LV terminal to GROUND for supply voltages greater than 3.5 volts.
- Do not short circuit the output to V^+ supply for supply voltages above 5.5 volts for extended periods, however, transient conditions including startup are okay.
- When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the TSC7660 and the + terminal of C_2 must be connected to GROUND.
- Add diode D_X as shown in Figure 1 for high-voltage, elevated temperature applications. A1N914 diode is suitable.

Considerations for High Voltage and Elevated Temperature

The TSC7660 will operate efficiently over its specified temperature range with only two external passive components (storage and pump capacitors), provided the operating supply voltage does not exceed 6.5 volts at +70° C and 5.0 volts at +125° C. Exceeding these maximums at the temperatures indicated may result in desctructive latch-up of the TSC7660 (Ref: Graph "Operating Voltage Vs. Temperature")

Operation at supply voltages of up to 10.0 volts over the full temperature range without danger of latch-up can be achieved by adding a general purpose diode in series with the TSC7660 output, as shown by "D_X" in the circuit diagrams. The effect of this diode on overall circuit performance is the reduction of output voltage by one diode drop (approximately 0.6 volts).

Typical Applications

Simple Negative Voltage Converter

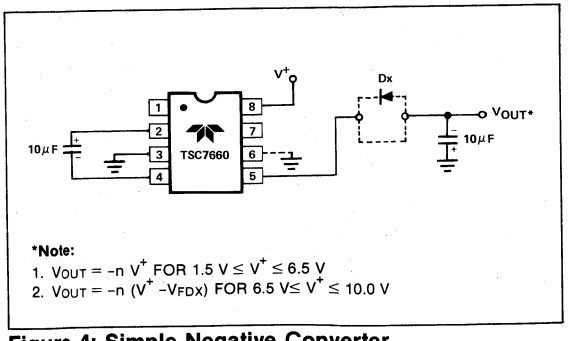
Figure 4 shows typical connections to provide a negative supply where a positive supply is available. A similar scheme may be employed for supply voltages anywhere in the operating range of +1.5 V to +10.0 V, keeping in mind that pin 6 (LV) is tied to the supply negative (GND) only for supply voltages below 3.5 volts, and that diode D_X must be included for proper operation at higher voltage and/or elevated temperatures.

The output characteristics of the circuit in Figure 4 are those of a nearly ideal voltage source in series with 70 ohms. Thus for a load current of −10 mA and a supply voltage of +5 volts, the output voltage would be −4.3 volts. The dynamic output impedance due to the capacitor impedances is approximately $1/\omega C$ where:

$$C = C_1 = C_2$$

$$\text{giving} \quad \frac{1}{\omega C} = \frac{1}{2\pi\ f_{OSC} \times 10^{-5}} = 3 \text{ ohms}$$

for $C = 10\ \mu F$ and $f_{OSC} = 5$ kHZ (1/2 of oscillator frequency)



*Note:
1. $V_{OUT} = -n\ V^+$ FOR $1.5\ V \le V^+ \le 6.5\ V$
2. $V_{OUT} = -n\ (V^+ - V_{FDX})$ FOR $6.5\ V \le V^+ \le 10.0\ V$

Figure 4: Simple Negative Converter

Paralleling Devices

Any number of TSC7660 voltage convertors may be paralleled to reduce output resistance. The reservoir capacitor, C_2, serves all devices while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately

$$R_{OUT} = \frac{R_{OUT} \text{ (of TSC7660)}}{n \text{ (number of devices)}}$$

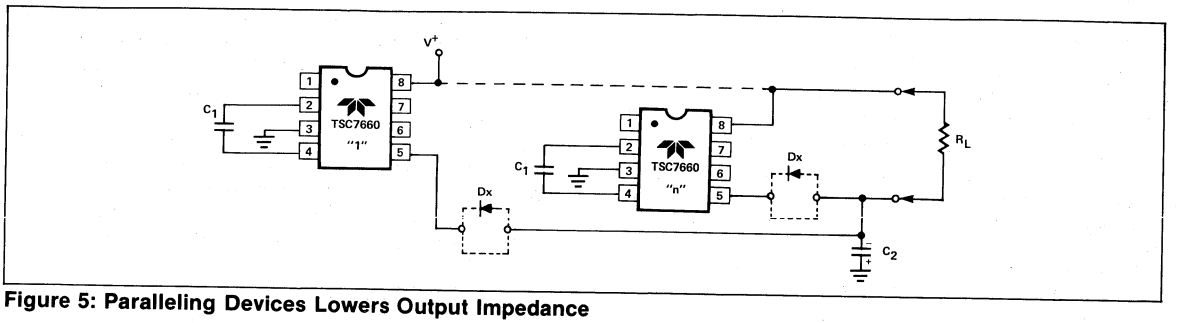


Figure 5: Paralleling Devices Lowers Output Impedance

Cascading Devices

The TSC7660 may be cascaded as shown to produce larger negative multiplication of the initial supply voltage, however, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n\ (V_{IN}),$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual TSC7660 R_{OUT} values.

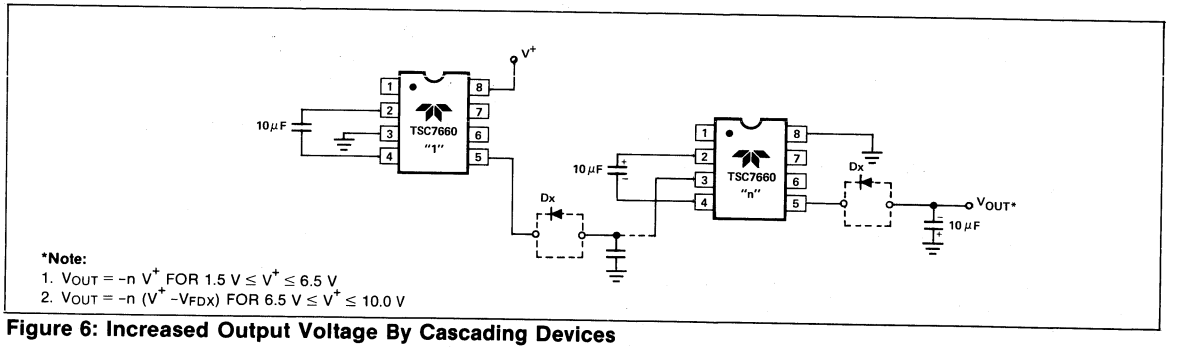


Figure 6: Increased Output Voltage By Cascading Devices

Changing the TSC7660 Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 7. In order to prevent possible device latchup, a 1 kΩ resistor must be used in series with the clock output. In the situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10 kΩ pullup resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

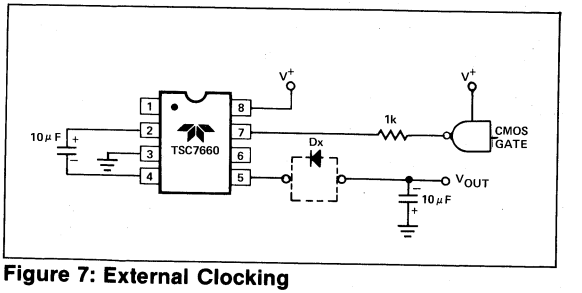


Figure 7: External Clocking

It is also possible to increase the conversion efficiency of the TSC7660 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is achieved by connecting an additional capacitor, C_{OSC}, as shown in Figure 8. Lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and the reservoir (C_2) capacitors. To overcome this increase the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100 pf capacitor between pin 7 (Osc) and V^+ will lower the oscillator frequency to 1 kHz from its nominal frequency of 10 kHz (a multiple of 10), and necessitate a corresponding increase in the value of C_1 and C_2 (from 10 μF to 100 μF).

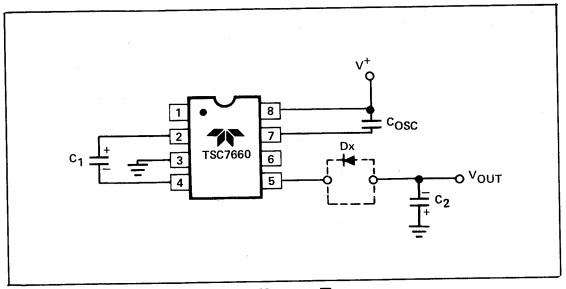


Figure 8: Lowering Oscillator Frequency

Positive Voltage Multiplication

The TSC7660 may be employed to achieve positive voltage multiplication using the circuit shown in Figure 9. In this application, the pump inverter switches of the TSC7660 are used to charge C_1 to a voltage level of $V^+ - V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V^+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes $(2\ V^+) - (2\ V_F)$ or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 5$ volts and an output current of 10 mA it will be approximately 60 ohms.

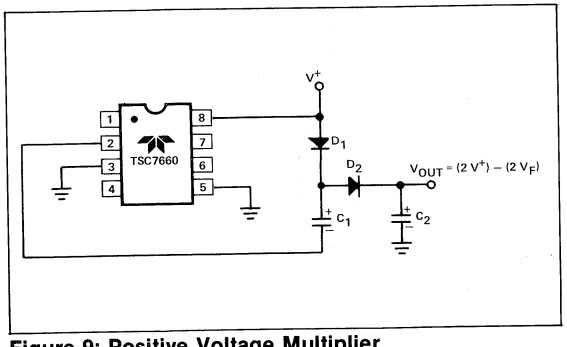


Figure 9: Positive Voltage Multiplier

Combined Negative Voltage Conversion and Positive Supply Multiplication

Figure 10 combines the functions shown in Figures 4 and 9 to provide negative voltage conversion and positive voltage multiplication simultaneously. This approach would be, for example, suitable for generating +9 volts and -5 volts from an existing +5 volt supply. In this instance capacitors C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir respectively for the multiplied positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

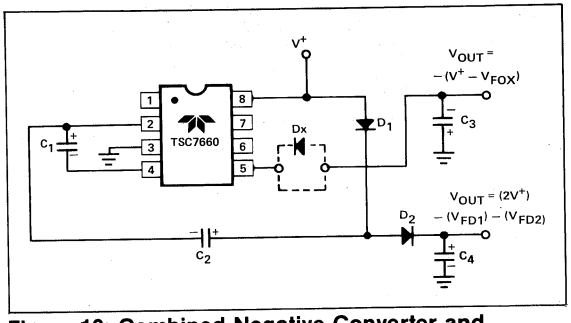


Figure 10: Combined Negative Converter and Positive Multiplier

Efficient Positive Voltage Multiplication/Conversion

Since the switches that allow the charge pumping operation are bidirectional, the charge transer can be performed backwards as easily as forwards. Figure 11 shows a TSC7660 transforming -5 V to +5 V (or +5 V to +10 V, etc.). The only problem here is that the internal clock and switch-drive section will not operate until some positive voltage has been generated. An initial inefficient pump, as shown in Figure 10, could be used to start this circuit up, after which it will bypass the other (D1 and D2 in Figure 10 would never turn on) or else the diode and resistor shown dotted in Figure 11 can be used to "force" the internal regulator on.

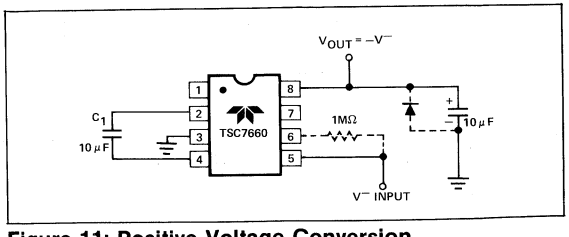


Figure 11: Positive Voltage Conversion

Voltage Splitting

The same bidirectional characteristics used in Figure 11 can also be used to split a higher supply in half, as shown in Figure 12. The combined load will be evenly shared between the two sides. Once again, a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 6, +15 V can be converted (via +7.5, and -7.5 V) to a nominal -15 V, though with rather high series resistance (~250 Ω).

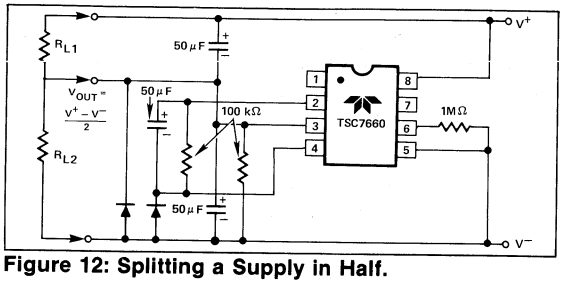


Figure 12: Splitting a Supply in Half.

Negative Voltage Generation for Display ADCs

The TSC7106 is designed to work from a 9 V battery. With fixed power supply system the TSC7106 will perform conversions with input signals referenced to power supply ground.

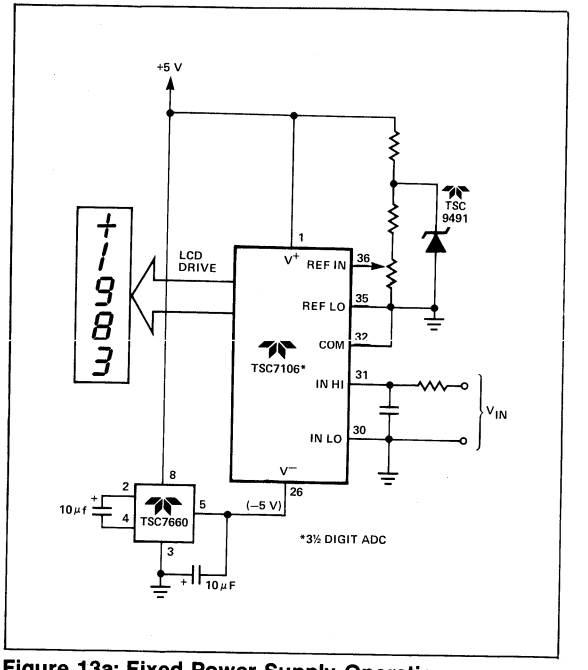


Figure 13a: Fixed Power Supply Operation of TSC7106 ADC.

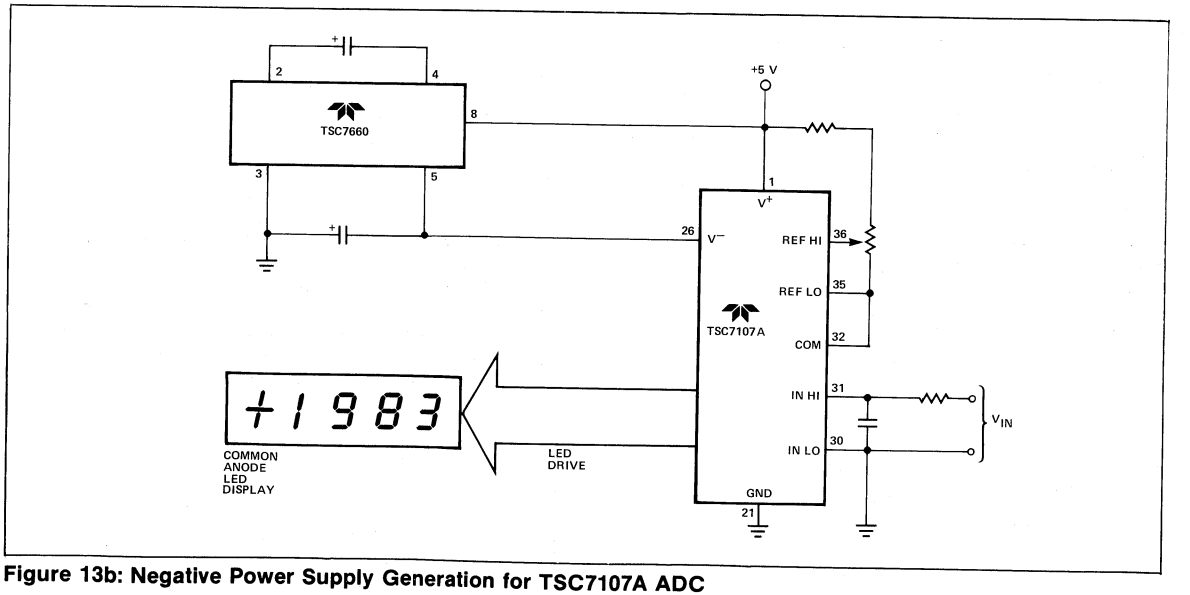


Figure 13b: Negative Power Supply Generation for TSC7107A ADC

Negative Supply Generation for 4 1/2 Digit Data Acquisition System

The TSC7136 is a 4 1/2 Digit ADC operating from ±5 V supplies. The TSC7660 inexpensively provides a -5 V source. see AN16 and AN17 for TSC7135 interface details and software routines.

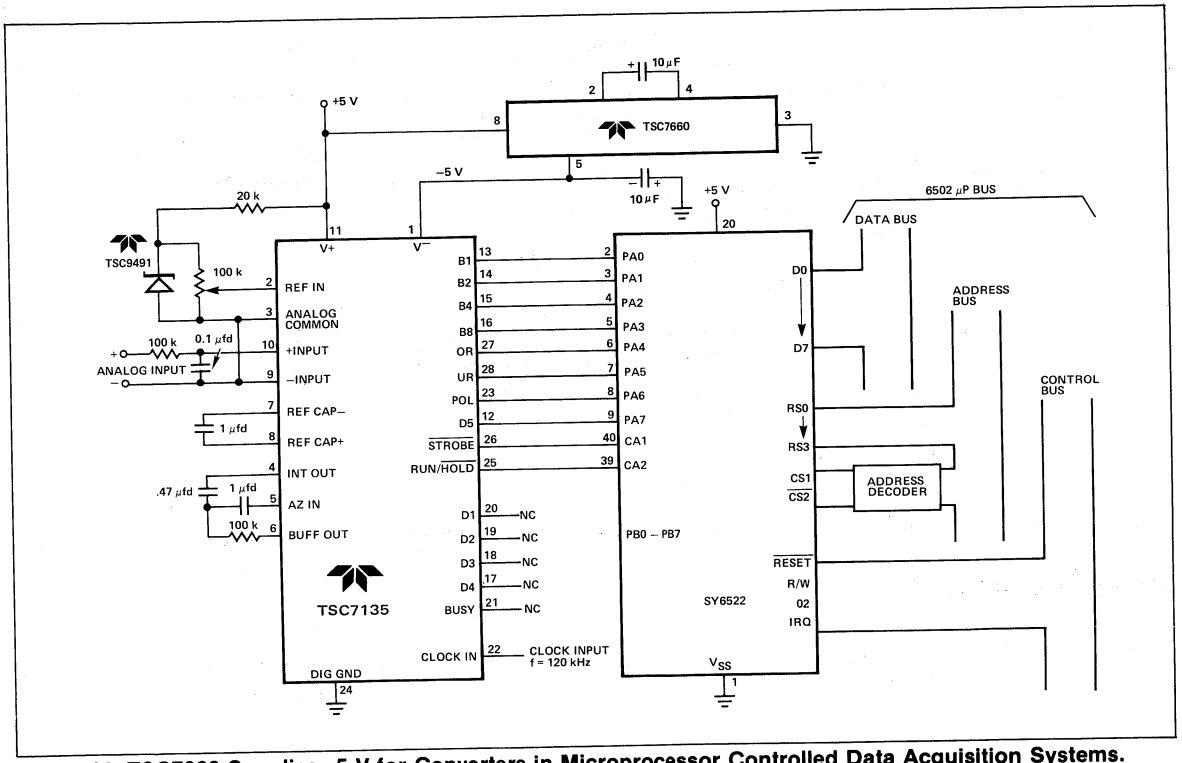


Figure 14: TSC7660 Supplies -5 V for Converters in Microprocessor Controlled Data Acquisition Systems.

Negative Supply Generation for TSC94XX Frequency to Voltage Converters.

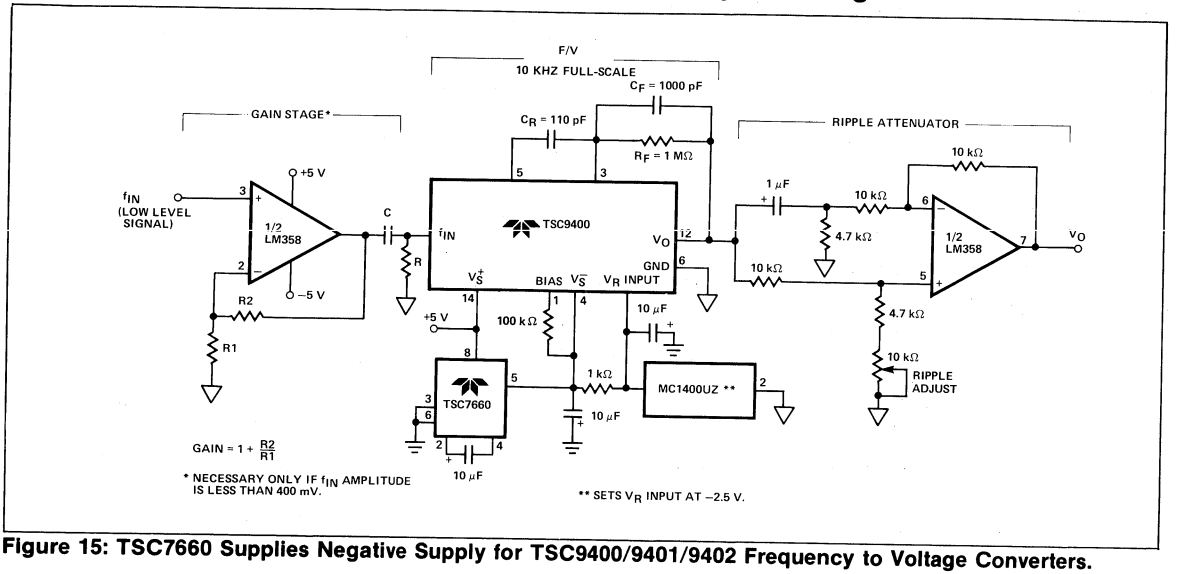
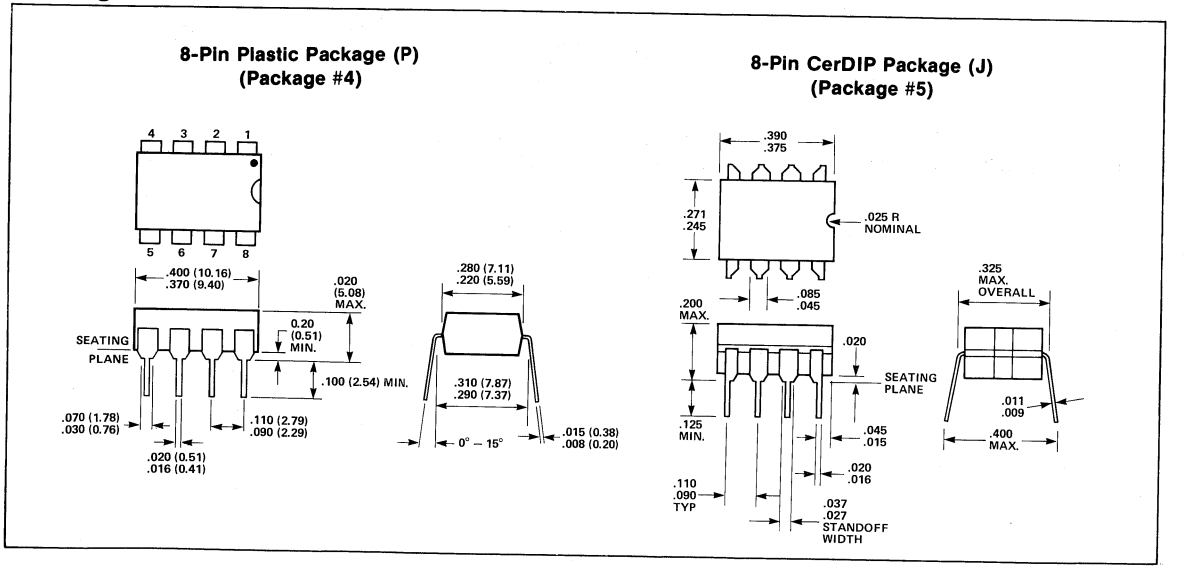


Figure 15: TSC7660 Supplies Negative Supply for TSC9400/9401/9402 Frequency to Voltage Converters.

Package Outline



TELEDYNE SEMICONDUCTOR

TSC9403
TSC9404
Serial Input/16-Bit Parallel Output Peripheral Driver
• High Voltage, High Current Outputs

General Description

The Teledyne Semiconductor TSC9403 and TSC9404 are serial input, 16-bit parallel output shift registers. High output power MOS switching transistors make the TSC9403 and TSC9404 ideal interface circuits between microprocessor I/O ports and high current/voltage peripherals. The CMOS construction limits quiescent power dissipation to 20 mW.

The TSC9403 common source, open drain MOS outputs sustain 20 V in the OFF state and maintain leakage currents under 100 μA. The TSC9404 outputs are rated at 15 V. The 16 parallel outputs will continuously sink 60 mA. ($V_{SAT} \leq 0.5$ V).

Successive connection of serial data outputs to serial data inputs make longer length serial to parallel conversions possible. Device cascading makes the TSC9403 and TSC9404 ideal thermal printhead or high resolution LED bar graph drivers.

Features

- High Voltage Outputs: 20 V (TSC9403), 15 V (TSC9404)
- High Output Current Sink Capability: 60 mA
- Low Standby Power: 20 mW
- High Speed Operation: 3.0 MHz
- 16 Parallel Outputs
- Cascading Possible for Longer Data Words

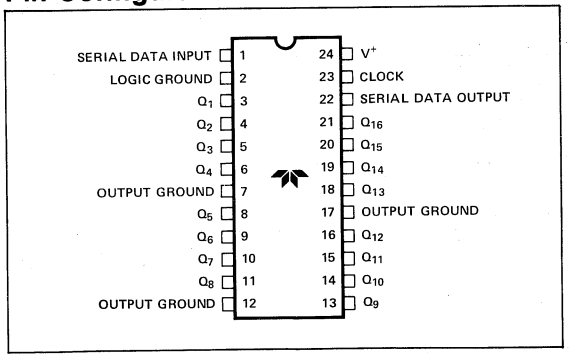
Applications

- Incandescent Lamp Driver
- Thermal Printhead Driver
- LED Bar Graph Driver
- High Current, Microprocessor Serial Port Expander
- Relay/Solenoid Driver
- Tungsten Lamp Driver
- SCR Gate Driver

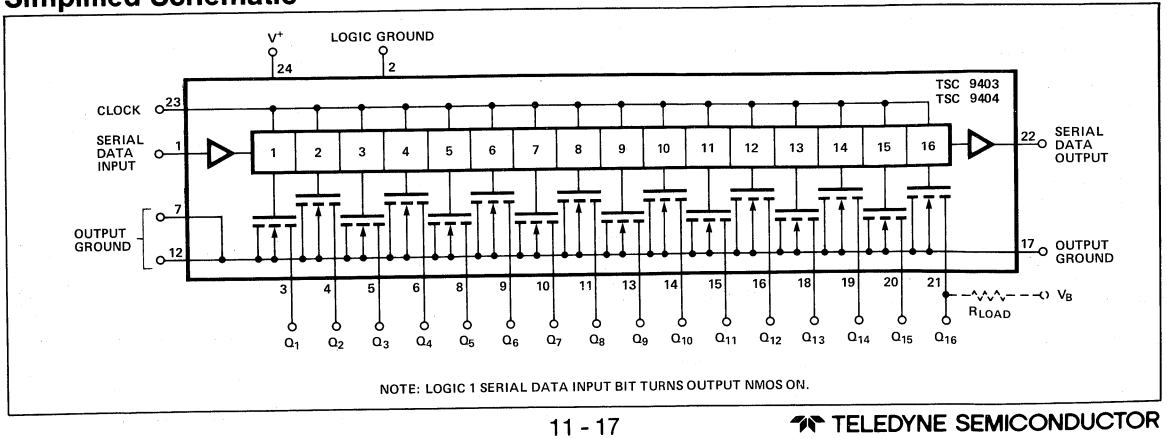
Ordering Information

Part	Package	Temperature Range	Output Voltage
TSC9403CJ	24-Pin Epoxy Dip	0°C to 70°C	20 V
TSC9403IL	24-Pin CerDIP	-25°C to 85°C	20 V
TSC9404CJ	24-Pin Epoxy Dip	0°C to 70°C	15 V
TSC9404IL	24-Pin CerDIP	-25°C to 85°C	15 V
TSC9404ML	24-Pin CerDIP	-55°C to 125°C	15 V
Devices Available with MIL-STD-883 Processing			
TSC9404ML/883	24-Pin CerDIP	-55°C to 125°C	15 V

Pin Configuration



Simplified Schematic



NOTE: LOGIC 1 SERIAL DATA INPUT BIT TURNS OUTPUT NMOS ON.

Absolute Maximum Ratings

Supply Voltage (V+ to Logic Ground) ..... 7.0 V
Digital Logic Input Voltage ..... 5.5 V
Parallel Output Drain Voltage ..... 22 V
Parallel Output Drain Current ..... 80 mA
Logic Ground to Output Ground
Potential Difference ..... 100 mV
Package Power Dissipation
CerDIP Package ..... 1 W @ 85° C
CerDIP Package ..... 0.4 W @ +125° C
Epoxy Package ..... 1 W @ 70° C
Operating Temperature
CerDIP Package (IL) ..... $-25° C \leq T_A \leq +85° C$
CerDIP Pacakge (ML) ..... $-55° C \leq T_A \leq +125° C$
Epoxy Package (CJ) ..... $0° C \leq T_A \leq +70° C$
Storage Temperature ..... $-65° C \leq T_A \leq +150° C$
Lead Temperature (Soldering, 60 Sec) ..... +300° C

Electrical Characteristics (V_S = 5.0 V, $0° C \leq T_A \leq +70° C$ for TSC9403CJ, TSC9404CJ and $-25° C \leq T_A +85° C$ for TSC9403IL, TSC9404IL, and -55° C to +125° C for TSC9404ML unless otherwise stated).

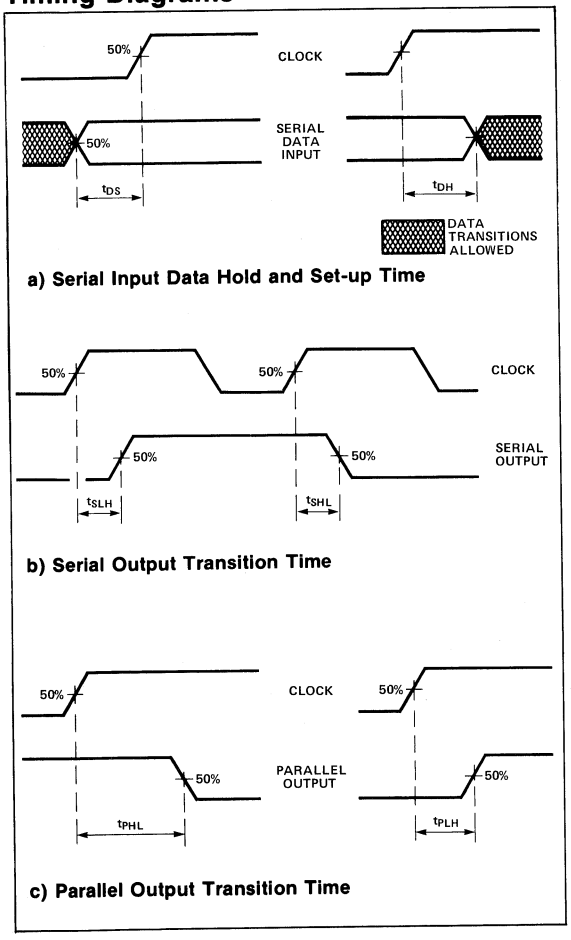
PARAMETER	SYMBOL	CONDITIONS	TSC9403/TSC9404 MIN	TYP	MAX	UNITS
Output ON Voltage	V_{SAT}	I_O = 60 mA V_S = 4.75 V	—	0.35	0.5	V
Output OFF Voltage	V_B	TSC9403	—	—	20	V
		TSC9404	—	—	15	V
Output Sink Current	I/O	$V_{SAT} \leq 0.5$ V (Note 1)	60	—	—	mA
Output Leakage Current	I_{OX}	V_S = 4.75 V V_B = 20 V (TSC9403) V_B = 15 V (TSC9404)	—	—	100	μA
Logic "1" Input Voltage	V_{INH}	V_S = 5.25 V	3.3	—	—	V
Logic "0" Input Voltage	V_{INL}	V_S = 5.25 V	—	—	0.8	V
Logic "1" Input Current	I_{INH}	V_S = 5.25 V	—	—	20	μA
Logic "0" Input Current	I_{INL}	V_{INL}= 0.4 V V_S = 5.25 V	—	—	400	μA
Input Capacitance	C_{IN}	V_{INL} = 0 V	—	15	—	pF
Serial Output Logic "1" Voltage	V_{OH}	I_{OH} = 400 μA I_{OH} = 10 μ A	2.4 4.5	— —	— —	V V
Serial Output Logic "0" Voltage	V_{OL}	I_{OL} = 5 mA	—	—	0.4	V
Serial Input Data Hold Time	t_{DH}		20	0	—	ns
Serial Input Data Set-up Time	t_{DS}		100	70	—	ns
Clock Frequency	t_{CP}		3	5	—	MHz
Clock Pulse Width	t_{PW}		150	100	—	ns
Parallel Output Low to High Transition Time	t_{PLH}	V_B = 20 V (TSC9403) V_B = 15 V (TSC9404) R_L = 330 Ω C_L = 25 pF	—	—	150	ns
Parallel Output High to Low Transition Time	t_{PHL}	V_B = 20 V (TSC9403) V_B = 15 V (TSC9404) R_L = 330Ω C_L = pF	—	—	200	ns
Serial Output Low to High Transition Time	t_{SLH}	I_{OH} = 400 μA C_L = 25 pF	—	—	150	ns

Electrical Characteristics (Cont.)

PARAMETER	SYMBOL	CONDITIONS	TSC9403/TSC9404 MIN	TYP	MAX	UNITS
Serial Output High to Low Transition Time	t_{SHL}	I_{OL} = 5 mA C_L = 25 pF	—	—	75	ns
Operating Supply Voltage	V_S		4.75	5.0	5.25	V
Quiescent Power Supply	I_S	V_S = 5.25 V f_C = 0 Hz V_{IHL} = 0 V I_O = 0 mA Pin 22 Open	—	1.0	4.0	mA

Note 1: Maintain Chip Temperature ≤ 150° C.

Timing Diagrams



Function Table

DATA INPUT D_N	CLOCK INPUT	PARALLEL OUTPUTS Q_1	Q_2	Q_3	... Q_{16}
X	L	$\overline{D_1}$	$\overline{D_2}$	$\overline{D_3}$	... $\overline{D_{16}}$
H	↓	L*	$\overline{D_1}$	$\overline{D_2}$	... $\overline{D_{15}}$
L	↓	H*	$\overline{D_1}$	$\overline{D_2}$	$\overline{D_{15}}$

L = Logic 0
H = Logic 1

L* = Output NMOS ON
H* = Output NMOS OFF

X = Don't Care

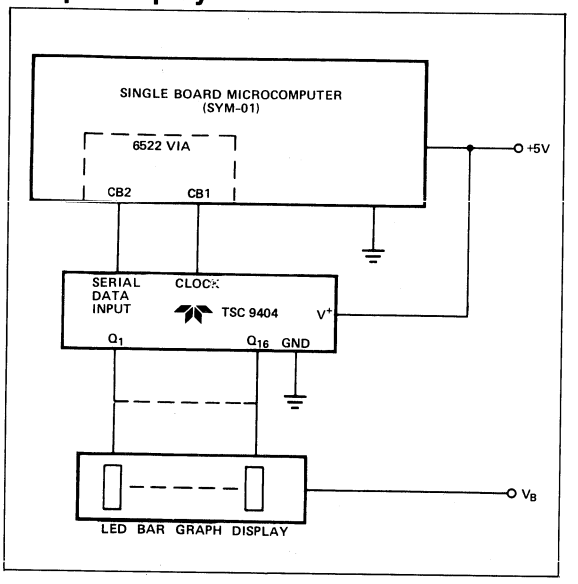
↓ = Transition from Low to High

D_1, D_2, ... D_{16} = Data Inputs at Clock Time T_{-N}.
Data is Inverted at the Parallel Outputs.

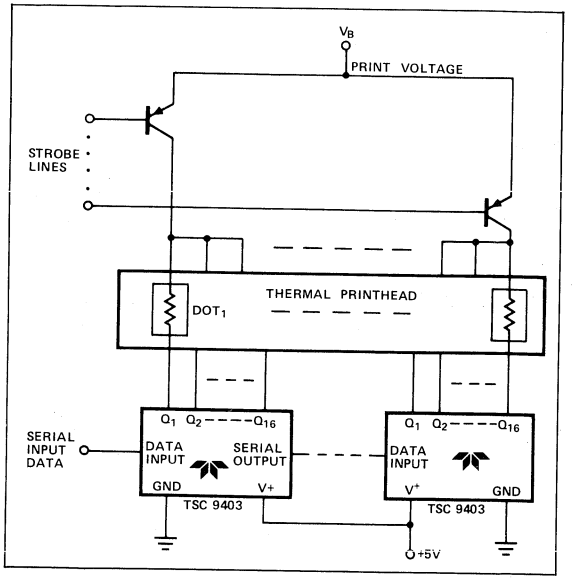
11

Applications

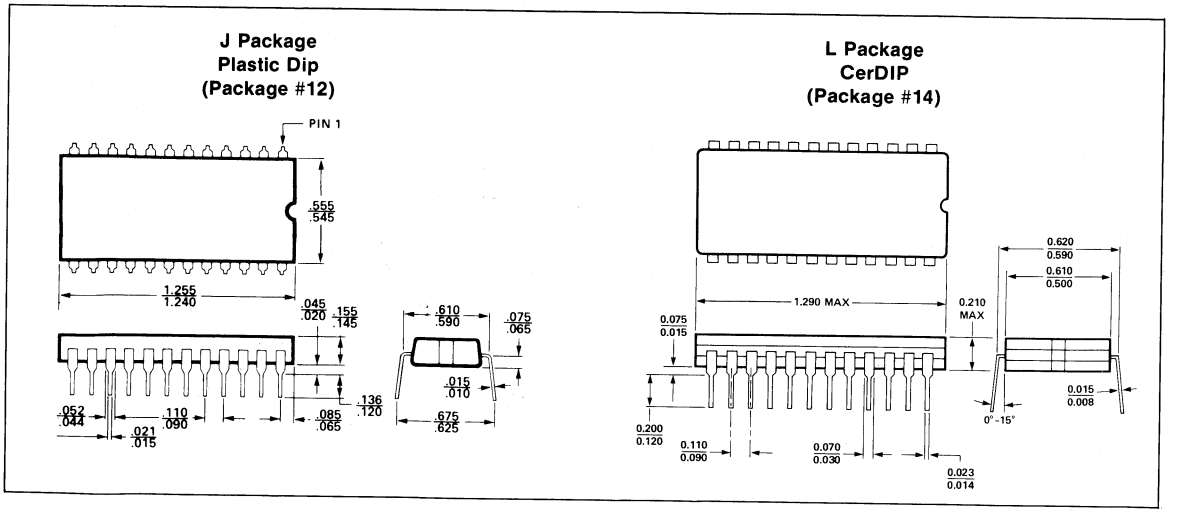
Microprocessor Controlled LED Bar Graph Display

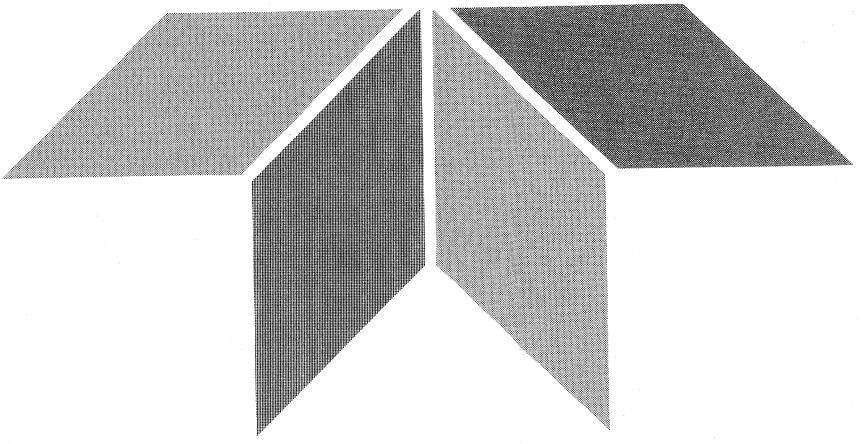


Thermal Printhead Driver



Package Outline





SECTION 12

References

Section 12
References 12-1

TSC9491	1.22 V Bandgap Reference	12-3
TSC9495	+5 V Bandgap Voltage Reference/Temperature Transducer	12-5
TSC9496	+10 V Bandgap Voltage Reference	12-9

TSC9491
1.22 V. Bandgap Reference

Features

- Guaranteed temperature coefficient: 50 or 100 ppm/°C
- Low bias current: 50μA
- Low breakdown voltage: 1.22V
- Low dynamic impedance 2Ω max.
- TO-18 or TO-92 package
- Low Cost

Applications

- Reference for A/D and D/A converters
- Threshold detectors
- Voltage Regulators
- VOM and VTVM's
- Amplifier biasing
- Battery operated equipment

General Description

The 9491 is a 1.22V temperature compensated voltage reference. It uses the band-gap principal to achieve extremely tight regulation over a wide range of operating currents. The use of thin film resistors assures long term stability and low noise.

Connection Diagram

Bottom Views

TO-18 TO-92

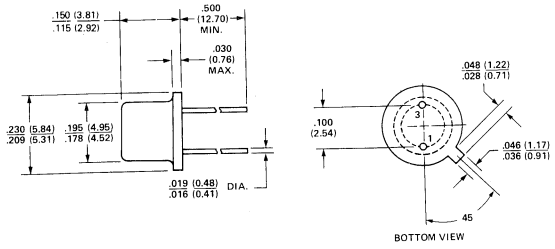
Ordering Information

	Temperature Range	
Temp. Coeff.	−55°C to +125°C (TO-18)	0°C to 70°C (TO-92)
50 ppm/°C	TSC9491AM	TSC9491AJ
100 ppm/°C	TSC9491BM	TSC9491BJ

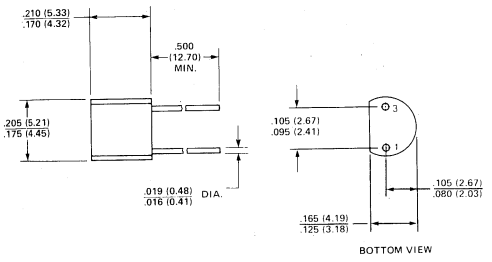
12

Packaging Information

TO-18
(2 PIN)



TO-92
(2 PIN)



All dimensions in inches (millimeters)

Absolute Maximum Ratings

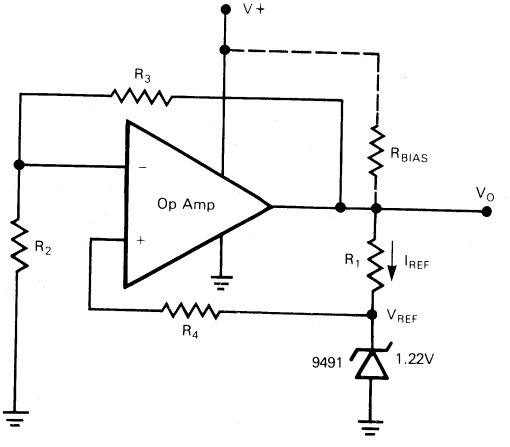
	TO-18	TO-92
Storage Temperature	−65°C to +200°C	−55°C to +150°C
Operating Temperature	−55°C to +125°C	0°C to +70°C
Forward Current, Max.	5mA	5mA
Reverse Current, Max.	1mA	1mA
Power Dissipation	Limited by max forward/reverse current	
Lead Temperature (Soldering, 10 seconds)	300°C	260°C

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Parameters		Min	Typ	Max	Units	Conditions
Reverse Breakdown Voltage	B_{VR}	1.20	1.22	1.25	V	I_R = 500μA
Reverse Breakdown Voltage Change	ΔB_{VR}	—	15	20	mV	50μA < I_R < 500μA
Temp. Coefficient TSC9491B	$\frac{\Delta B_{VR}}{\Delta T}$		.003	0.01	%/°C	I_R = 500μA
TSC9491A			.003	0.005		
Reverse Current	I_R	0.05	—		mA	

Applications/Design Circuits

Adjustable Voltage Reference



$$V_O = V_{REF}\left(\frac{R_2 + R_3}{R_2}\right)$$

$$I_{REF} = \frac{V_O - V_{REF}}{R_1}$$

$$R_4 = \frac{R_2 \cdot R_3}{R_2 + R_3}$$

TSC9495
+5 V Band Gap Voltage Reference

General Description

The TSC9495, Precision Voltage Reference, uses the band gap principle to generate an extremely stable 5 volt reference. Included in the TSC9495 are a band gap reference, an output amplifier and a voltage which varies linearily with temperature. The reference is ideal because of its low cost, low output noise and low power requirement. The TSC9495 is exceptionally stable over wide variations in temperature, line voltage and load current. The reference operates on a single supply with voltages of 7 volts to 40 volts.

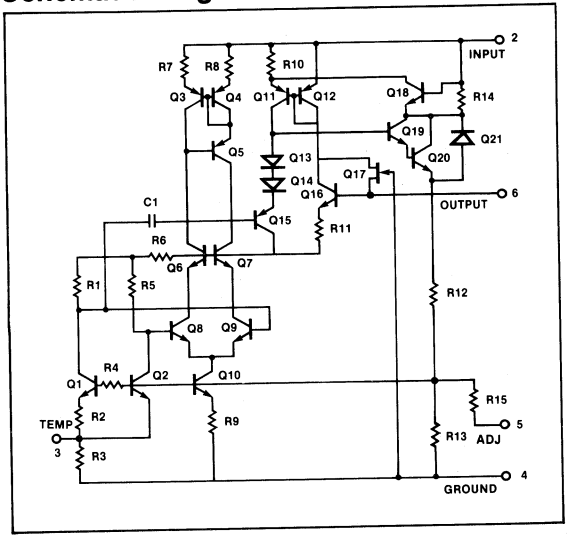
The TSC9495 is available with an initial accuracy of ±1%. An external potentiometer can be used to vary the output voltage ±6% with little effect on the temperature coefficient. The potentiometer can also be used to adjust the voltage for binary applications such as 5.12 volts.

Pin 3 of the TSC9495 has available a voltage which varies linearily with temperature. The typical change is 2.1 mv/° C. By using a buffer amplifier, the output voltage can be scaled to the desired resolution and range.

Ordering Information

Part No.	Package	Max. Voltage	Initial Accuracy	Temp. Range	Max. Temp Coefficient
TSC9495CJ	8-Pin Mini-Dip	30 V	1.0%	0 - 70° C	65 ppm

Schematic Diagram



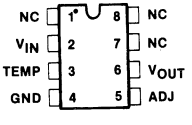
Features

- Excellent Temperature Stability: 20ppm/° C
- Tight Output Tolerance: 1%
- Adjustable Output
- Input Voltage Range: 7V to 40V
- Low Noise: 15 μVpp max.
- 10mA Output Current
- Short Circuit Proof
- Low Power: 1.4mA
- Temperature Output
- Replaces REF-02

Applications

- A/D Reference
- D/A Reference
- Current Source
- Transducer Reference
- Calibration Standard
- Thermometer

Pin Configuration

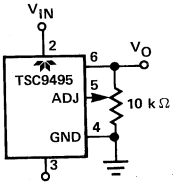


8 Pin Plastic Mini Dip

12

Output Adjustment

The output voltage of the TSC9495 can easily be adjusted by connecting a potentiometer to pin 5 as shown in the adjacent figure. Changing the output voltage does affect the overall temperature coefficient, however, this effect is small being typically only 0.7 ppm/° C per 100 mV of adjustment.



$V_{TEMP} \approx 2.1\ mV/^{o}C$

Absolute Maximum Ratings

Input Voltage . . . . . 30 V
Power Dissipation . . . . . 500 mW
Derating: Mini Dip, above 30°C ambient . . . . . 5.6mW/°C

Operating Temperature . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 60 sec.) . . . . . 300°C

Electrical Characteristics: These specifications apply for V_{IN} = +15 V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITION	TSC9495CJ MIN	TYP	MAX	UNITS
Output Voltage	V_O	I_L = 0 mA	4.950	5.000	5.050	V
Output Adjustment Range	ΔV_{trim}	R_p = 10 kΩ	±2.7	±6.0	-	%
Output Voltage Noise	e_{np-p}	0.1 Hz to 10 Hz	-	12	18	μVp-p
Input Voltage Range	V_{IN}		7	-	30	V
Line Regulation (Note 1)		V_{IN} = 8 to 30 V	-	0.009	0.015	5/V
Load Regulation (Note 1)		I_L = 0 to 8 mA	-	0.006	0.015	%/mA
Load Regulation (Note 1)		I_L = 0 to 4 mA	-	-	-	%/mA
Turn-on-Settling Time	t_{on}	To ±0.1% of final value	-	5.0	-	μsec
Quiescent Supply Current	I_{SY}	No Load	-	1.0	1.6	mA
Load Current	I_L		8	21	-	mA
Sink Current	I_S		-0.2	-0.5	-	mA
Short Circuit Current	I_{SC}	V_O = 0	-	30	-	mA
Temp Voltage Output	V_T	(Note 2)	-	630	-	mV
The following specifications apply for V_{IN} = =15 V, 0°C ≤ T_A ≤ = 70°C and I_L = 0mA, unless otherwise noted.						
Output Voltage Change with Temperature	ΔV_{OT}	(Note 3)	-	0.14	0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 4)	-	20	65	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10 kΩ	-	0.7	-	ppm/%
Line Regulation (Note 1)		V_{IN} = 8 to 30 V	-	0.011	0.018	%/V
Load Regulation (Note 1)		I_L = 0 to 5 mA	-	0.008	0.018	%/mA
Temp Voltage Output Temperature Coefficient	TCV_T	(Note 2)	-	2.1	-	mV/°C

Notes:

1. Line and Load Regulation specifications include the effects of self heating.
2. Limit current in or out of pin 3 to 50 nA and capacitance on pin 3 to 30 pF.
3. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5v:

$$\Delta V_{OT} = \frac{V_{MAX}\text{-}V_{MIN}}{5V} \times 100$$

4. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.

$$TCV_O = \frac{\Delta V_{OT}}{70°C}$$

Definitions

Line Regulation
The ratio of the change in output voltage to the change in line voltage producing it.

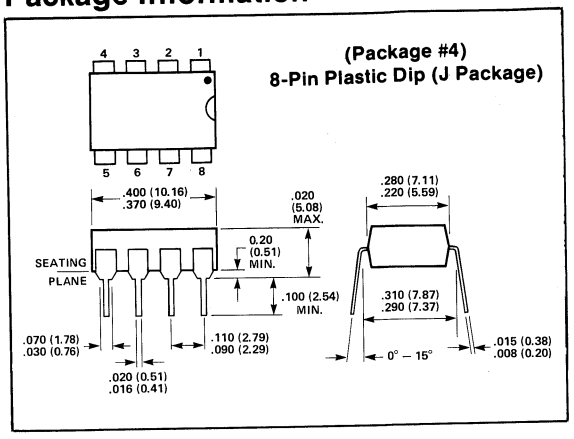
Load Regulation
The ratio of the change in output voltage to the change in load current producing it.

Quiescent Current (I_{SY})
The current required from the supply to operate the device with no load.

Output Voltage Noise (e_{np-p})
The peak to peak output noise voltage in a specified frequency band.

Output Turn-On Settling Time (t_{on})
The time required for the output voltage to reach its final value within a specified error band after application of V_{IN}.

Package Information



12

TSC9496
+10 V Band Gap Voltage Reference

General Description

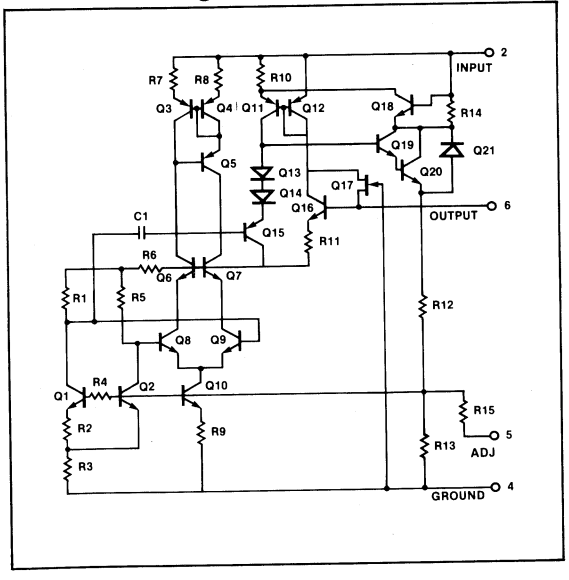
The TSC9496, Precision Voltage Reference, uses the band gap principle to generate an extremely stable 10 volt reference. Included in the TSC9496 are a band gap reference, and an output amplifier, which delivers 10mA of output current. The reference is ideal because of its low cost, low output noise and low power requirement. The TSC9496 is exceptionally stable over wide variations in temperature, line voltage and load current. The reference operates on a single supply with voltages of 12 volts to 40 volts.

The 9496 is available with an initial accuracy of ±1%. An external potentiometer can be used to vary the output voltage ±3% with little effect on the temperature coefficient. The potentiometer can also be used to adjust the voltage for binary applications such as 10.24 volts.

Ordering Information

Part No.	Package	Max. Voltage	Initial Accuracy	Temp. Range	Max. Temp Coefficient
TSC9496CJ	8-Pin Mini-Dip	30 V	1.0%	0 - 70° C	65 ppm

Schematic Diagram



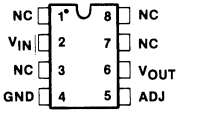
Features

- Excellent Temperature Stability: 20ppm/° C
- Tight Output Tolerance: 1%
- Adjustable Output
- Input Voltage Range: 12V to 40V
- Low Noise: 30 μVp-p max.
- 10mA Output Current
- Short Circuit Proof
- Low Power: 1.4mA
- Replaces REF-01

Applications

- A/D Reference
- D/A Reference
- Current Source
- Transducer Reference
- Calibration Standard

Pin Configuration

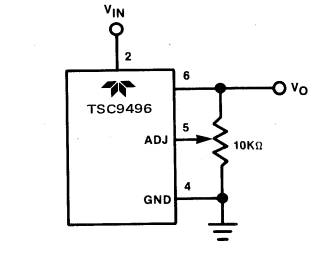


8 Pin Plastic Mini Dip

12

Output Adjustment

The output voltage of the TSC9496 can easily be adjusted by connecting a potentiometer to pin 5 as shown in the figure below. Changing the output voltage does affect the overall temperature coefficient, however, this effect is small being typically only 0.7 ppm/° C per 100 mV of adjustment.



Absolute Maximum Ratings

Input Voltage ..... 30 V
Power Dissipation ..... 500 mW
Derating: Mini Dip, above 30°C ambient ..... 5.6mW/°C

Operating Temperature ..... 0°C to 70°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 60 sec.) ..... 300°C

Electrical Characteristics: These specifications apply for V_{IN} = +15 V, T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITION	TSC9496CJ MIN	TYP	MAX	UNITS
Output Voltage	V_O	I_L = 0 mA	9.90	10.000	10.10	V
Output Adjustment Range	ΔV_{trim}	R_p = 10 kΩ	±2.7	±3.3	-	%
Output Voltage Noise	e_{np-p}	0.1 Hz to 10 Hz	-	25	35	μVp-p
Input Voltage Range	V_{IN}		12	-	30	V
Line Regulation (Note 1)		V_{IN} = 13 to 30 V	-	0.009	0.015	%/V
Load Regulation (Note 1)		I_L = 0 to 8 mA	-	0.006	0.015	%/mA
Load Regulation (Note 1)		I_L = 0 to 4 mA	-	0.006	0.015	%/mA
Turn-on-Settling Time	t_{on}	To ±0.1% of final value	-	5.0	-	μsec
Quiescent Supply Current	I_{SY}	No Load	-	1.0	1.6	mA
Load Current	I_L		8	21	-	mA
Sink Current	I_S		-0.2	-0.5	-	mA
Short Circuit Current	I_{SC}	V_O = 0	-	30	-	mA
The following specifications apply for V_{IN} = +15 V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted.						
Output Voltage Change with Temperature	ΔV_{OT}	(Note 3)	-	0.14	0.45	%
Output Voltage Temperature Coefficient	TCV_0	(Note 4)	-	20	65	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10 kΩ	-	0.7	-	ppm/%
Line Regulation (Note 1)		V_{IN} = 13 to 30 V	-	0.011	0.018	%/V
Load Regulation (Note 1)		I_L = 0 to 5 mA	-	0.008	0.018	%/mA

Notes:

1. Line and Load Regulation specifications include the effects of self heating.
2. TCV_O is defined as ΔV_{OT} divided by the temperature range, i.e.

$$TCV_O = \frac{\Delta V_{OT}}{70°C}$$

3. ΔV_{OT} is defined as the absolute difference between the maximum output voltage and minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \frac{V_{MAX} - V_{MIN}}{10V} \times 100$$

Definitions

Line Regulation
The ratio of the change in output voltage to the change in line voltage producing it.

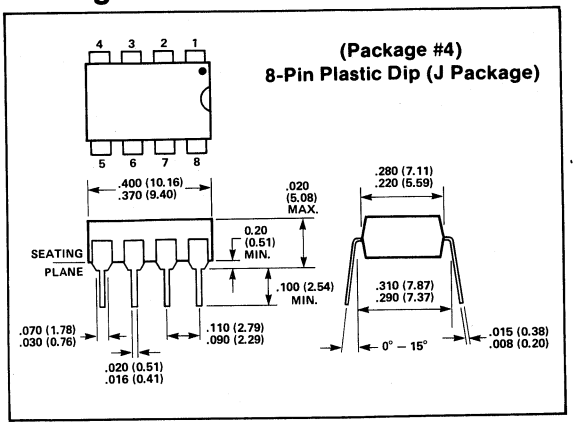
Load Regulation
The ratio of the change in output voltage to the change in load current producing it.

Quiescent Current (I_{SY})
The current required from the supply to operate the device with no load.

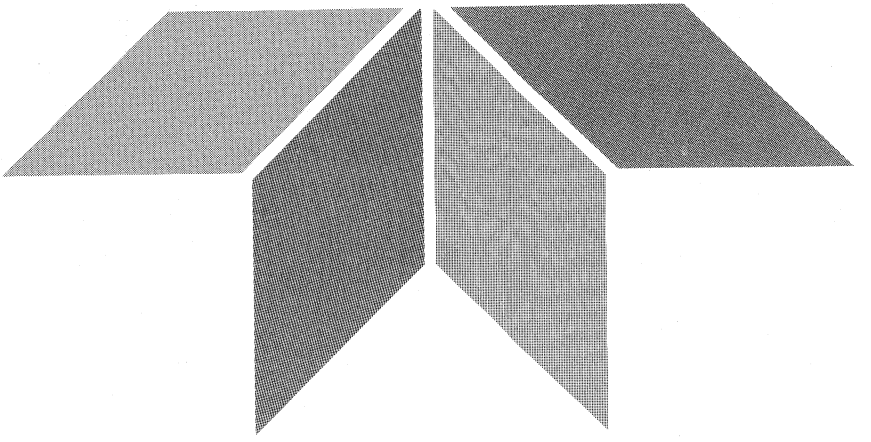
Output Voltage Noise (e_{np-p})
The peak to peak output noise voltage in a specified frequency band.

Output Turn-On Settling Time (t_{on})
The time required for the output voltage to reach its final value within a specified error band after application of V_{IN}.

Package Information



12



SECTION 13

Operational Amplifiers

Section 13
Operational Amplifiers 13-1

TSC7650 Precision Chopper - Stabilized Operational Amplifier 13-3

TELEDYNE SEMICONDUCTOR

Preliminary

TSC7650
Precision Chopper-Stabilized Operational Amplifier
• 0.7 μV Offset Voltage
• 50 nV/°C Offset Voltage Drift

General Description

The TSC7650 CMOS chopper-stabilized operational amplifier practically removes offset voltage error terms from system error calculations. The 5 μV maximum V_{OS} specification, for example, represents a fifteen times improvement over the industry standard OPO7E. The 50 nV/°C offset drift specification is over twenty-five times lower than the OPO7E. The increased performance eliminates V_{OS} trim procedures, periodic potentiometer adjustment and the reliability problems caused by damaged trimmers.

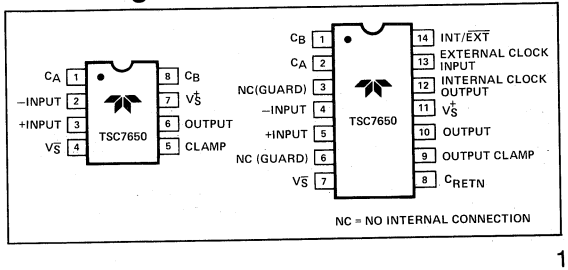
The TSC7650 performance advantages are achieved without the additional manufacturing complexity and cost incurred with laser or "zener zap" V_{OS} trim techniques. The TSC7650 is one of the lowest cost precision operational amplifiers available.

The TSC7650 nulling scheme corrects both dc V_{OS} errors and V_{OS} drift errors with temperature. A nulling amplifier alternately corrects its own V_{OS} errors and the main amplifier V_{OS} error. Offset nulling voltages are stored on two user supplied external capacitors. The capacitors connect to the internal amplifier V_{OS} null points. The main amplifier input signal is never switched. Switching spikes are not present at the TSC7650 output. The null scheme keeps V_{OS} errors low throughout the operating temperature range. Laser and "zener zap" trimming can correct for V_{OS} at only one temperature.

The nulling circuit oscillator and control circuits are integrated on chip. Only two external V_{OS} error storage capacitors are required. The TSC7650 operates as a conventional operational amplifier with vastly improved input specifications. The low V_{OS} and V_{OS} drift errors make the TSC7650 ideal for thermocouple, thermistor, and strain gauge applications. Low dc errors and high open loop gain make the TSC7650 an excellent preamplifier for precision analog to digital converters like the TSC7135 and TSC800.

The 14-pin dual in line package (DIP) has an external oscillator input to drive the nulling circuitry for optimum noise performance. Both the 8 and 14-pin DIP have an output voltage clamp circuit to minimize overload recovery time.

Pin Configuration



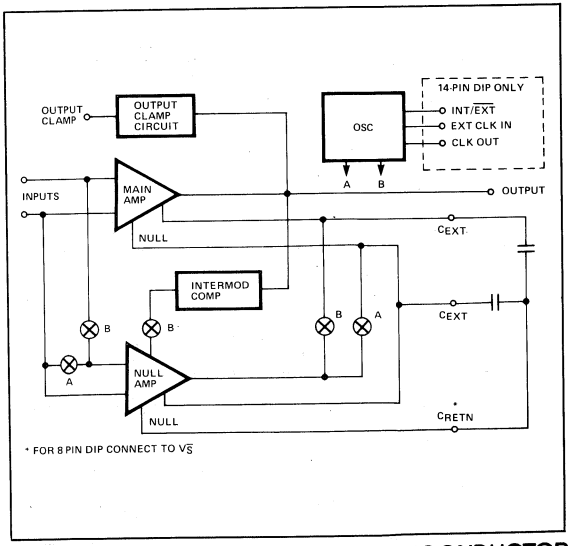
Features

- Low Input Offset Voltage ..... 0.7 μV
- Low Input Offset Voltage Drift ..... 0.05 μV/°C Max.
- Low Input Bias Current ..... 10 pA Max.
- High Impedance Differential CMOS Inputs ..... 10^{12} Ω
- High Open Loop Voltage Gain ..... 120 dB Min.
- Low Input Noise Voltage ..... 2.0 μVp-p
- High Slew Rate ..... 2.5 V/μs
- Low Power Operation ..... 20 mW
- Output Clamp Speeds Recovery Time
- Compensated Internally for Stable Unity Gain Operation
- Direct Replacement for ICL7650
- Available in 8-Pin Dip

Ordering Information

Part No.	Package	Temp. Range	Max. Offset Voltage
TSC7650CPA	8-Pin Plastic Dip	0°C to + 70°C	5 μV
TSC7650IJA	8-Pin CerDIP	-25°C to +85°C	5 μV
TSC7650CPD	14-Pin Plastic Dip	0°C to +70°C	5 μV
TSC7650IJD	14-Pin CerDIP	-25°C to +85°C	5 μV

Functional Diagram



13

Absolute Maximum Ratings

Total Supply Voltage (V_S^+ to V_S^-) ..... 18 Volts
Input Voltage ..... (V_S^+ + 0.3) to (V_S^- - 0.3) Volts
Storage Temp. Range ..... -55° C to 150° C
Lead Temperature (Soldering, 10 sec) ..... 300° C
Voltage on Oscillator Control Pins ..... V_S^+ to V_S^-
Output Short Circuit Duration ..... Indefinite
Current into Any Pin ..... 10 mA
While Operating (Note 4) ..... 100 μA
Operating Temp. Range
M Device ..... -55° C to +125° C
I Device ..... -25° C to +85° C
C Device ..... 0° C to +70° C
Package Power Dissipation (T_A = 25° C)
CerDIP Package ..... 500 mV
Plastic Package ..... 375 mW

Electrical Characteristics: V_S^+ = +5 V, V_S^- = -5 V, C_A = C_B = 0.1 μF. T_A = 25° C.

TYPE	NO.	SYMBOL	PARAMETER	TEST CONDITIONS	TSC7650 MIN	TYP	MAX	UNIT
INPUT	1	V_{OS}	Input Offset Voltage	T_A = +25° C	—	± 0.7	± 5.0	μV
				Over Operating Temp. Range (Note 1)	—	± 1.0	—	
	2	$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Average Temp. Coefficient	Operating Temp Range (Note 1)	—	0.01	0.05	μV/° C
	3		Offset Voltage vs Time		—	100	—	$\frac{nV}{\sqrt{month}}$
	4	I_{BIAS}	Input Bias Current	T_A = + 25° C	—	1.5	10	pA
				0° C ≤ T_A ≤ + 70° C	—	35	150	
				-25° C ≤ T_A ≤ + 85° C	—	100	400	
	5	I_{OS}	Input Offset Current	T_A = 25° C	—	0.5	—	pA
	6	e_{np-p}	Input Noise Voltage	R_S = 100 Ω 0 to 10 Hz	—	2	—	μV_{p-p}
	7	i_n	Input Noise Current	f = 10 Hz	—	0.01	—	pA/√Hz
	8	R_{IN}	Input Resistance		—	10^{12}		Ω
	9	CMVR	Common-Mode Voltage Range		-5.0	-5.2 to +2.0	+1.5 V	V
	10	CMRR	Common-Mode Rejection Ratio	CMVR = -5 V to +1. 5 V	120	130	—	dB
OUTPUT	11	A_V	Large-Signal Voltage Gain	R_L = 10 kΩ	120	130	—	dB
	12	V_{OUT}	Output Voltage Swing (Note 3)	R_L = 10 kΩ	± 4.7	± 4.85	—	V
				R_L = 100 kΩ	—	± 4.95	—	
	13		Clamp ON Current (Note 2)	R_L = 100 kΩ	25	70	200	μA
	14		Clamp OFF Current (Note 2)	-4.0 V < V_{OUT} < + 4.0 V	—	1	—	pA
DYNAMIC	15	B_W	Unity Gain Bandwidth	Unity Gain (+1)	—	2.0	—	MHz
	16	S_R	Slew Rate	C_L = 50 pF, R_L = 10 k	—	2.5	—	V/μs
	17	t_r	Rise Time		—	0.2	—	μs
	18		Overshoot		—	20	—	%
	19	f_{ch}	Internal Chopping Frequency	Pins 12-14 Open (DIP)	120	200	375	Hz
SUPPLY	20	V_S^+ to V_S^-	Operating Supply Range		4.5	—	16	V
	21	I_S	Supply Current	No Load	—	2.0	3.5	mA
	22	PSRR	Power Supply Rejection Ratio	V_S = ± 3 V to ± 8 V	120	130	—	dB

Notes:
1. Operating temperature range is -25° C to +85° C for "I" grade and 0° C to +70° C for "C" grade.
2. See OUTPUT CLAMP discussion.
3. OUTPUT CLAMP not connected. See characteristic curves for output swing vs clamp current.
4. Limiting input current to 100 μA is recommended to avoid latch-up problems.
5. Static Sensitive Device. Unused devices must be stored in conductive material to protect devices from possible static damage.
6. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Theory of Operation

Figure 1 shows the major elements of the TSC7650. There are two amplifiers, the main amplifier and the nulling amplifier; both have offset-null capability. The main amplifier is connected full-time from the input to the output. The nulling amplifier, under the control of the chopping frequency oscillator and clock circuit, alternately nulls itself and the main amplifier. Two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power-supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A_{VOL}.

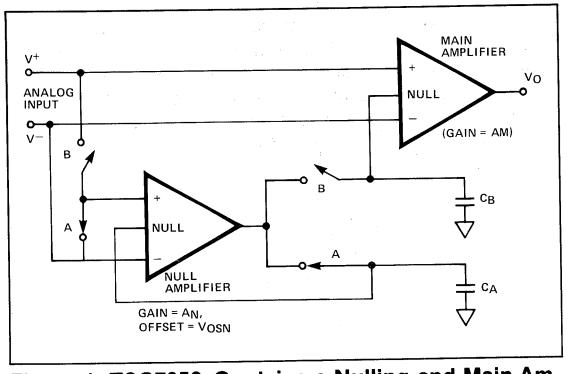


Figure 1: TSC7650 Contains a Nulling and Main Amplifier. Offset Correction Voltages are Stored on Two External Capacitors.

Careful balancing of the input switches minimizes chopper frequency charge injection at the input terminals, and the feed forward-type injection into the compensation capacitor that can cause output spikes in this type of circuit.

The circuits offset voltage compensation is easily shown. With the nulling inputs shorted a voltage almost identical to the nulling amplifier offset voltage is stored on C_A. The effective offset voltage at the null amplifier input is:

$$(1)\quad V_{OSE} = \frac{1}{A_N + 1} V_{OSN}$$

After the nulling amplifier is zeroed the main amplifier is zeroed; the A switches open and B switches close.

The output voltage equation is:

$$(2)\quad V_O = A_M \left[V_{OSM} + (V^+ - V^-) + A_N(V^+ - V^-) + A_N V_{OSE} \right]$$

Substituting (1) ➤(2) and assuming $A_N >> 1$.

$$(3)\quad V_O = A_M A_N \left[(V^+ - V^-) + \frac{V_{OSM} + V_{OSN}}{A_N} \right]$$

As desired the device offset voltages are reduced by the high open-loop gain of the nulling amplifier.

Output Stage/Load Driving

The output circuit is a high-impedance stage (approximately 18 kΩ). With loads less than this the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17 dB lower with a 1 kΩ load than with a 10 kΩ load. If the amplifier is used strictly for dc the lower gain is of little consequence since the dc gain is typically greater than 120 dB even with a 1 kΩ load. In wideband applications, the best frequency response will be achieved with a load resistor of 10 kΩ or higher. This will result in a smooth 6 dB/octave response from 0.1 Hz to 2 MHz, with phase shifts of less than 10° in the transition region where the main amplifier takes over from the null amplifier. The clock frequency sets the transition region.

Intermodulation

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite ac gain of the amplifier results in a small ac signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs. frequency characteristics near the chopping frequency. These effects are substantially reduced in the TSC7650 by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to a finite ac gain. The intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

Nulling Capacitor Connection

The offset voltage correction capacitors are connected to C_A and C_B. The common capacitor connection is made to V_S^- (Pin 4) on the 8-pin packages and to capacitor return (C_R, Pin 8) on the 14-pin packages. The common connection should be made through either a separate pc trace or wire to avoid voltage drops. The capacitors outside foil, if possible, should be connected to C_R or V_S^-.

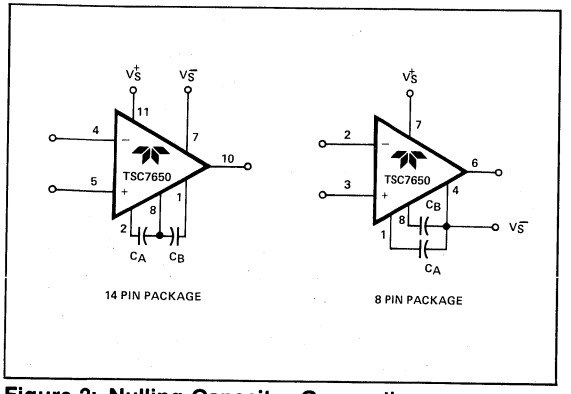


Figure 2: Nulling Capacitor Connection

Clock Operation

The internal oscillator is set for a 200 Hz nominal chopping frequency on both the 8 and 14-pin dual in line packages. With the 14-pin DIP TSC7650, the 200 Hz internal chopping frequency is available at the internal clock output (Pin 12). A 400 Hz nominal signal will be present at the external clock input pin (Pin 13) with $\overline{EXT}$/INT high or open. This is the internal clock signal before a divide by two operation.

The 14-pin DIP device can be driven by an external clock. Offset voltage and noise characteristics vs chopping frequency are shown in the typical operating characteristic curves. The INT/$\overline{EXT}$ input (Pin 14) has an internal pull-up and maybe left open for internal clock operation. If an external clock is used INT/$\overline{EXT}$ must be tied to V_S^- (Pin 7) to disable the internal clock. The external clock signal is applied to the external clock input (Pin 13).

The external clock amplitude should swing between V_S^+ and ground for power supplies up to ± 6 V and between V^+ and V^+ -6 V for higher supply voltages.

At low frequencies the external clock duty cycle is not critical since an internal divide by two gives the desired 50% switching duty cycle. The offset storage correction capacitors are charged only when the external clock input is high. A 50-80% external clock positive duty cycle is desired for frequencies above 500 Hz to guarantee transients settle before the internal switches open.

The external clock input can also be used as a strobe input. If a strobe signal is connected at the external clock input so that it is low during the time an overload signal is applied, neither capacitor will be charged. The leakage currents at the capacitor pins are very low. At 25° C a typical TSC7650 will drift less than 10 μV/sec.

Output Clamp

Chopper-stabilized systems can show long recovery times from overloads. If the output is driven to either supply rail, output saturation occurs. The inputs are no longer held at a "virtual ground." The V_{OS} null circuit treats the differential signal as an offset and tries to correct it by charging the external capacitors. The nulling circuit also saturates. Once the input signal returns to normal, the response time is lengthened by the long recovery time of the nulling amplifier and external capacitors.

Through an external clamp connection, the TSC7650 eliminates the overload recovery problem by reducing the feedback network gain before the output voltage reaches either supply rail.

The output clamp circuit is shown in Figure 3 with typical inverting and non-inverting circuit connections shown in Figure 4 and 5. Output voltage vs clamp circuit current characteristics are shown in the typical operating curves. For the clamp to be fully effective, the impedance across the clamp output should be greater than 100 kΩ.

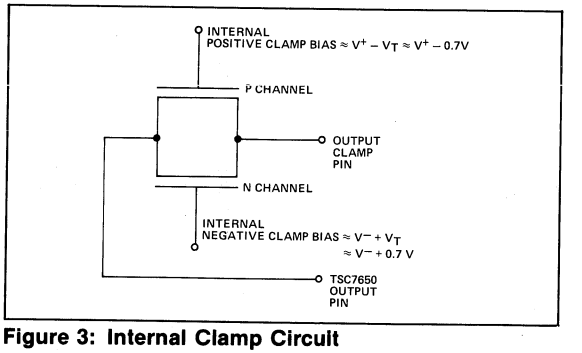


Figure 3: Internal Clamp Circuit

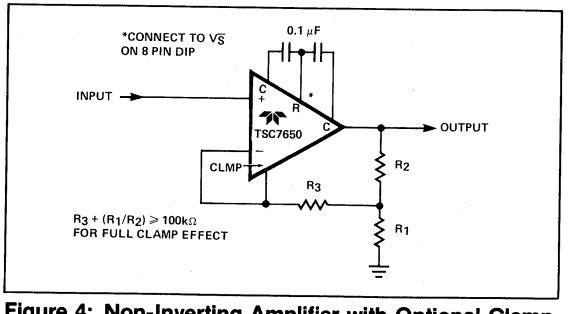


Figure 4: Non-Inverting Amplifier with Optional Clamp

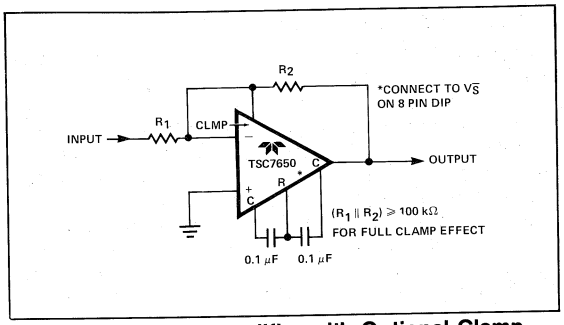


Figure 5: Inverting Amplifier with Optional Clamp

Static Protection

All device pins are static-protected. Strong static fields and discharges should be avoided, however, as they can degrade diode junction characteristics and increase input-leakage currents.

Many companies are actively involved in providing services, educational material, and supplies to aid electronic manufacturers in establishing "static safe" work areas where CMOS components are handled. A partial company listing is:

- 3M
  Static Control Systems Division
  223-25W EM Center
  St. Paul, MN 55101
  (800) 792-1072
- Semtronics
  P.O. Box 592
  Martinsville, NJ 08836
  (210) 561-9520
- American Convertors
  1919 South Butlerfield Road
  Mundelein, IL 60060
  (312) 362-9000
- ACL
  1960 East Devon Avenue
  Elk Grove Village, IL 60007
  (312) 981-9212

Latch-Up Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low impedance state, resulting in excessive supply current. To avoid the condition, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 0.1 mA to avoid latchup.

Thermo-Electric Potentials

Precision dc measurements are ultimately limited by thermoelectric potentials developed in thermocouple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermoelectric voltages typically around 0.1 μV/°C, but up to tens of μV/°C for some materials, will be generated. In order to realize the benefits extremely low offset voltages provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially those caused by power-dissipating elements in the system. Low thermoelectric-coefficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and separation from surrounding heat-dissipating elements is advised.

Pin Compatibility

On the 8-pin mini-dip TSC7650 the external null storage capacitors are connected to pins 1 and 8. On most other operational amplifiers these are left open or are used for offset potentiometer or compensation capacitor connections.

For OPO5 and OPO7 operational amplifiers, the replacement of the offset null pot between pins 1 and 8 by two capacitors from the pins to V^-_S will convert the OPO5/07 pin configuration for TSC7650 operation. For LM108 devices the compensation capacitor is replaced by the external nulling capacitors. The LM101/748/709 pin outs are modified similarly by also removing any circuit connections to pin 5. On the TSC7650 pin 5 is the output clamp connection. Other operational amplifiers may use this pin as an offset or compensation point.

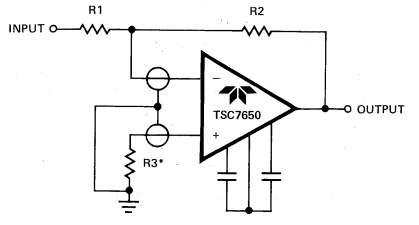
The minor modifications needed to retrofit a TSC7650 into existing sockets operating at reduced power supply voltages make prototyping and circuit verification straight forward.

Input Guarding

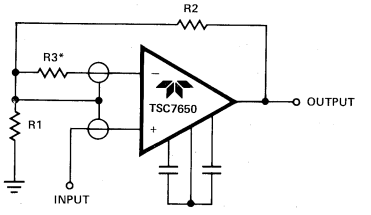
High impedance, low leakage CMOS inputs allow the TSC7650 to make measurements of high impedance sources. Stray leakage paths can increase input currents and decrease input resistance unless inputs are guarded. A guard is a conductive pc trace surrounding the input terminals. The ring connects to a low impedance point as the same potential as the inputs. Stray leakages are absorbed by the low impedance ring. The equal potential between ring and inputs prevents input leakage currents. Typical guard connections are shown in Figure 6.

The 14-pin DIP configuration has been specifically designed to ease input guarding. The pins adjacent to the inputs are unused.

In applications requiring low leakage currents, boards should be cleaned thoroughly and blown dry after soldering. Protective coatings will prevent future board contamination.



Inverting

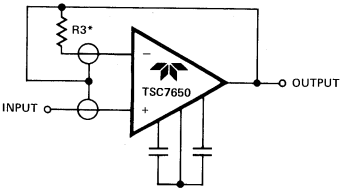


NOTE: $R_3 = \frac{R_1 R_2}{R_1 + R_2}$

SHOULD BE LOW IMPEDANCE FOR OPTIMUM GUARDING

Non-Inverting

*USE R3 TO COMPENSATE FOR LARGE SOURCE RESISTANCES, OR FOR CLAMP OPERATION.



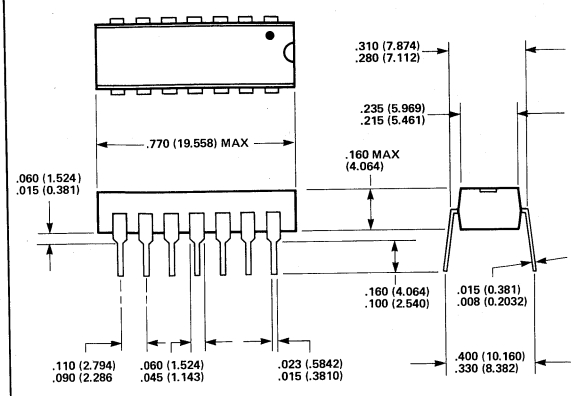
Follower

Component Selection

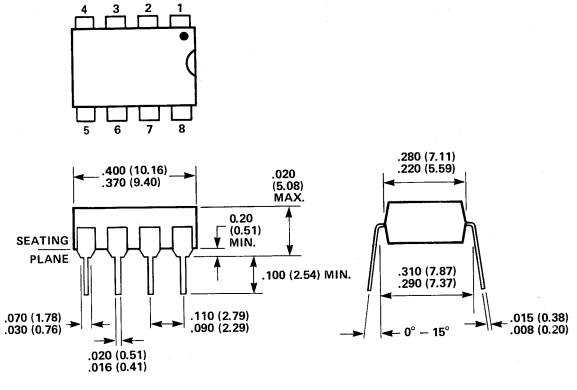
The two required capacitors, C_A C_B, have optimum values depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1 μF. To maintain the same relationship between the chopping frequency and the nulling time constant, the capacitor values should be scaled in proportion to the external clock if used. High-quality film-type capacitors such as mylar are preferred. Ceramic or other lower-grade capacitors may be suitable in some applications. For fast settling on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1 μV.

Figure 6: Input Guard Connection

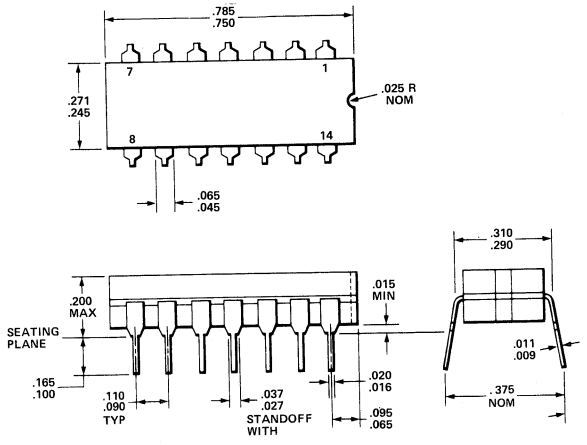
Package Outline



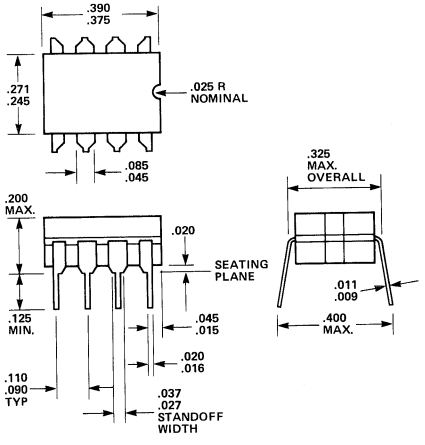
14-Pin Plastic Package (P)
(Package #6)



8-Pin Plastic Package (P)
(Package #4)

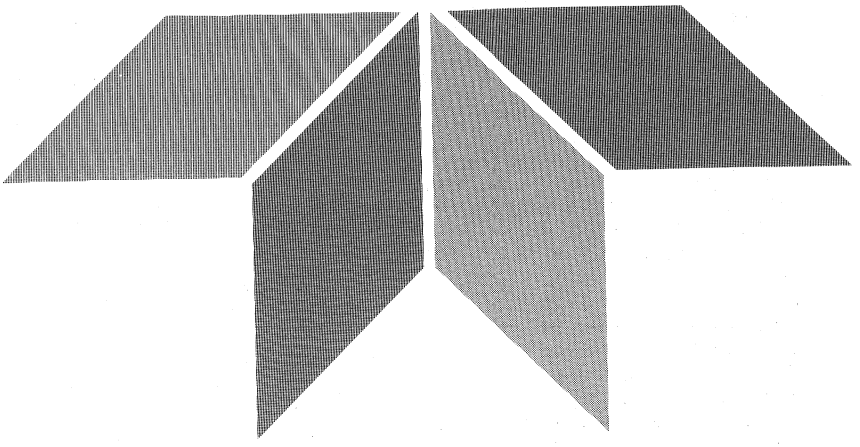


14-Pin CerDIP Package (J)
(Package #7)



8-Pin CerDIP Package (J)
(Package #5)

13



SECTION 14

Digital Logic

Section 14
Digital Logic

		14-1
	Purpose of Bipolar Interface Logic	14-3
	Most Popular 300 Series Devices	14-4
	Electrical Summary Data	14-6
	Input Current Requirements	14-8
	Output Sink Current vs. Output Voltage	14-9
	Pin-Out Guide	14-10
TSC301	Power NAND Gates Dual 5-Input	14-15
TSC302	Power NAND Gates Quad 2-Input	14-15
TSC303	Power NAND Gates Quad 2-Input	14-15
TSC304	Power NAND Gates Triple 4, 3, 4-Input	14-15
TSC306	NOR Gate Quad 2, 2, 3, 3-Input	14-19
TSC307	NOR Gate Quad 2, 2, 3, 3-Input	14-19
TSC311	Flip Flops Master/Slave RST	14-21
TSC312	Flip Flops Dual J-K Edge Triggered	14-21
TSC313	Flip Flops Dual J-K Master/Slave	14-21
TSC321	NAND Gates Quad 2-Input	14-27
TSC322	NAND Gates Dual 5-Input	14-27
TSC323	NAND Gates Quad 2-Input	14-27
TSC324	NAND Gates Quad 2-Input	14-27
TSC325	NAND Gates 2, 2, 3, 3-Input	14-31
TSC326	NAND Gates 2, 2, 3, 3-Input	14-31
TSC331	Gate Expander Dual 5-input	14-35
TSC332	Hex Inverter Gates 4-Inverter, 2-NAND	14-37
TSC333	Hex Inverter Gates 4-Inverter, 2-NAND	14-37
TSC334	Hex Inverter Gates Strobed Hex NAND	14-37
TSC335	Hex Inverter Gates Strobed Hex NAND	14-37
TSC341	Multifunction Gates Dual 2-Wide, 2-Input and/or Invert	14-41
TSC342	Dual Monostable Multivibrator	14-45
TSC343	Digital Comparator 4-Bit	14-49
TSC347	Dual Retriggerable Monostable Multivibrator	14-53
TSC349	Dual Retriggerable Pulse Stretcher	14-57
TSC350	Multiplexers 8-Bit	14-61
TSC351	Multiplexers Dual 4-Bit	14-61
TSC355	Timer	14-65
TSC361	Dual 11-16 V to 5 V Interface Voltage Translator	14-69
TSC362	5 V to 11-16 V Interface Dual Transistor	14-71
TSC363	5 V to 11-16 V Interface Quad 2-Input NAND	14-71
TSC367	Schmitt Trigger Quad Active Pullup	14-75
TSC368	Schmitt Trigger Quad Open Collector	14-75
TSC370	Flip Flop Quad D	14-81
TSC371	Counters Decade	14-83
TSC372	Counters Hexadecimal	14-83
TSC373	Up-Down Counter Decade	14-87
TSC374	Up-Down Counter Hexadecimal	14-87
TSC375	Shift Register 4-Bit	14-91
TSC380	BCD-to-Decade Decoder/Drivers Lamp Driver	14-95
TSC381	BCD-to-Decade Decoder/Drivers Logic Driver	14-95
TSC382	BCD-to-Decade Decoder/Drivers Gas Tube Driver	14-99
TSC383	Decoder/Driver BCD-to-7 Segment	14-103
TSC390	Dual Interface Buffers 4-Input Expandable AND	14-107
TSC391	Dual Interface Buffers 2-Input AND	14-107
TSC392	Dual Interface Buffers 2-Input NAND	14-107
TSC393	Dual Interface Buffers 2-Input OR	14-107
TSC394	Dual Interface Buffers 2-Input NOR	14-107
TSC395	Dual Interface Buffers 4-Input Expandable NAND	14-107
TSC396	Line Driver Receiver Dual Differential	14-111

NOTE:

Application Notes and Application Briefs pertaining to the products in this section can be found in the Application Notes section of this catalog.

Bipolar Interface Logic

Purpose of Bipolar Interface Logic

PROTECTING CMOS AND µP SYSTEMS

Bipolar Interface Logic - the 300 Series - is a remarkably simple solution to interfacing your CMOS and µp systems (which operate on 12 or 15V power supplies) with the outside world.

OPERATION ON 11V TO 16V

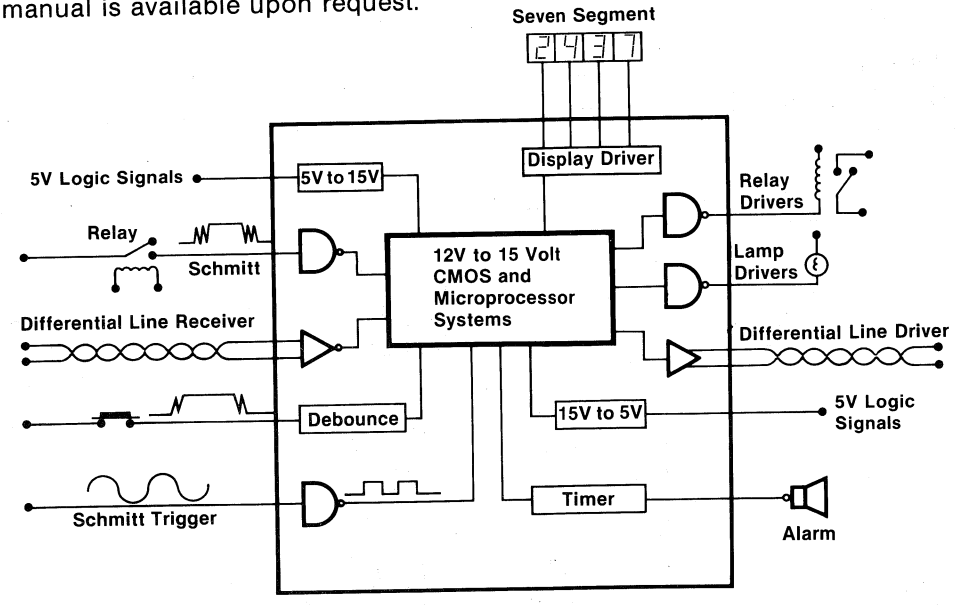
These bipolar circuits have the unique ability to operate on 11V to 16V power supplies with an input threshold of 6V, which allows noise margins from 3.5V up to 6.5V. This eliminates worry about the high-voltage spikes or noise generated by bouncing switches, SCR's, relays, solenoids or large motors. Also, the rugged bipolar construction of the 300 series minimizes catastrophic failures often caused by high voltage spikes or improper maintenance.

LOW OUTPUT IMPEDANCE

With low output impedances, the 300 series can handle high drive currents of up to 250mA, which makes them ideal for driving relays, solenoids, SCR's, displays or long lines.

MANY SOLUTIONS OFFERED BY THE 300 SERIES

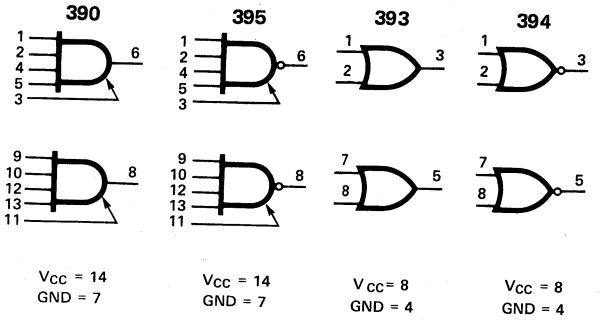
Teledyne Semiconductor's Bipolar Interface Logic line includes buffer gates, power drivers, timing elements and much more. For more product information, a new 170-page data manual is available upon request.



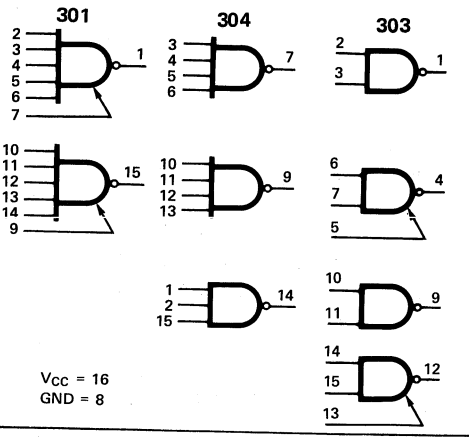
A detailed explanation of High Noise Immunity Bipolar Interface Logic and its uses can be found in Application Note 1 reprinted in Section 15 of this data book.

Most Popular 300 Series Devices

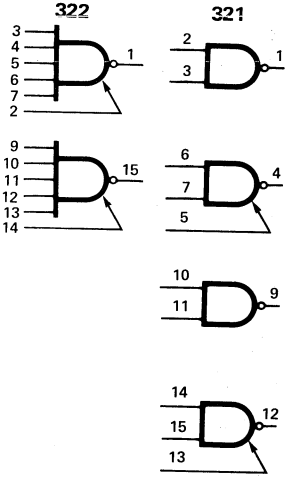
POWER GATES
250mA SINK CURRENT



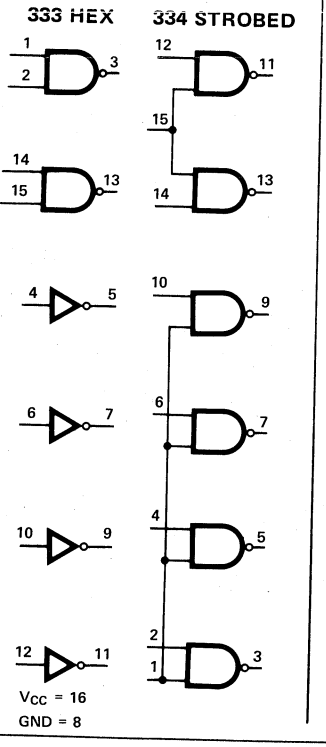
BUFFER GATES
42mA SINK CURRENT



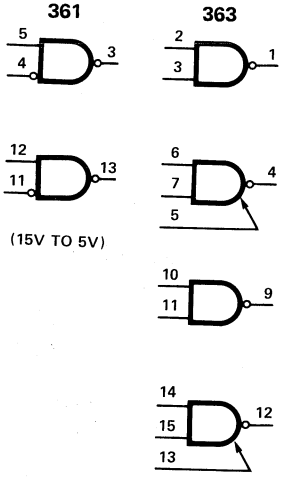
GATES
10mA SINK CURRENT



HEX BUFFERS
10mA SINK CURRENT



VOLTAGE LEVEL TRANSLATORS

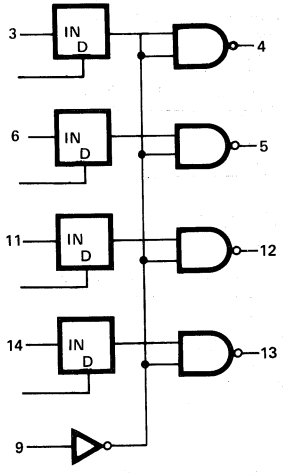


Bipolar Interface Logic

Most Popular 300 Series Devices

QUAD SCHMITT TRIGGER

367/368

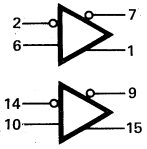


V_{CC} = 16
GND = 8

D = DELAY PIN

DIFFERENTIAL LINE DRIVER/ RECEIVER

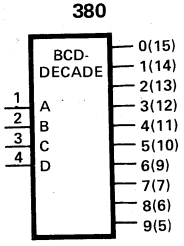
396



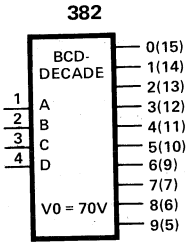
V_{CC} = 16
GND = 8

DECODERS/DRIVERS

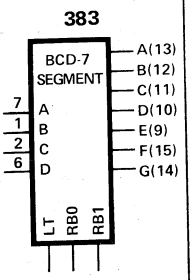
380



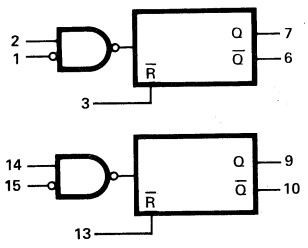
382



383

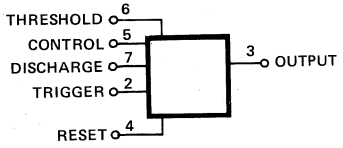


DUAL RETRIGGERABLE ONE SHOT



V_{CC} = 16
GND = 8

TIMER FROM MICROSECONDS TO HOURS



PIN COMPATIBLE TO 555
FOR V_{CC} = 10.5 - 16V

V_{CC} = 8
GND = 1

Additional Products:

- **Digital Multiplexers**
- **Four Bit Comparators**
- **Decade Counters**
- **Up/Down Counters**
- **Quad D Flip Flops**
- **AND-OR-Invert Gates**
- **Dual, Triple and Quad Gates**

14

Bipolar Interface Logic
Electrical Summary Data

Parameter	Definition	Type C* (V_{CC} = +12V ±1V) -30° C ≤ T_A ≤ +85° C	Test Conditions
V_{CC}	Supply Voltage	13V max 12V nominal 11V min	(Voltage for other tests — see below)
V_{INL}	Input Threshold Voltage, Low	5.0V min	Guaranteed input low threshold for all inputs except 311 T_2 = 4.8V min @ 15V
V_{INH}	Input Threshold Voltage, High	6.5V max	Guaranteed input high threshold for all inputs except 311 $\overline{S}$&$\overline{R}$ inputs = 7.0V max
I_{INL}	Input Current, Low; 1 Unit Load (UL)	2.1 mA max	At V_{CC} max with V_{IN} = V_{OL}
I_{INH}	Input Leakage Current; 1 Unit Load (UL)	10 μA max	At V_{CC} = max with V_{IN} = V_{CC} max
I_{MAX} 382	Output High Breakdown Current (Open Collector Devices)	2 mA max	V_{CEX} = +65V
V_{OL}	Output Low Voltage (see Loading Table on Data Sheet)	1.5V max	I_{OL} = F.O. x UL at V_{CC} min with V_{INL} = 5.0V and V_{INH} = 6.5V
V_{OL} 302 323 332 334 380 382 383 383	Output Low Voltage (Open Collector Devices)	.4V max .4V max .4V max .4V max 1.2V max 2.5V max .7V max 1.2V max	I_{OL} = 16 mA (10 TTL UL) I_{OL} = 6.4 mA (4 TTL UL) I_{OL} = 6.4 mA (4 TTL UL) I_{OL} = 6.4 mA (4 TTL UL) I_{OL} = 30 mA I_{OL} = 7 mA I_{OL} = 20 mA (100% Duty Cycle) I_{OL} = 40 mA (50% Duty Cycle)
V_{OH}	Output High Voltage of all Devices Without Open Collector Except 362 and 396	10.0V min	At V_{CC} min, V_{INL} = 5.0V, V_{INH} = 6.5V; I_{OH} = F.O. x UL
V_{MAX} 302,323 332,334 380 381 390-395	Output High Breakdown Voltage (Open Collector Devices)	13.0V min 20.0V min 24.0V min 15.0V min 30.0V min	I_{MAX} = 4 mA I_{MAX} = 4 mA I_{MAX} = 0.5 mA I_{MAX} = 0.5 mA
V_{OHL}	Output High Voltage, Loaded, of Active Pullup Devices Except 362 and 306	7.0V min	At V_{CC} nominal, V_{INL} = 5.0V, V_{INH} = 6.5V; I_{OH} = -5 mA (except -15 mA for 301 and -12 mA for 350,351
I_{CEX} 302,323,307 332,334 380,381 382 383 390-395	Output High Leakage Current (Open Collector Devices)	25 μA max 25μA max 25 μA max 50 μA max 25 μA max 100 μA max	V_{CEX} = V_{CC} max V_{CEX} = V_{CC} max V_{CEX} = V_{CC} max V_{CEX} = +55V V_{CEX} = V_{CC} max V_{CEX} = 30V
"0" N.I.	Zero State Noise Immunity	3.5V min	Guaranteed zero state noise immunity across temp range and V_{CC} ± 1V. V_{INL} — V_{OL}
"I" N.I.	One State Noise Immunity	3.5V min	Guaranteed one state noise immunity across temp range and V_{CC} ± 1V. V_{OH} — V_{INH}

Notes: F.O. is fanout in unit loads (UL). Unit loadings are given in the pin tables on the individual data sheets. A unit load for High Noise Immunity Logic is defined by the above input specifications.

See individual data sheets for additional specifications.

*Military spec Type B (V_{CC} = 12V) and Type M (V_{CC} = 15V) are available to meet -55° C to +125° C temperature requirements. Available in ceramic package only. See ordering data.

Electrical Summary Data (Continued)

Absolute Maximum Ratings

	L Package, Ceramic	J Package, Plastic
Storage Temperature	-65° C to +150° C	-55° C to +100° C
Lead Temperature (1/16 inch from case, 10 sec max)	300° C	300° C
Continuous Supply Voltage		
Type C*, B*	+15.0V	+15.0V
Type A*, M*	+16.5V	+16.5V
Pulsed Supply Voltage (less than 100 msec)	+18.0V	+18.0V
Input Voltage (any input)		
Type C*, B*	-0.5 to +15V	-0.5 to +15V
Type A*, M*	-0.5 to +18V	-0.5 to +18V
Surge Sink Current (less than 100 msec at 25° C T_A)		
Standard Outputs	20mA	20mA
301, 302 and 303	100mA	100mA
306, 307, 332 through 335, 350, 351, 380, 381, 383	35mA	35mA
390-395	300mA	—
355	150mA	150mA
Expander Input Currents	-0.5 to +0.5mA	-0.5 to +0.5mA

Note: Exceeding the absolute maximum ratings may cause permanent damage. Function of HiNIL devices at the absolute maximum ratings or beyond the conditions guaranteed is not implied.

Bipolar Interface Logic

Input Current Requirements

Device Number	I_{INL} @ V_{CC} = 12V and V_{IL} = 1.5V (mA)	I_{INL} @ V_{CC} = 15V and V_{IL} = 1.5V (mA)	I_{INH} @ V_{CC} = 12 or 15V, V_{INH} = V_{CC} (mA)
301	2.1	2.6	10
302	2.1	2.6	10
303	2.1	2.6	10
304	2.1	2.6	10
306	1.3	1.6	10
307	1.3	1.6	10
311	2.1-4.2	2.6-5.2	10-20
312	2.1-4.2	2.6-5.2	10-20
313	2.1-4.2	2.6-5.2	10-20
321	2.1	2.6	10
322	2.1	2.6	10
323	2.1	2.6	10
324	2.1	2.6	10
325	2.1	2.6	10
326	2.1	2.6	10
332	2.1	2.6	10
333	2.1	2.6	10
334	2.1	2.6	10
335	2.1	2.6	10
341	2.1	2.6	10
342	2.1	2.6	10
343	2.1-4.2	2.6-5.2	10-20
347	2.1-4.2	2.6-5.2	10-20
349	2.1	2.6	10
350	2.1	2.6	10
351	2.1	2.6	10
355	0.01	0.01	10
361	2.1	2.6	10
362	0.47	0.47	10
363	1.6	1.6	10
367	2.1	2.6	40
368	2.1	2.6	40
370	2.1-4.2	2.6-5.2	10-20
371	2.1-4.2	2.6-5.2	10-20
372	2.1-4.2	2.6-5.2	10-20
373	2.1	2.6	10
374	2.1	2.6	10
375	2.1	2.6	10
380	2.1	2.6	10
381	2.1	2.6	10
382	2.1	2.6	10
383	2.1-6.3	2.6-7.8	10-30
390	0.7	1.0	10
391	0.7	1.0	10
392	0.7	1.0	10
393	0.7	1.0	10
394	0.7	1.0	10
395	0.7	1.0	10
396	0.4	1.0	10

Notes:

1. If there are several types of inputs on a device, then the currents listed above are the range of values for the various inputs. Check the individual data sheets to determine what the input current requirements are for each input.
2. A unit load is defined as I_{INL} @ 12V = 2.1mA max, I_{INL} @ 15V = 2.6mA max and I_{INH} = 10μA max at 12 or 15V.
3. CMOS operated at 12 or 15V can be used to drive these devices even if the V_{OL} rating of the CMOS device does not appear to give enough sink current. This is possible since the 300 series of devices has input low rated at ≤5V instead of 0.8V as is common with TTL parts. The result is the CMOS output will be operated at a V_{OL} larger than is typical for CMOS or TTL systems.

Output Sink Current vs. Output Voltage

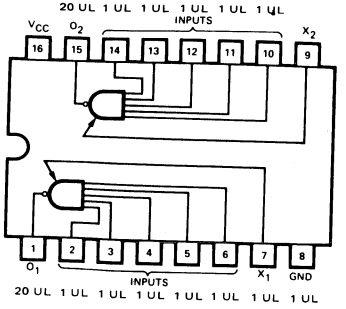
Device Number	V_{OL} (V)	I_{OL} (mA)
301	1.5	42
302	.4	42
303	.4	42
304	.4	42
306	1.5	18
307	.4	10
311	1.5	12
312	1.5	10
313	1.5	10
321	1.5	10
322	1.5	10
323	.4	10
324	.4	10
325	1.5	10
326	.4	10
332	.4	10
333	.4	10
334	.4	10
335	.4	10
341	1.5	10
342	1.5	10
343	1.5	10
347	1.5	10
349	1.5	10

Device Number	V_{OL} (V)	I_{OL} (mA)
350	1.5	16
351	1.5	16
355	2.0	75
361	.4	10
362	.4	10
363	.4	30
367	1.5	10
368	.4	10
370	.4	10
371	.4	10
372	.4	10
373	1.5	10
374	1.5	10
375	1.5	6
380	.4	20
381	.4	10
382	2.5	7
383	.7	20
390	.7	250
391	.7	250
392	.7	250
393	.7	250
394	.7	250
395	.7	250
396	1.5	12

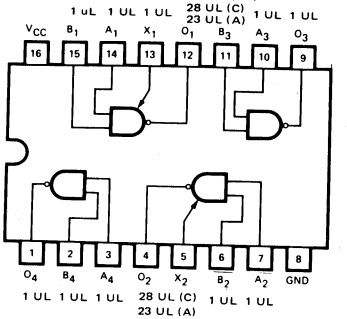
Bipolar Interface Logic

Pin-Out Guide

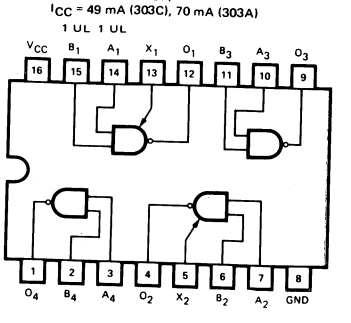
301 DUAL FIVE INPUT POWER NAND GATE
(ACTIVE PULL-UP)
I_{CC} = 48 mA (301C), 68 mA (301A)



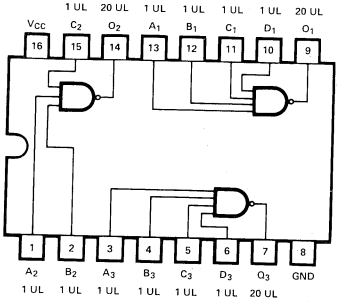
302 QUAD TWO INPUT POWER GATE
(OPEN COLLECTOR)
I_{CC} = 40 mA (302C), 60 mA (302A)



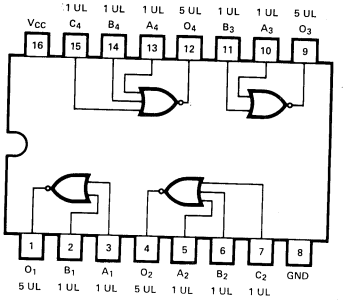
303 QUAD TWO INPUT POWER GATE
(PASSIVE PULL-UP)
I_{CC} = 49 mA (303C), 70 mA (303A)



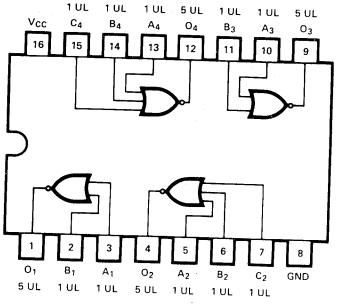
304 TRIPLE 4, 3, 4 INPUT NAND
(PASSIVE PULL-UP)
I_{CC} = 40 mA (304C), 60 mA (304A)



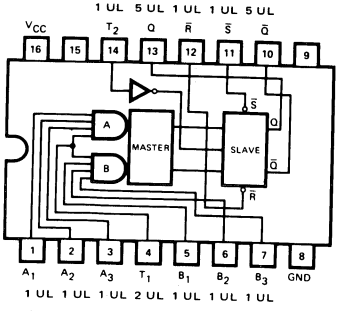
306 2, 2, 3, 3 INPUT NOR GATE
(ACTIVE PULL-UP)
I_{CC} = 34 mA (306C), 40 mA (306A)



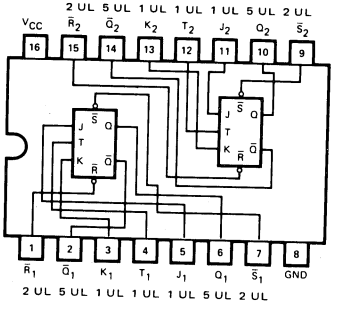
307 2, 2, 3, 3 INPUT NOR GATE
(OPEN COLLECTOR)
I_{CC} = 23 mA (307C), 28 mA (307A)



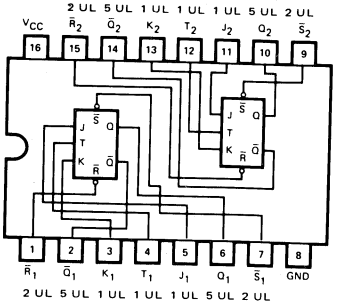
311 MASTER/SLAVE FLIP-FLOP
(ACTIVE PULL-UP)
I_{CC} = 18 mA (311C) 25 mA (311A)



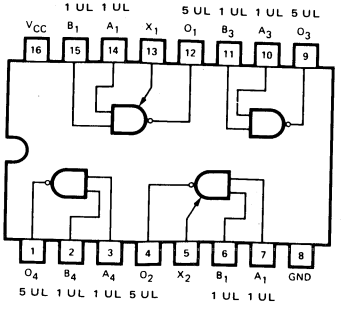
312 DUAL J-K FLIP-FLOP
(ACTIVE PULL-UP)
I_{CC} = 30 mA (312C) 40 mA (312A)



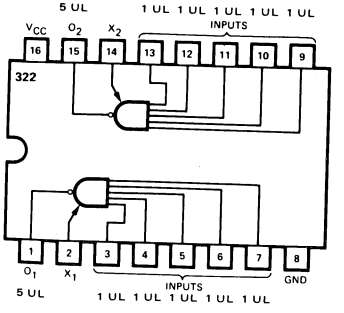
313 DUAL J-K FLIP-FLOP
(ACTIVE PULL-UP)
I_{CC} = 30 mA (312C) 40 mA (312A)



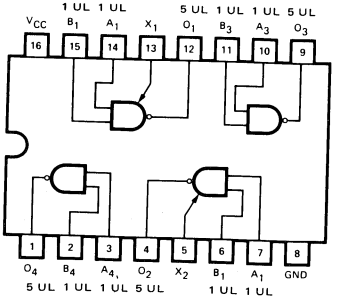
321 QUAD TWO INPUT NAND GATE
(ACTIVE PULL-UP)
I_{CC} = 15 mA (321C), 20 mA (321A)



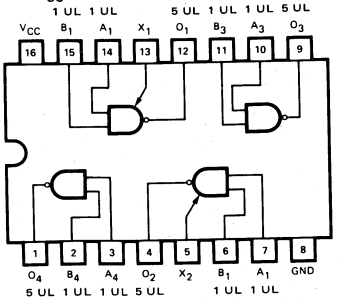
322 DUAL FIVE INPUT NAND GATE
(ACTIVE PULL-UP)
I_{CC} = 8 mA (322C), 11 mA (322A)



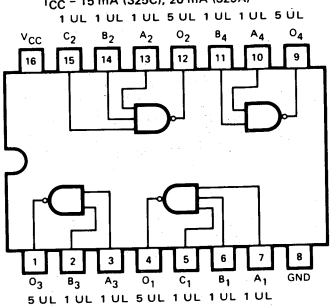
323 QUAD TWO INPUT NAND GATE
(OPEN COLLECTOR)
I_{CC} = 5.5 mA (323C), 8 mA (323A)



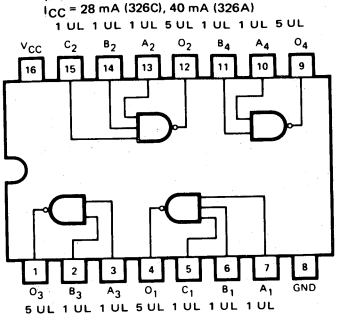
324 QUAD TWO INPUT NAND GATE
(PASSIVE PULL-UP)
I_{CC} = 28 mA (324C), 40 mA (324A)



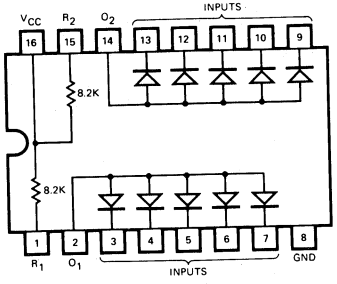
325 2, 2, 3, 3-INPUT NAND GATE
(ACTIVE PULL-UP)
I_{CC} = 15 mA (325C), 20 mA (325A)



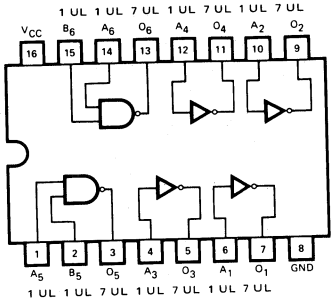
326 2, 2, 3, 3 INPUT NAND GATE
(PASSIVE PULL-UP)
I_{CC} = 28 mA (326C), 40 mA (326A)



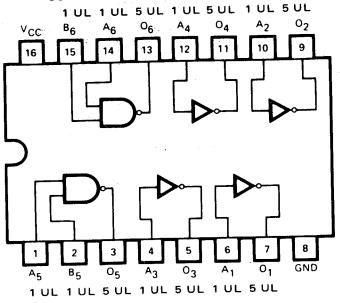
331 DUAL FIVE INPUT GATE EXPANDER
I_{CC} = 4.2 mA (331C), 5.2 mA (331A)



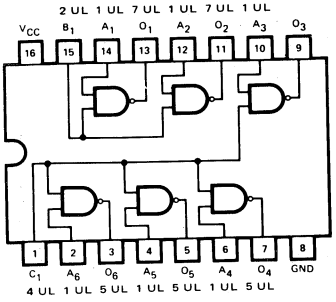
332 HEX INVERTER GATE
(OPEN COLLECTOR)
I_{CC} = 28 mA (332C), 42 mA (332A)



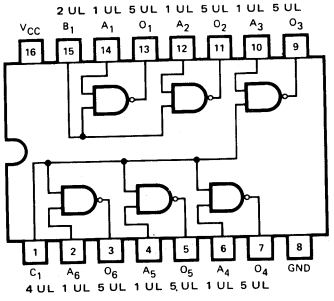
333 HEX INVERTER GATE
(PASSIVE PULL-UP)
I_{CC} = 42 mA (333C), 60 mA (333A)



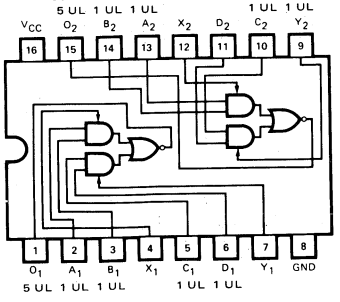
334 STROBED HEX INVERTER GATE
(OPEN-COLLECTOR)
I_{CC} = 28 mA (334C), 42 mA (334A)



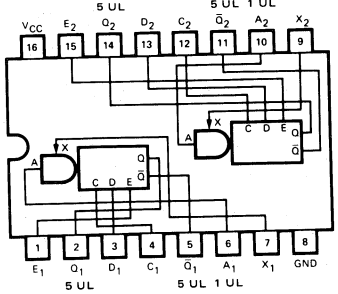
335 STROBED HEX INVERTER GATE
(PASSIVE PULL-UP)
I_{CC} = 42 mA (335C), 60 mA (335A)



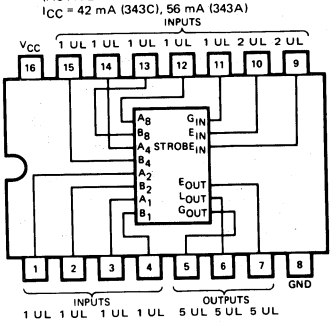
341 DUAL 2-WIDE, 2 INPUT AND-OR-INVERT GATE
(ACTIVE PULL-UP)
I_{CC} = 11 mA (341C), 15 mA (341A)



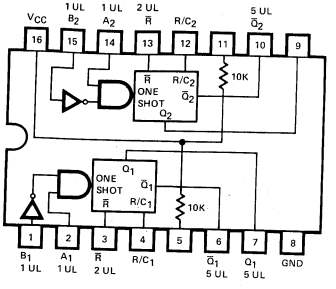
342 DUAL MONOSTABLE MULTIVIBRATOR
(ACTIVE PULL-UP)
I_{CC} = 17 mA (342C), 23 mA (342A)



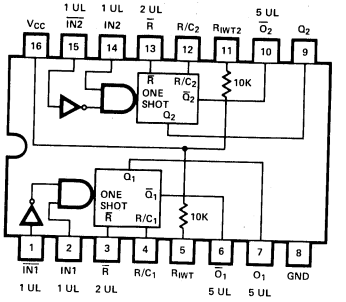
343 FOUR BIT COMPARATOR
(ACTIVE PULL-UP)
I_{CC} = 42 mA (343C), 56 mA (343A)



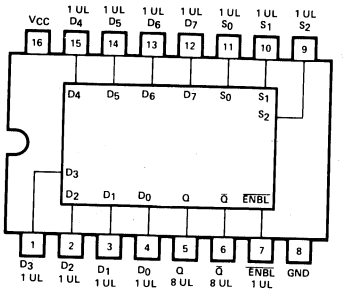
347 DUAL RETRIGGERABLE MONOSTABLE
(ACTIVE PULL-UP)



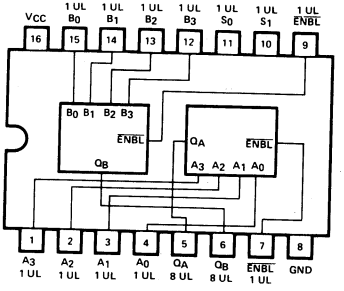
349 DUAL RETRIGGERABLE PULSE STRETCHER
(ACTIVE PULL-UP)
I_{CC} = 40 mA (349C), 50 mA (349A)



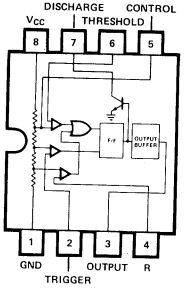
350 EIGHT BIT MULTIPLEXER
(ACTIVE PULL-UP)
I_{CC} = 33 mA (350C), 40 mA (350A)



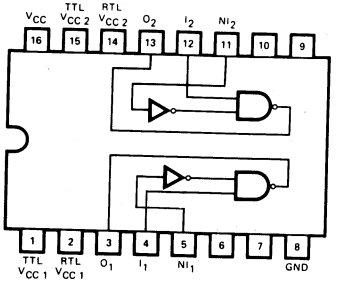
351 DUAL FOUR BIT MULTIPLEXER
(ACTIVE PULL-UP)
I_{CC} = 33 mA (351C), 40 mA (351A)



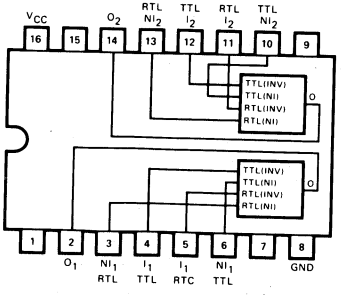
355 TIMER
I_{CC} = 20 mA



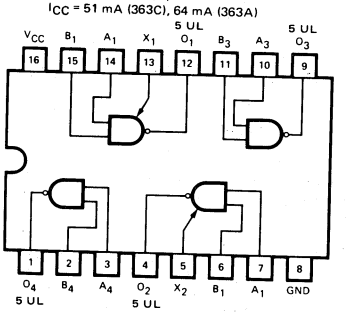
361 DUAL INPUT INTERFACE
(PASSIVE PULL-UP)
I_{CC} = 8 mA (361C), 11 mA (361A)



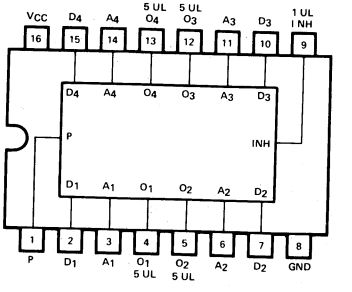
362 DUAL OUTPUT INTERFACE
(ACTIVE PULL-UP)
I_{CC} = 10 mA (362C), 13 mA (362A)



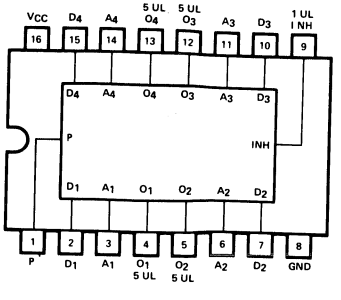
363 QUAD OUTPUT INTERFACE
(PASSIVE PULL-UP)
I_{CC} = 51 mA (363C), 64 mA (363A)



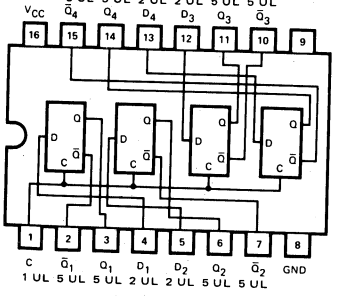
367 QUAD SCHMITT TRIGGER
(ACTIVE PULL-UP)
I_{CC} = 36 mA (367C), 54 mA (367A)



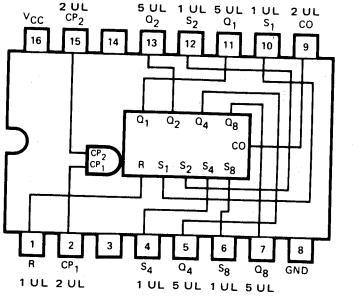
368 QUAD SCHMITT TRIGGER
(OPEN COLLECTOR)
I_{CC} = 33 mA (368C), 50 mA (368A)



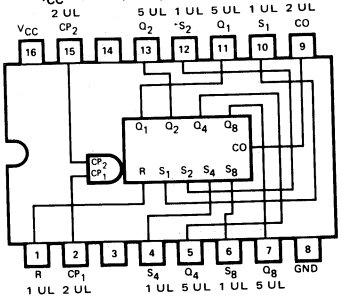
370 QUAD D FLIP-FLOP
(PASSIVE PULL-UP)
I_{CC} = 38 mA (370C), 48 mA (370A)



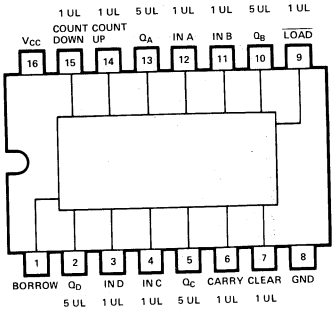
371 DECADE COUNTER
(PASSIVE PULL-UP)
I_{CC} = 41 mA (371C), 53 mA (371A)



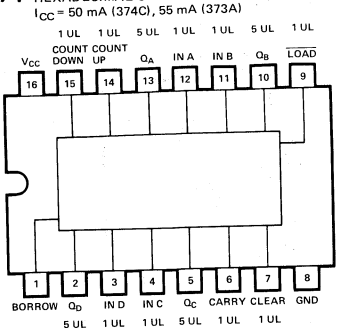
372 HEXADECIMAL COUNTER
(PASSIVE PULL-UP)
I_{CC} = 41 mA (372C), 53 mA (372A)



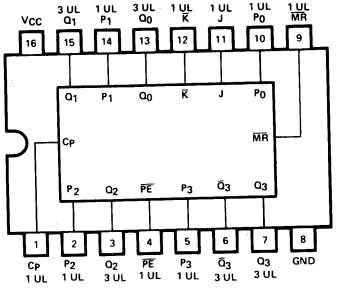
373 DECADE UP-DOWN COUNTER
I_{CC} = 50 mA (373C), 55 mA (373A)



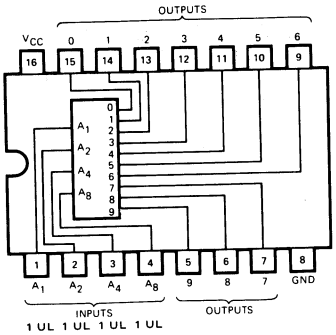
374 HEXADECIMAL UP-DOWN COUNTER
I_{CC} = 50 mA (374C), 55 mA (373A)



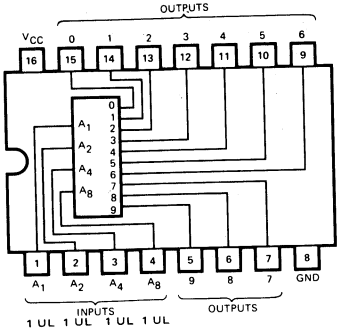
375 FOUR BIT SHIFT REGISTER
(ACTIVE PULL-UP)
I_{CC} = 48 mA (375C), 64 mA (375A)



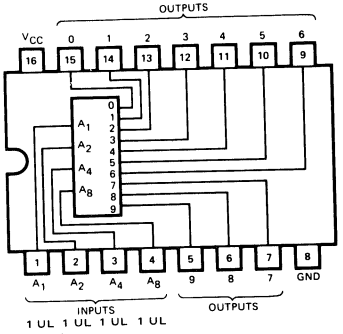
380 BCD TO DECADE DECODER/LAMP DRIVER
(OPEN-COLLECTOR)
I_{CC} = 30 mA (380C), 38 mA (380A)



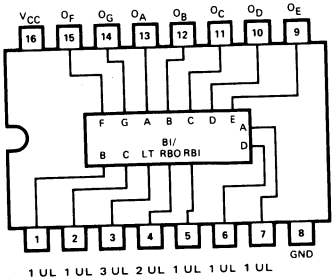
381 BCD TO DECADE DECODER/LOGIC DRIVER
(OPEN COLLECTOR)
I_{CC} = 30 mA (383C), 38 mA (383A)



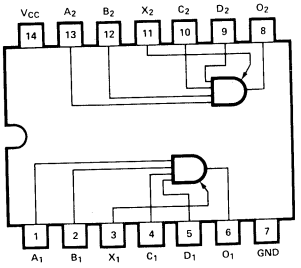
382 BCD TO DECADE DECODER/GAS DISCHARGE
(OPEN-COLLECTOR) TUBE DRIVER
I_{CC} = 24 mA (382C), 31 mA (382C)



383 BCD TO SEVEN SEGMENT DECODER/DRIVER
(OPEN-COLLECTOR)
I_{CC} = 40 mA (383C), 44 mA (383A)

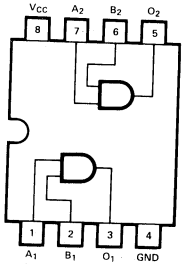


390 DUAL 4 INPUT POWER AND
I_{CC} = 40 mA

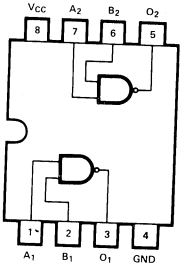


14

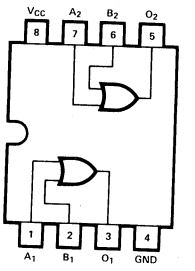
391 DUAL 2 INPUT POWER AND
I_{CC} = 40 mA



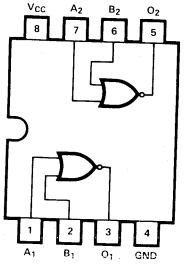
392 DUAL 2 INPUT POWER NAND
I_{CC} = 40 mA



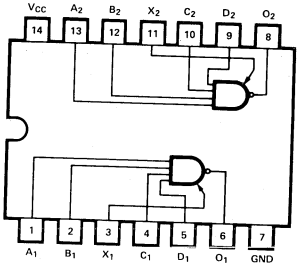
393 DUAL 2 INPUT POWER OR
I_{CC} = 40 mA



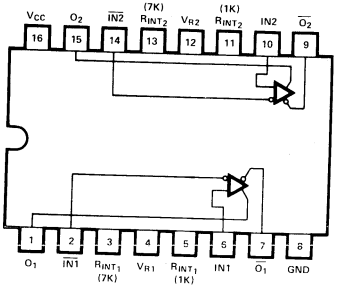
394 DUAL 2 INPUT POWER NOR
I_{CC} = 40 mA



395 DUAL 4 INPUT POWER NAND
I_{CC} = 40 mA



396 DUAL DIFF. LINE DRIVER/RECEIVER
I_{CC} = 25 mA



TELEDYNE SEMICONDUCTOR

TSC301/302/303/304
Power NAND Gates
- Dual 5-Input
- Quad 2-Input (Open Collector)
- Quad 2-Input (Passive Pullup)
- Triple 4, 3, 4-Input (Passive Pullup)

Features

- 15 mA DRIVE CURRENT
- DRIVES LINES UP TO 1,000 FEET LONG
- IDEAL SYSTEM CLOCK DRIVER
- DRIVES LAMPS AND RELAYS DIRECTLY
- EXPANDER INPUTS

302/303/304

- FANOUT UP TO 20
- COLLECTOR OR'ABLE
- IDEAL LAMP DRIVERS
- EXPANDER INPUTS
- 302 OUTPUT LEVELS ADJUSTABLE TO DTL, TTL OR MOS LEVELS
- 303, 304 HAVE PASSIVE PULLUP RESISTORS ON CHIP

General Descriptions

301

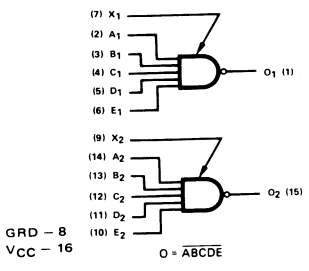
The 301 is an expandable buffer gate with high drive and sink currents. It is ideal for applications such as driving lamps, relays and long lines, and it makes an excellent system clock driver. The outputs are active pullup.

302/303/304

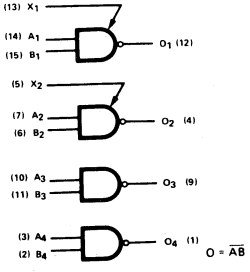
The 302, 303 and 304 are buffer gates for applications such as "wire-OR" logic systems, lamp driving and interfaces with other logic families. Two gates in each 302 and 303 package have expander inputs. The 302 is used with an external pullup resistor while the 303 and 304 have pullup resistors on the chip.

Logic Diagrams

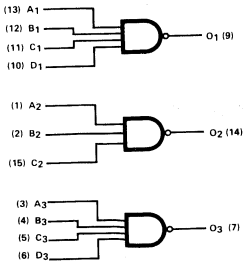
301



302/303



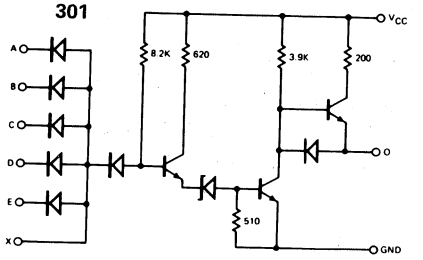
304



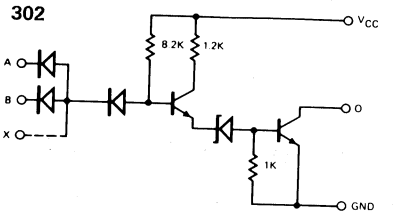
14

Equivalent Circuits

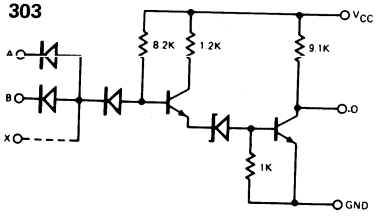
301



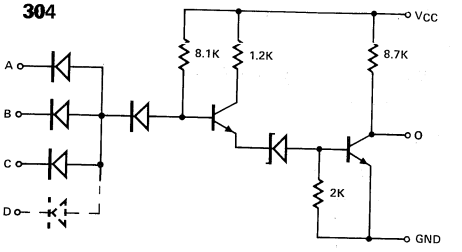
302



303



304



Specifications

301

I_{CC} (WORST-CASE)	48 mA @ 13V, 68 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	240 ns A+O–	400 ns A–O+

302

I_{CC} (WORST-CASE)	40 mA @ 13V, 60 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	240 ns A+O–	600 ns A–O+

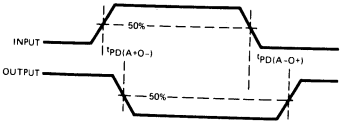
303, 304

I_{CC} (WORST-CASE)	49 mA @ 13V, 70 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	240 ns A+O–	600 ns A–O+

NOTE:
I_{CC} is tested at V_{CC} + 1 Volt (+13V for C Type and +16V for A Type) and is guaranteed across the applicable temp range. t_{PD} is guaranteed at V_{CC} ±1V and across the applicable temp range with the output loaded (28 UL – 302C, 25 UL – 303C, 304C; 23 UL – 302A, 20 UL – 303A, 304A).

See page 12 for electrical summary data.

Switching Time Waveforms



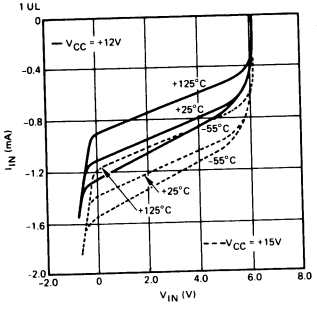
Loading Table

PINS	FUNCTION	LOADING
A,B	Inputs	1 UL
X	Expanders	Each diode tied to X, or X_2 is 1 unit load
0	Outputs	20 UL (301) 20 UL (302 with 3.9KΩ pullup resistor) 20 UL (303, 304 with 5.6KΩ pullup resistor)

302 handles 10 TTL loads at 400 mV.

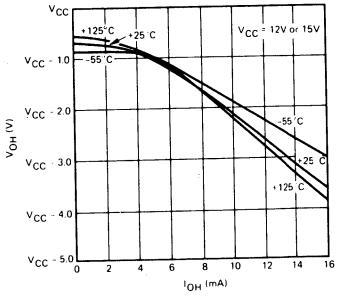
Typical Performance Characteristics

INPUT CURRENT VS. INPUT VOLTAGE

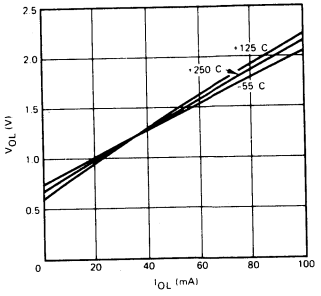


OUTPUT CURRENT VS OUTPUT VOLTAGE

OUTPUT HIGH 301

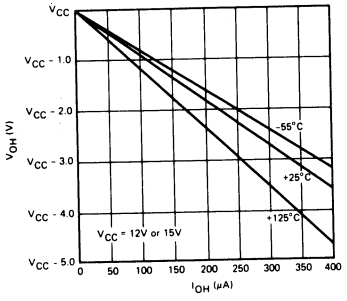


OUTPUT LOW 301

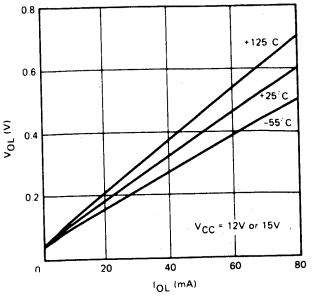


OUTPUT CURRENT VS OUTPUT VOLTAGE

OUTPUT HIGH 303, 304



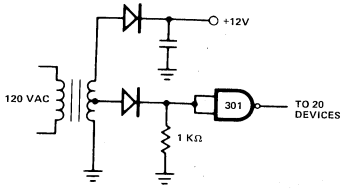
OUTPUT LOW 302, 303, 304



14

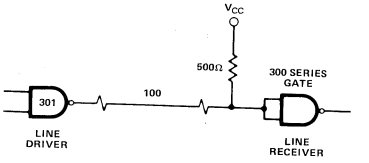
Typical Applications

60 Hz SYSTEM CLOCK



The center tap on the power supply transformer serves as a system clock.

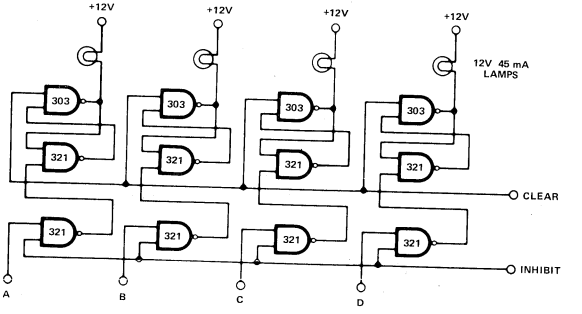
LINE DRIVER



Up to 10,000 pF can be driven by the 301. When the 301 is used in this way, terminate the line with a 500Ω resistor.

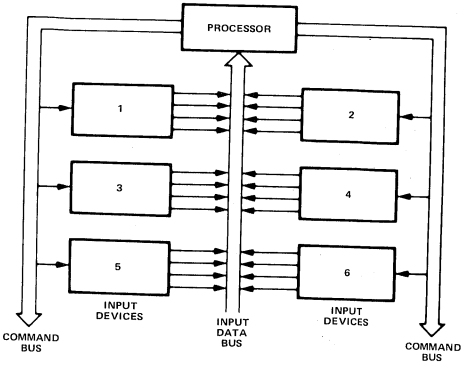
Rules for selecting external resistors and calculating fanout with collectors OR'd are given in the applications notes. The external resistor of the 302 may be connected to a voltage other than V_{CC} to adjust the output voltage level. The expandable gates may be provided any number of inputs by adding 331 gate expanders or 1N4148 diodes (or any 20-volt silicon diodes) to the expander inputs.

50 mA QUAD FLIP-FLOP

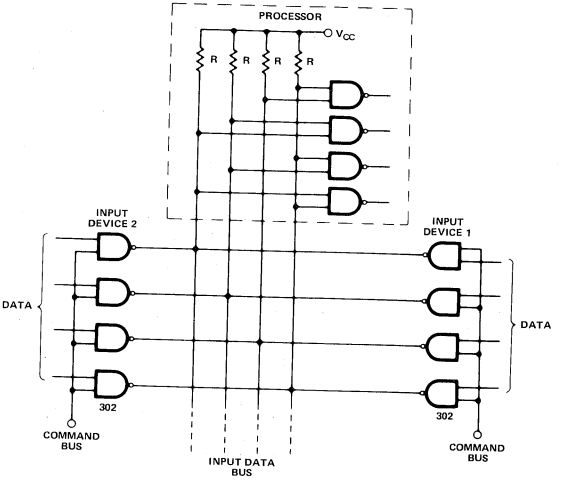


The 303 serves here as lamp driver outputs on latches formed by 303 and 321 gates. The circuit also provides inhibit and clear lines.

CONNECTIONS TO DATA BUS



Each input device is connected to the data bus through a 302 used in the collector-OR configuration. Up to 20 input devices may be connected to a 4-line bus segment. Pullup resistors R are chosen by the rules given in the applications notes.



TSC306/307 NOR Gates

- Quad 2, 2, 3, 3-Input (Active Pullup)
- Quad 2, 2, 3, 3-Input (Open Collector)

Features

Versatile Configuration

Active Pullup Outputs (306)

Open Collector Outputs (307) — Collector OR'able

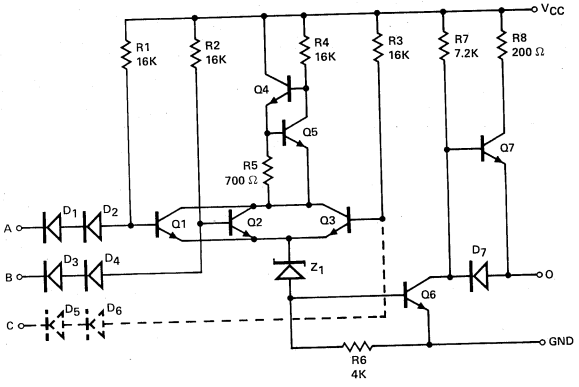
I_{OHL} = 10mA (306) — drives lines up to 10 feet

General Description

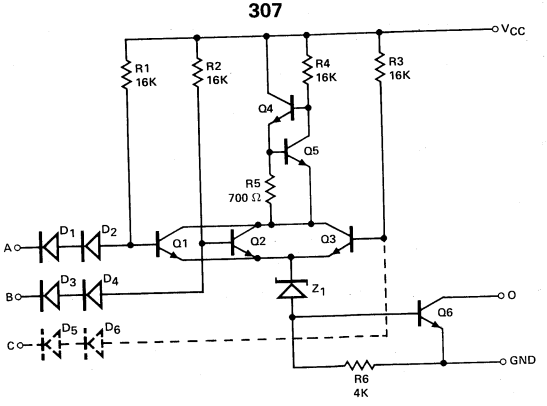
The HiNIL 306 and 307 each contain two 2-input NOR gates and two 3-input NOR gates. The active pullup and 10mA output drive current of the 306 allow it to drive moderately long lines with no loss of noise immunity. The 307 has open collectors, so that outputs may be collector OR'd.

Equivalent Circuits

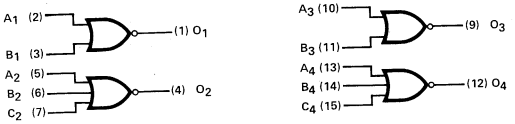
306



307



Logic Diagrams

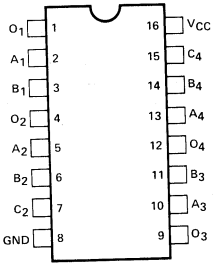


Loading Table

Pins	Function	Loading
A, B, C	Input	1 UL
O	Outputs	10 UL (306)
		10 UL (307 with 5.6KΩ pullup resistor

Connection Diagrams

L Package
16 Lead Ceramic DIP



Order Part Numbers:

306AL/CL, 307AL/CL
(V_{CC} = 10V to 16V,
$-30^{\circ}C \leq T_A \leq +70^{\circ}C$)

14

Absolute Maximum Ratings

	L Package
Continuous Supply Voltage	16.5V
Pulsed Supply Voltage (less than 100 ms)	18.0V
Input Voltage (any input)	−0.5 to +18V
Surge Sink Current (less than 100 ms at 25°C T_A)	35 mA
Storage Temperature	−65°C to +150°C
Lead Temperature (1/16 inch from case, 10 sec max)	300°C

Electrical Characteristics (Operating V_{CC} range = 10V to 16V, −30°C ≤ T_A ≤ +70°C)

Parameter		Definition	Limits @ V_{CC} = 10V	Limits @ V_{CC} = 13V	Limits @ V_{CC} = 16V	Units	Conditions
V_{INL}		Input Threshold Voltage, Low	5.0	5.0	5.0	V min.	
V_{INH}		Input Threshold Voltage, High	6.5	6.5	6.5	V max.	
I_{INL}		Input Current, Low	−1.0	−1.3	−1.6	mA max.	V_{IN} = 1.5V
V_{OL}		Output Low Voltage	1.5	1.5	1.5	V max.	I_{OL} = 16 mA, V_{IN} = 6.5V I_{OL} = 21 mA, V_{IN} = 6.5V I_{OL} = 26 mA, V_{IN} = 6.5V
V_{OL2}	(307)	Output Low Voltage, Driving TTL	400	400	400	mV max.	I_{OL} = 10 mA, V_{IN} = 6.5V
V_{OH}	(306)	Output High Voltage	9	12	15	V min.	I_{OH} = −100μA, V_{IN} = 5.0V
V_{OHL}	(306)	Output High Voltage, Loaded	5	8	11	V min.	I_{OH} = −10 mA, V_{IN} = 5.0V
V_{MAX}	(307)	Output High Breakdown Voltage	16.5	16.5	16.5	V min.	I_{MAX} = 4 mA, V_{IN} = 5.0V
I_{CEX}	(307)	Output High Leakage Current	25	25	25	μA max.	V_{CEX} = 16V, V_{IN} = 5.0V
I_{CC}	(306) (307)	Supply Current	28 18	34 23	40 28	mA max.	V_{IN} = 6.5V, one input per gate; V_{IN} = 1.5V, all other inputs
t_{PDHL}		Propagation Delay, Output High to Low Transition	100	100	100	nsec max.	Input pulse = 10V, $t_r = t_f \leq 10$ nsec F.O. = 0 to 10, 50% to 50% (5.6K pullup resistor on 307)
t_{PDLH}		Propagation Delay, Output Low to High Transition	600	600	600	nsec max.	Input pulse = 10V, $t_r = t_f \leq 10$ nsec F.O. = 0 to 10, 50% to 50% (5.6K pullup resistor on 307)

Note: Exceeding the absolute maximum ratings may cause permanent damage. Function of HiNIL devices at the absolute maximum ratings or beyond the conditions guaranteed is not implied.

TSC311/312/313
Flip Flops
- Master/Slave RST
- Dual J-K Edge Triggered
- Dual J-K Master/Slave

Features

311

- NOT EDGE-SENSITIVE
- DIRECT SET AND RESET INPUTS
- SIX DATA INPUTS
- SEPARATE CLOCK INPUTS ALLOW TWO-PHASE OPERATION

312/313

- CAN BE SET OR RESET WITH CLOCK HIGH OR LOW
- CLOCK INPUTS ARE ONLY 1 UNIT LOAD
- J-K OR S-R OPERATION (313 J-K MASTER/SLAVE)
- FAST—5 MHz TYPICAL TOGGLE RATE
- EDGE-SENSITIVE OPERATION (ON 312)
- NON-EDGE SENSITIVE OPERATION (ON 313)

General Descriptions

311

The 311 is a clocked master/slave flip-flop that can operate in set-reset or J-K modes. Applications flexibility is increased by three data inputs to each side of the master flip-flop and by two clock inputs. It provides three S-R inputs, or two J-K inputs, and operates single-phase or two-phase.

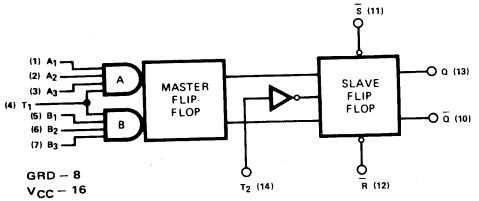
312/313

The 312/313 provides two fast, edge-triggered flip-flops in a single package. Separate logic inputs allow them to be used independently as J-K or set-reset flip-flops. Clock inputs present only 1 unit load.

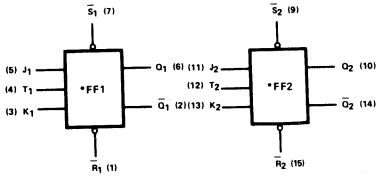
For use in new designs, the non-edge sensitive 313 is recommended.

Logic Diagrams

311



312/313



On 313 FF1 and FF2 are master/slave flip-flops.

Truth Tables

J-K MODE

J	K	Q^{n+1}
L	L	Q^n
L	H	L
H	L	H
H	H	$\bar{Q}^n$

S-R MODE

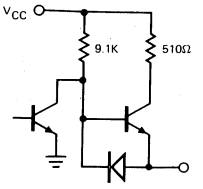
$\bar{S}$	$\bar{R}$	Q
H	H	X
H	L	L
L	H	H
L	L	H

X = Indeterminate state

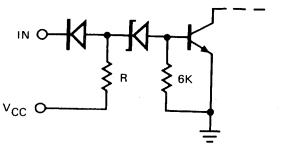
14

Equivalent Circuits

TYPICAL OUTPUT



TYPICAL INPUT



R = 8.2K ON A, B, $\overline{S}$, $\overline{R}$, T_2
R = 4.1K ON T_1.

Specifications

311

I_{CC} (WORST-CASE)	18 mA @ 13V, 25 mA @ 16V			
t_{PD} I/O FUNCTION FOR t_{PD}	820 ns T–Q+	610 ns T–Q–	400 ns $\overline{R}$–Q+	250 ns $\overline{R}$–Q–

TYPICAL TOGGLE RATE is 2 MHz

312,313

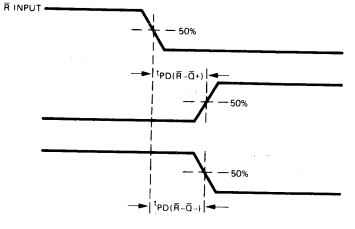
I_{CC} (WORST-CASE)	30 mA @13V, 40 mA @16V			
t_{PD} I/O FUNCTION FOR t_{PD}	300 ns T–Q+	230 ns T–Q–	600 ns $\overline{R}$–Q+	320 ns $\overline{R}$–Q–

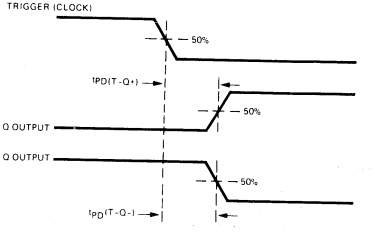
TYPICAL TOGGLE RATE IS 5 MHz

NOTE:
I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range. t_{PD} is guaranteed at V_{CC} ±1V and across the applicable temp range with the output loaded with 6 unit loads.

See page 12 for electrical summary data.

Switching Time Waveforms





NOTE:
J and K are tied to V_{CC}.

Loading Tables

311

PINS	FUNCTION	LOADING
A,B	Data inputs	1 UL
T_1	Clock input	2 UL
T_2	Clock input	1 UL
$\overline{S}$,$\overline{R}$	Direct $\overline{S}$-$\overline{R}$ inputs	1 UL
Q,$\overline{Q}$	Outputs	6 UL

312

PINS	FUNCTION	LOADING
J,K	J-K inputs	1 UL
T	Clock inputs	1 UL
$\overline{S}$,$\overline{R}$	Direct $\overline{S}$-$\overline{R}$ inputs	2 UL
Q,$\overline{Q}$	Outputs	5 UL

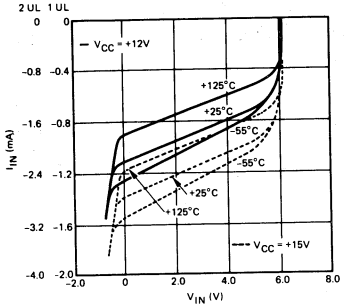
Loading Tables (contd.)

313

PINS	FUNCTION	LOADING
J,K	Data inputs	1 UL
T	Clock input	1 UL
$\overline{R},\overline{S}$	Direct Set/Reset Inputs	2 UL
Q,$\overline{Q}$	Outputs	5 UL

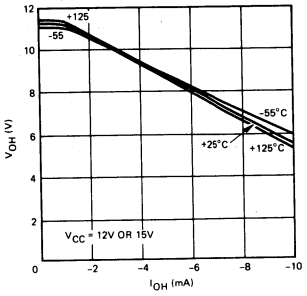
Typical Performance Characteristics

INPUT CURRENT VS. INPUT VOLTAGE

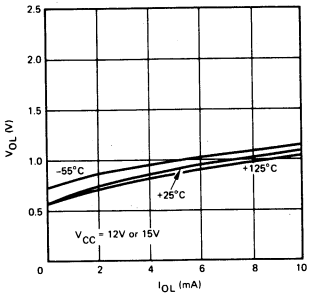


OUTPUT CURRENT VS OUTPUT VOLTAGE

OUTPUT HIGH



OUTPUT LOW



Typical Applications

311

AND gates A and B form the set and reset inputs of the master flip-flop. The slave has direct set and reset inputs that operate active low (for example, the $\overline{R}$ input is switched low while the clock is high to reset the flip-flop). Also, input T_2 has a built-in inverter to inhibit data transfer from the master to the slave when the clock is high. The T_1 and T_2 thresholds are offset as shown on the single-phase timing diagram, to ensure proper inhibition of the master and slave in the single-phase mode.

Since there are three sets of master inputs, two J and K inputs are available in the J-K connection. In either the set-reset or J-K modes, single-phase operation is obtained by connecting T_1 to T_2, or two-phase operation by applying out-of-phase clocks to T_1 and T_2.

312

The 312 triggers on the falling edge of the clock pulse, which must fall faster than 3V/microsecond for proper operation. Direct set and reset may be accomplished at any time, with the clock either high or low.

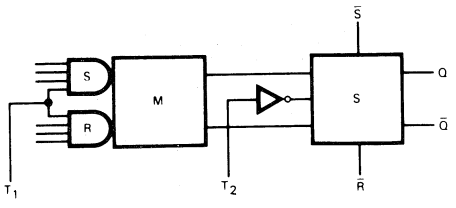
313

The 313 was developed to give the HiNIL logic designer the most flexible dual flip-flop package possible. The 313 is capable of J-K Master/Slave or S-R operation with set and reset inputs.

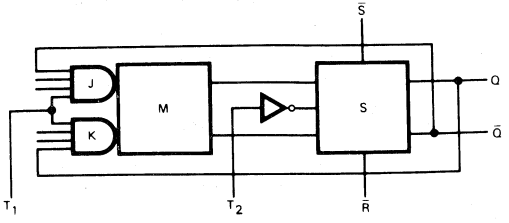
The timing diagram shown on page 28 indicates the operation sequence for J-K Master/Slave operation. The positive going edge of the clock pulse inhibits the slave and enables data transfer

311 CONFIGURATION

SET–RESET MODE

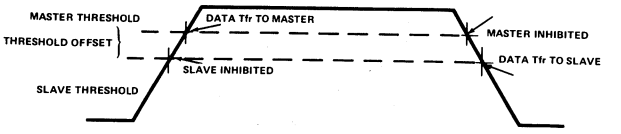


J-K MODE



14

Typical Applications (contd.)



to the master (Master/Slave thresholds are offset to ensure proper inhibition and enable). The falling edge inhibits the master and allows data transfer to the slave.

Direct set or reset may be accomplished at any time, with the clock pulse either high or low.

For reliable operation the following 313 timing recommendations should be followed. They apply across both the applicable temp range and V_{CC} spread.

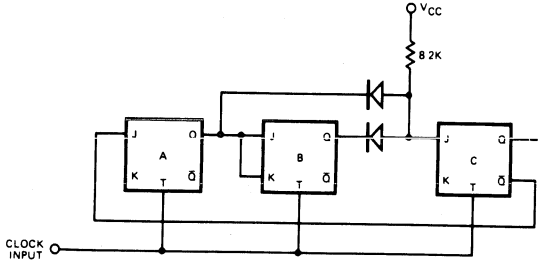
Clock Pulse Width (CP)	300 nsec min.
J-K Input Setup Time	$\geqslant$ CP
J-K Input Release Time	0 nsec min.
$\overline{S}$ or $\overline{R}$ Pulse Width	300 nsec min.
Clock Rise and Fall Time	N/A

Due to the master/slave action of the 313, data must be present during the entire time the clock is high to ensure proper data transfer to the output.

NOTE:
Because of the high noise immunity of the 312/313, it can be used in a variety of counter configurations with inexpensive diodes replacing the external gating normally required. Use IN4148 or similar high-voltage diodes or the diodes in a 331 gate expander.

312, 313 CONFIGURATIONS

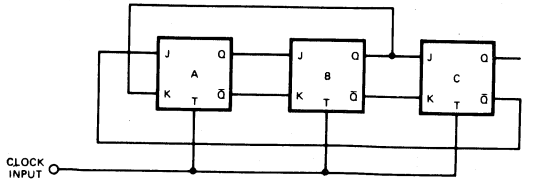
SYNCHRONOUS MOD 5, BINARY CODED OUTPUT



TRUTH TABLE

T	Q_A	Q_B	Q_C
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	0	0	0

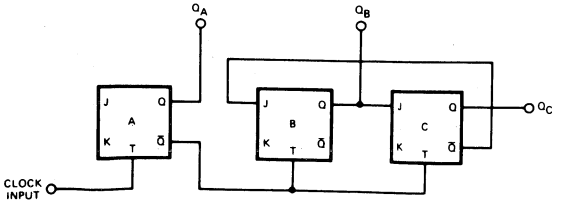
SYNCHRONOUS MOD 5, SHIFT MODE



TRUTH TABLE

T	Q_A	Q_B	Q_C
0	0	0	0
1	1	0	0
2	1	1	0
3	0	1	1
4	0	0	1
5	0	0	0

MOD 6, BINARY CODED OUTPUT

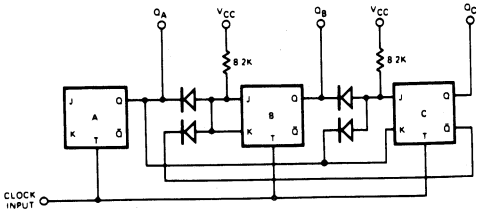


TRUTH TABLE

T	Q_A	Q_B	Q_C
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	0	0

Typical Applications (contd.)

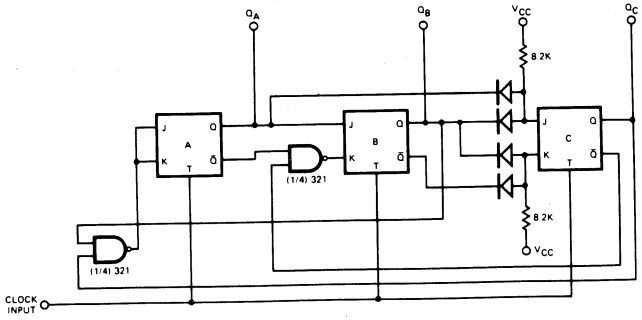
SYNCHRONOUS MOD 6, BINARY CODED OUTPUT



TRUTH TABLE

T	Q_A	Q_B	Q_C
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	0	0

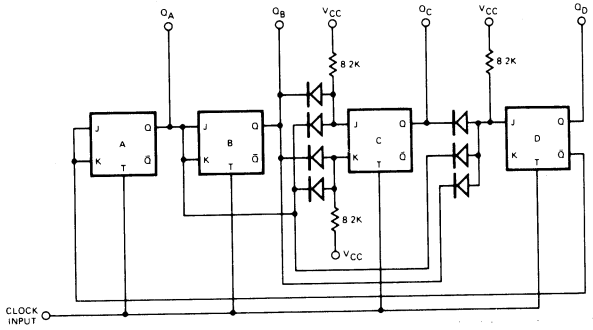
SYNCHRONOUS MOD 7, BINARY CODED OUTPUT



TRUTH TABLE

T	Q_A	Q_B	Q_C
0	0	0	0
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	1	1
7	0	0	0

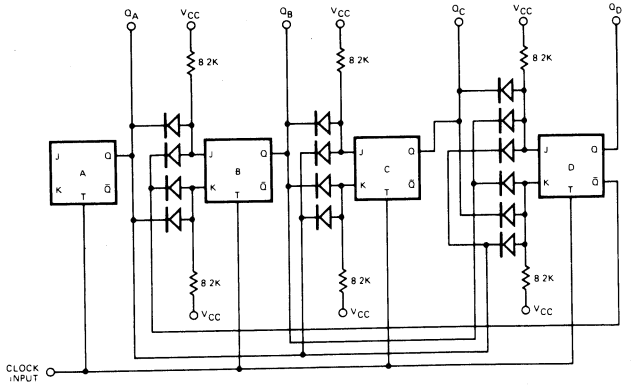
SYNCHRONOUS MOD 9, BINARY CODED OUTPUT



TRUTH TABLE

T	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	0	0	0	0

SYNCHRONOUS BCD DECADE COUNTER



TRUTH TABLE

T	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	0	0	0

14

TELEDYNE SEMICONDUCTOR

TSC321/322/323/324
NAND Gates
- Quad 2-Input (Active Pullup)
- Dual 5-Input (Active Pullup)
- Quad 2-Input (Open Collector)
- Quad 2-Input (Passive Pullup)

Features

321/322

- IDEAL FOR DRIVING LINES UP TO 10 FEET
- 5mA DRIVE CURRENT IN "1" STATE
- EXPANDER INPUTS
- ACTIVE PULLUP

323/324

- COLLECTOR OR'ABLE
- EXPANDER INPUTS
- 323 SINKS UP TO 11.5 mA (C TYPE) OR 14.0 mA (A TYPE)
- 323 OUTPUT LEVELS ADJUSTABLE TO DTL, TTL OR MOS LEVELS
- 324 HAS PULLUP RESISTORS ON CHIP
- 324 SINKS UP TO 16.8 mA (C TYPE) OR 20.8 mA (A TYPE)

General Descriptions

321/322

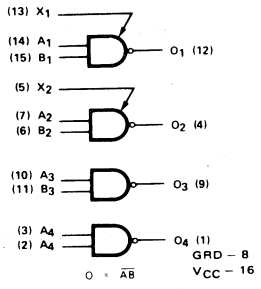
The 321 and 322 are expandable gates with active pullup outputs. Their 5 mA drive currents allow them to drive moderately long lines with no loss of noise immunity.

323/324

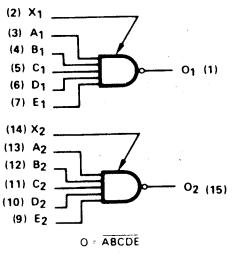
The 323 and 324 are expandable NAND gates for applications such as "wire-OR" logic systems and interfaces with other logic families. Two gates in each package have expander inputs. The 323 is used with an external pullup resistor while the 324 has pullup resistors on the chip.

Logic Diagrams

321, 323, 324

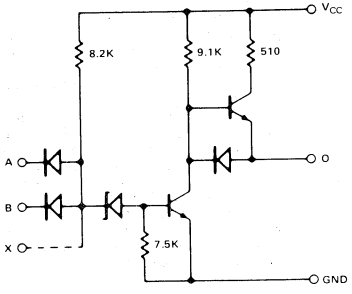


322

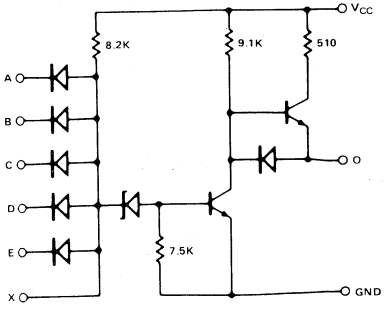


Equivalent Circuits

321



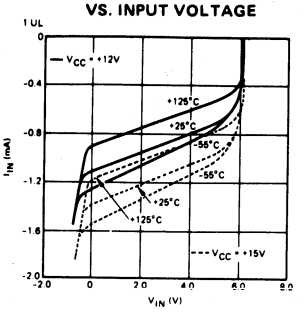
322



14

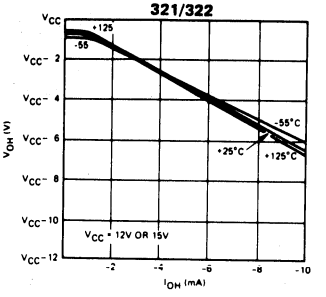
Typical Performance Characteristics

INPUT CURRENT VS. INPUT VOLTAGE

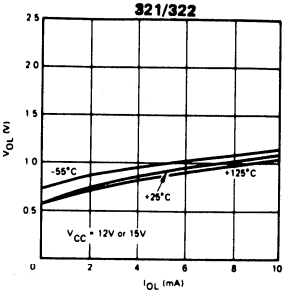


OUTPUT CURRENT VS OUTPUT VOLTAGE

OUTPUT HIGH 321/322

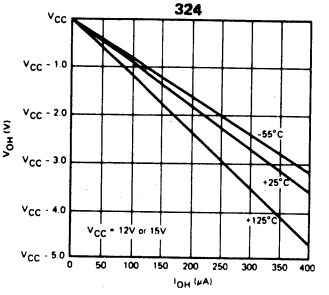


OUTPUT LOW 321/322

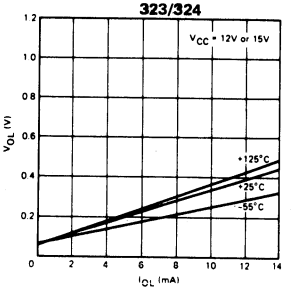


OUTPUT CURRENT VS OUTPUT VOLTAGE

OUTPUT HIGH 324



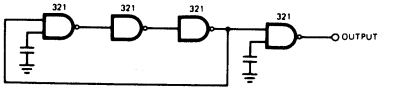
OUTPUT LOW 323/324



Typical Applications

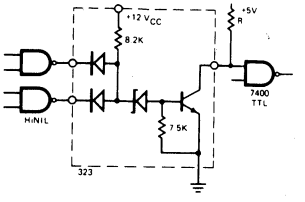
Rules for selecting external resistors and calculating fanout with collectors OR'd are given in the applications notes. The external resistor of the 323 may be connected to a voltage other than V_{CC} to adjust the output voltage level. The expandable gates may be provided any number of inputs by adding 331 gate expanders or 1N914 diodes (or any 20-volt silicon diodes) to the expander inputs.

FREE-RUNNING MULTIVIBRATOR



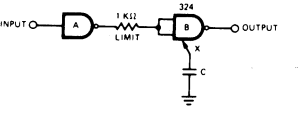
This self-starting circuit even works without capacitors.
PW ≅ 1.5 μsec. f ≅ 3MHz.

TTL INTERFACE



Choose the value of pullup resistor R by the rules given in the applications notes, with V_{CC} = 5V.

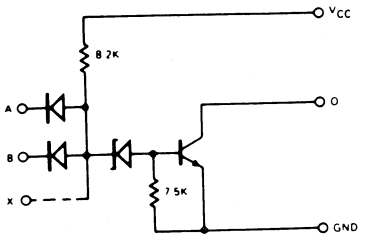
SYSTEM MONITOR



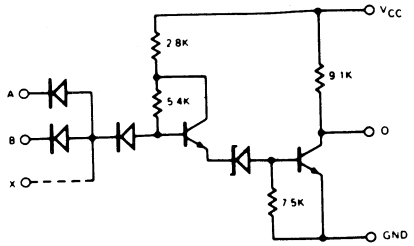
This circuit is used in applications such as detecting presence of data on a normally quiet line, or detecting malfunctions represented by an absence of pulses on a normally active line. A steady succession of pulses at the input holds the output high, but the output goes low if the input remains low for longer than a minimum time established by the value of C. A high input allows C to discharge, switching gate B to a high output. However, a low input causes C to charge at a rate t = C (8.2K) where 8.2K is B's input resistor (internal). For B's output to switch to low, the input to gate A must go low long enough for C to charge above the threshold of gate B. Any new input pulse retriggers the circuit and switches the output to high.

Equivalent Circuits (contd.)

323



324



Specifications

321

I_{CC} (WORST-CASE)	15 mA @ 13V, 20 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	200 ns A+O−	300 ns A−O+

322

I_{CC} (WORST-CASE)	8 mA @ 13V, 11 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	190 ns A+O−	550 ns A−O+

323

I_{CC} (WORST-CASE)	5.5 mA @ 13V, 8 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	160 ns A+O−	400 ns A−O+

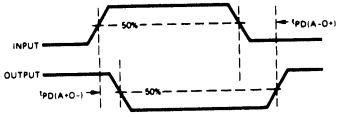
324

I_{CC} (WORST-CASE)	28 mA @ 13V, 40 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	200 ns A+O−	600 ns A−O+

NOTE:
I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range. t_{PD} is guaranteed at V_{CC} ±1V and across the applicable temp range with the output loaded with 5 unit loads.

See page 12 for electrical summary data.

Switching Time Waveform



Loading Table

PINS	FUNCTION	LOADING
A, B, A-E	Input	1 UL
X	Expanders	Each diode tied to X_1 or X_2 is 1 unit load
0	Outputs	5 UL (321, 322, 324) 7 UL (324 with supplemental 10 kΩ pullup resistor)

323 also handles 4 TTL loads at 400 mV.

TSC325/326
NAND Gates
- 2, 2, 3, 3-Input (Active Pullup)
- 2, 2, 3, 3-Input (Passive Pullup)

Features

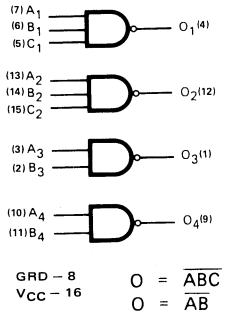
- VERSATILE CONFIGURATION
- ACTIVE PULLUP ON 325 OUTPUTS
- 5 mA DRIVE CURRENT IN "1" STATE MAKES 325 IDEAL FOR DRIVING LINES UP TO 10 FEET
- 326 OUTPUTS ARE COLLECTOR OR'ABLE

General Description

The 325 and 326 each contain two 2-input gates and two 3-input gates. The active pullup and 5 mA output drive current of the 325 allow it to drive moderately long lines with no loss of noise immunity. The 326 has passive pullup resistors on the chip, so that outputs may be collector OR'd.

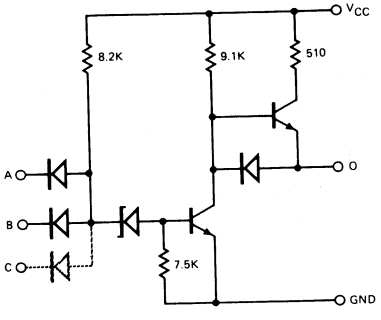
Logic Diagram

325/326

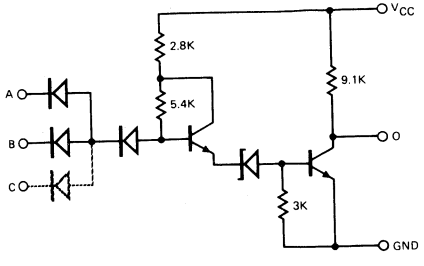


Equivalent Circuits

325



326



14

Specifications

325

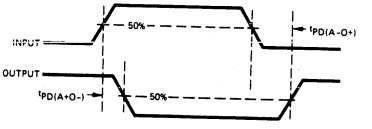
I_{CC} (WORST-CASE)	15 mA @ 13V, 20 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	200 ns A+O–	300 ns A–O+

326

I_{CC} (WORST-CASE)	28 mA @ 13V, 40 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	200 ns A+O–	600 ns A–O+

NOTE:
I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range. t_{PD} is guaranteed at V_{CC} ±1V and across the applicable temp range with the output loaded with 5 unit loads.
See page 12 for electrical summary data.

Switching Time Waveforms



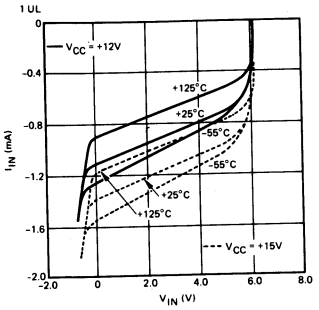
Loading Table

325/326

PINS	FUNCTION	LOADING
A-C 0	Inputs Outputs	1 UL 5 UL 7 UL (326 with supplemental 10KΩ pullup resistor

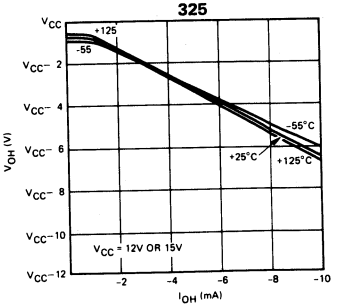
Typical Performance Characteristics

INPUT CURRENT VS. INPUT VOLTAGE

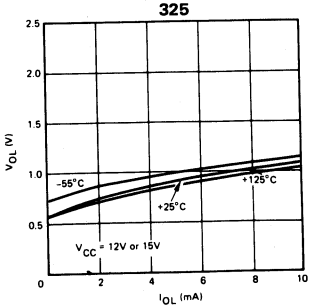


OUTPUT CURRENT VS OUTPUT VOLTAGE

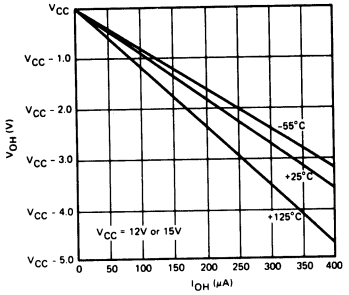
OUTPUT HIGH 325



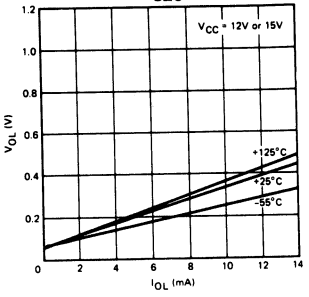
OUTPUT LOW 325



OUTPUT HIGH 326



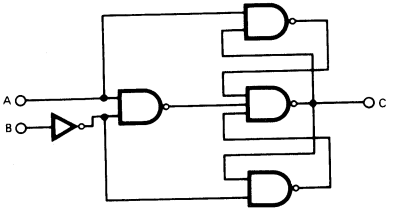
OUTPUT LOW 326



Typical Applications

See applications notes for instructions on selecting external resistors and collector OR'ing passive pullup outputs.

DIGITAL DIFFERENTIAL LINE RECEIVER

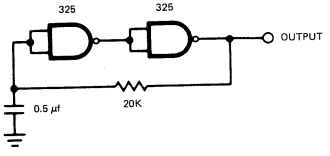


TRUTH TABLE

A	B	C
0	0	N.C.
0	1	0
1	0	1
1	1	N.C.

This circuit accepts only complementary input signals. Any noise common to A and B is rejected, providing additional noise immunity.

POWER-UP RESET CIRCUIT



The output goes low briefly when power is first applied, then remains normally high. Use this circuit, for example, to generate a flip-flop reset pulse in systems that must start up at zero.

14

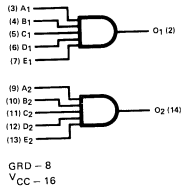
Features

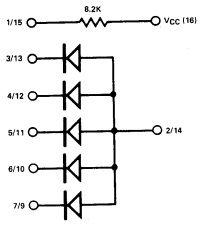
- PROVIDES 5 ADDITIONAL INPUTS TO EXPANDABLE GATES, BUFFERS AND OTHER HiNIL DEVICES
- OPTIONAL PULLUP RESISTORS FOR SECOND-LEVEL GATING

General Description

The 331 contains a diode array with the proper characteristics for use on the expander inputs of HiNIL logic devices. In addition, the chip provides two pullup resistors that allow each diode array to be used as a second-level AND gate.

Logic and Schematic Diagrams





Specifications

331

I_{CC} (WORST-CASE)	4.2 mA @ 13V, 5.2 mA @ 16V

NOTE:
I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range.
See page 12 for electrical summary data.

Loading Table

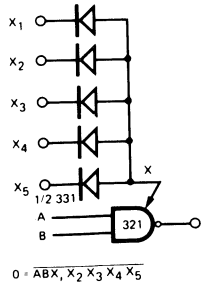
331

PINS	FUNCTION	LOADING
A-E	Inputs	1 UL
0	Outputs	

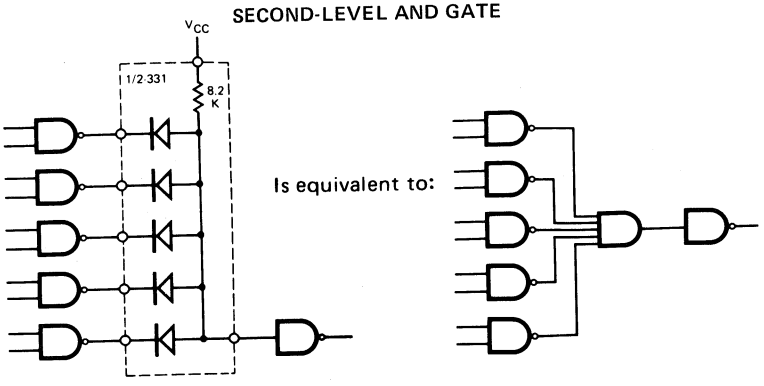
Typical Applications

Each diode presents one unit load to a HiNIL expander input. When used as a second-level gate, the output is connected through the pullup resistor to V_{CC}. Active devices are not used to restore logic levels in second-level gating applications. Instead, the first-level gate's high noise immunity overcomes the drop.

GATE EXPANSION



SECOND-LEVEL AND GATE



TELEDYNE SEMICONDUCTOR

TSC332/333/334/335
Hex Inverter Gates
- 4-Inverter, 2-NAND (Open Collector)
- 4-Inverter, 2-NAND (Passive Pullup)
- Strobed Hex NAND (Open Collector)
- Strobed Hex NAND (Passive Pullup)

Features

332/333/334/335

- FOUR INVERTERS AND TWO GATES IN 332/333
- COLLECTOR OR'ABLE
- 332 SINKS UP TO 16 mA AT 12V and 20 mA AT 15V
- 332/334 OUTPUT LEVELS ADJUSTABLE TO DTL, TTL OR MOS LEVELS
- 333/335 HAS PULLUP RESISTORS ON CHIP

General Description

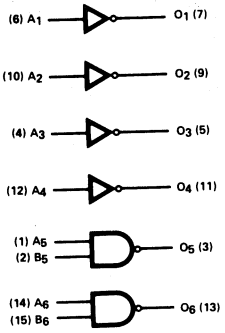
332/333/334/335

The 332 and 333 provide four inverters and two 2-input NAND gates for applications such as "wire-OR" logic systems and interfaces with other logic families. The 332 is used with an external pullup resistor while the 333 has pullup resistors on the chip.

The 334 and 335 contain six 2-input NAND gates connected such that two gates share one strobe input and four gates share another strobe input. The configuration is ideal for applications such as transferring data in parallel from one register to another. The devices may also be used in "wire-OR" logic systems and for the interfaces with other logic families.

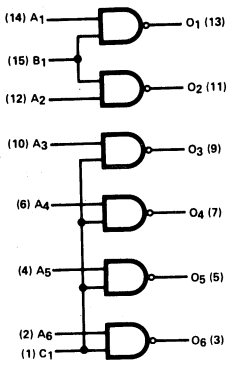
Logic Diagram

332/333



GRD – 8
V_{CC} – 16

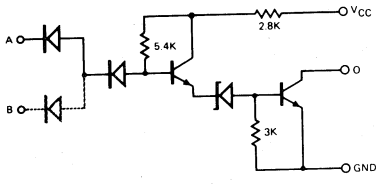
334/335



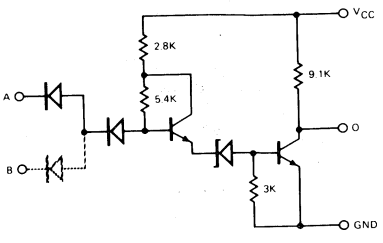
GRD – 8
V_{CC} – 16

Equivalent Circuits

332/334



333/335



14

Specifications

332/334

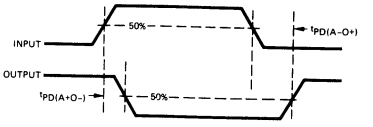
I_{CC} (WORST-CASE)	28 mA @ 13V, 42 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	140 ns A+O−	350 ns A−O+

333/335

I_{CC} (WORST-CASE)	42 mA @ 13V, 60 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	140 ns A+O−	350 ns A−O−

NOTE:
I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range.
t_{PD} is guaranteed at V_{CC} ±1V and across the applicable temp rage with the output loaded with 5 unit loads.
See page 12 for electrical summary data.

Switching Time Waveforms



Loading Tables

332/333

PINS	FUNCTION	LOADING
A,B	Inputs	1 UL
0	Outputs	5 UL (333) 7 UL (332 with 5 KΩ pullup resistor) 7 UL (333 with 10 KΩ supplemental pullup resistor)

332 also handles 4 TTL loads at 400 mV

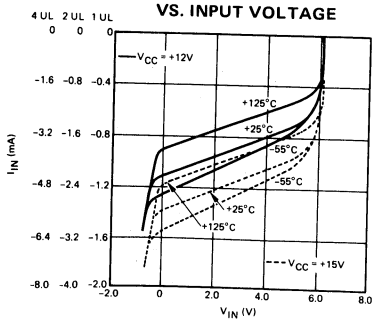
334/335

PINS	FUNCTION	LOADING
A	Data Inputs	1 UL
B	Strobe Input	2 UL
C	Strobe Input	4 UL
O	Outputs	5 UL (335) 7 UL (334 with 5 KΩ pullup resistor) 7 UL (335 with 10 KΩ supplemental pullup resistor)

334 also handles 4 TTL loads at 400 mV

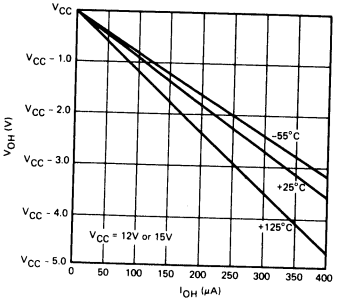
Typical Performance Characteristics

INPUT CURRENT VS. INPUT VOLTAGE



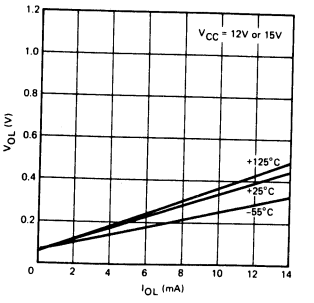
OUTPUT CURRENT VS OUTPUT VOLTAGE

OUTPUT HIGH*



*333, 335 only

OUTPUT LOW

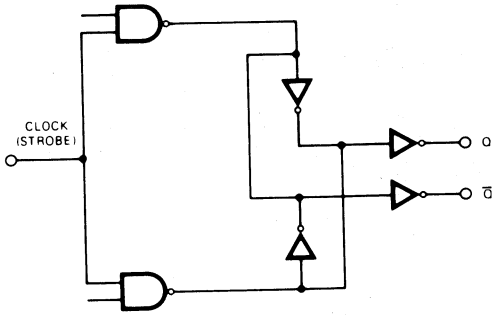


Typical Applications

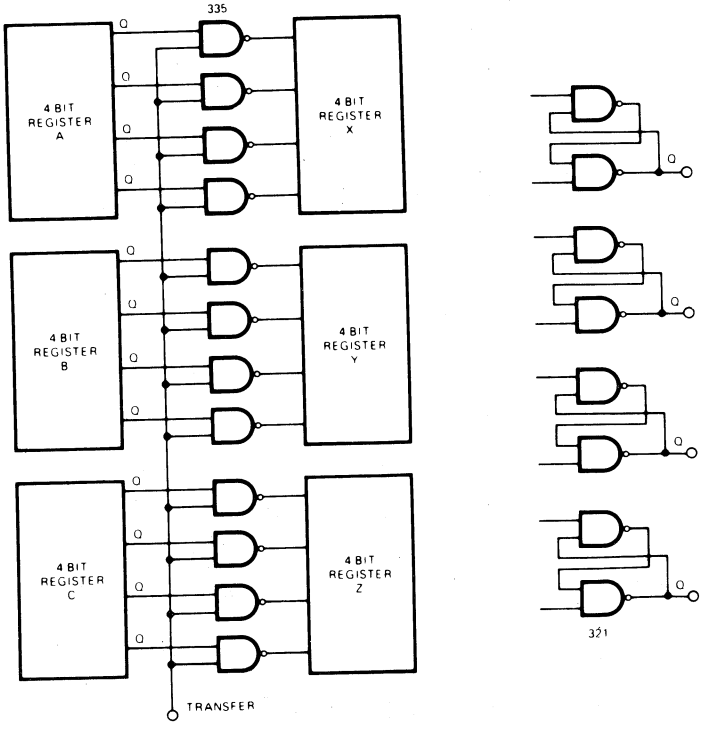
Rules for selecting external resistors and calculating fanout with collectors OR'd are given in the applications notes. The external resistor of the 332 or 334 may be connected to a voltage other than V_{CC} to adjust the output voltage level. To use the NAND gates as inverters, the A and B inputs may both be connected to the same input data line, or one input may be connected to V_{CC}.

For transfer of data, the strobe input is held high. Data on the A inputs of those gates will appear inverted on the outputs. When the strobe input is low, the outputs remain high. If the two strobe inputs are connected, six lines of data may be transferred with one strobe control (presenting 6 unit loads).

CLOCKED S-R FLIP-FLOP WITH BUFFERED OUTPUTS



PARALLEL TRANSFER OF DATA

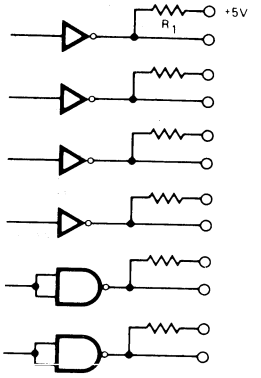


Two 335 strobed hex inverters transfer 12 lines in parallel from register A, B and C to register X, Y and Z when the strobe input (transfer line is momentarily taken high. The data inversion during transfer is circumvented by using the $\overline{Q}$ outputs of registers A, B and C. Each of these registers may be made with a pair of 321 quad NAND gates.

14

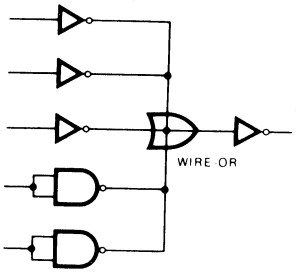
Typical Applications (contd.)

TTL INTERFACE
332

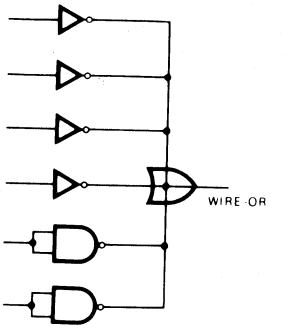


This type of interface will protect TTL data processing systems from electromechanical noise generated in peripherals. The value of R is selected by the rules given in the applications notes, except that pullup is to 5V rather than 12V or 15V V_{CC}.

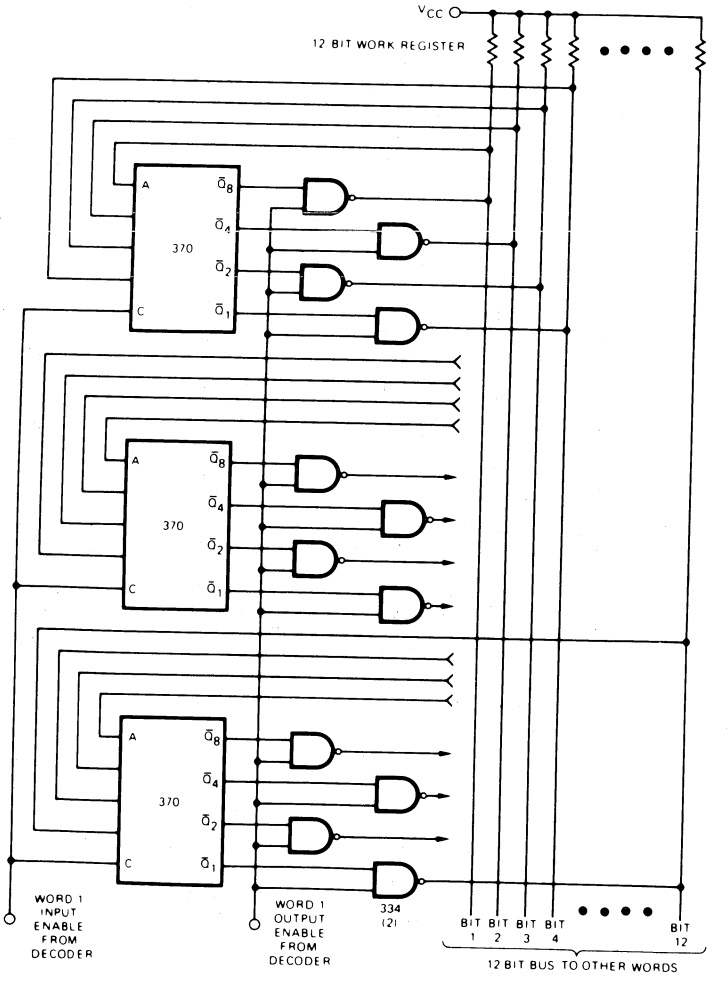
FIVE-INPUT OR GATE
332/333



SIX-INPUT OR GATE
332/333



BIDIRECTIONAL BUSING (MEMORY SYSTEM EXAMPLE)



TSC341
Multi-Function Gates
- Dual 2-Wide, 2-Input AND-OR-Invert
- Dual Expandable AND-NOR

Features

341

- PROVIDES COMPLEX FUNCTION WITH LOW SUPPLY DRAIN
- EXPANDABLE INPUTS
- ACTIVE PULLUP

344

- ALLOWS COMBINATION OF COLLECTOR OR'ING AND ACTIVE OUTPUT DESIGN
- COLLECTOR OR'ABLE WITH OTHER OPEN COLLECTOR GATES

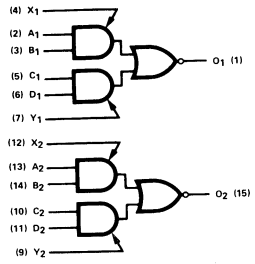
General Descriptions

341

The 341 is an expandable gate with active pullup outputs. It is used in applications such as comparing two binary numbers. Large numbers may be compared by using the expander inputs.

Logic Diagrams

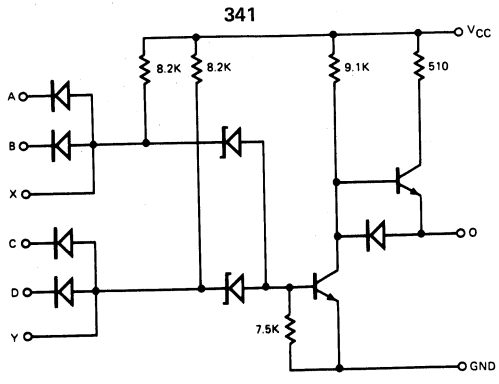
341



$O = \overline{AB \& CD}$ GRD – 8
V_{CC} – 16

Equivalent Circuit

341



Equivalent Circuits (contd.)

Specifications

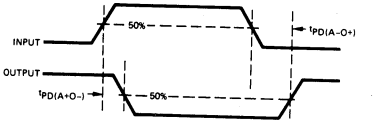
341

I_{CC} (WORST-CASE)	11 mA @ 13V, 15 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	150 ns A+O−	410 ns A−O+

NOTE:
I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range. t_{PD} is guaranteed at V_{CC} ±1V and across the applicable temp range with the output loaded with 5 unit loads.

See page 12 for electrical summary data.

Switching Time Waveforms



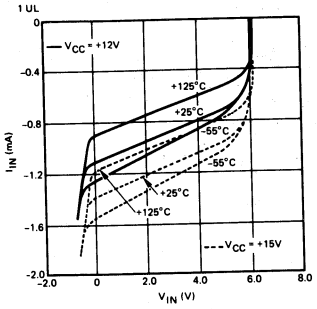
Loading Tables

341

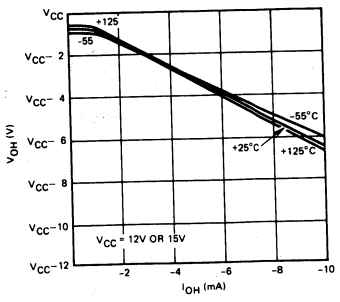
PINS	FUNCTION	LOADING
A-D	Inputs	1 UL
X	Expanders	Each diode tied to X_1 or X_2 is 1 unit load
0	Outputs	5 UL

Typical Performance Characteristics

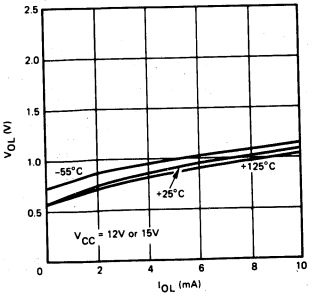
INPUT CURRENT VS. INPUT VOLTAGE



OUTPUT CURRENT VS OUTPUT VOLTAGE
OUTPUT HIGH

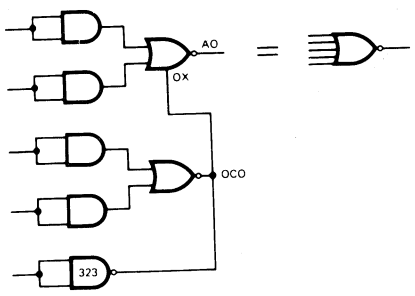


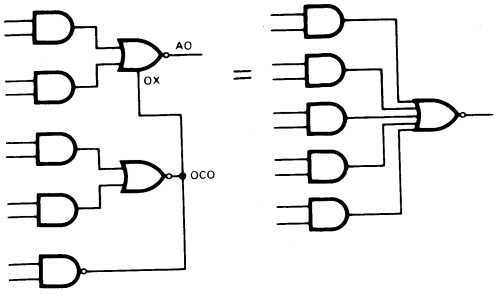
OUTPUT LOW

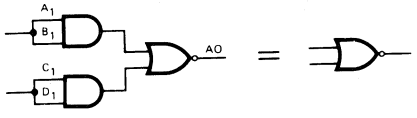


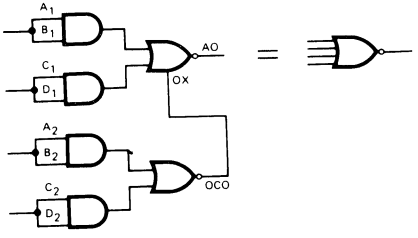
Typical Applications

The number of inputs to each gate may be increased to any desired number of adding 331 gate expanders or 1N4148 diodes (or any 20-volt silicon diode) to the expander inputs.





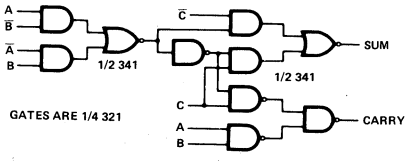




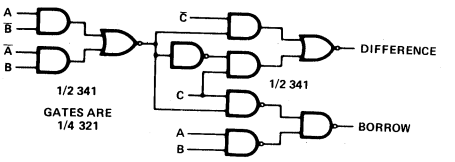
14

Typical Applications (contd.)

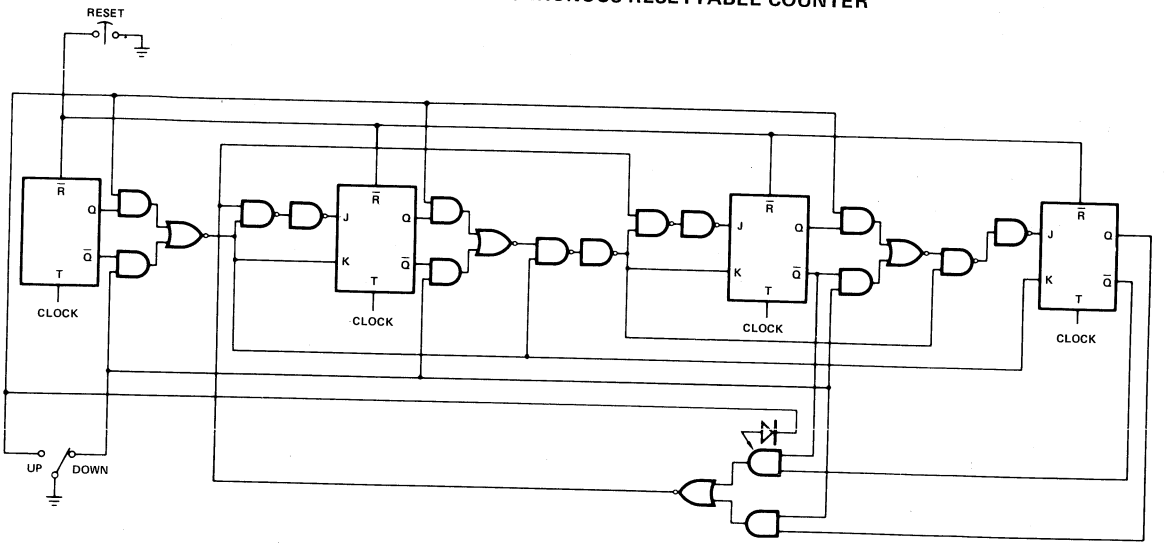
FULL ADDER



SUBTRACTOR



UP-DOWN BCD SYNCHRONOUS RESETTABLE COUNTER



This circuit requires only two 312, two 321 and two 341 packages, plus a 1N914 diode.

TSC342
Dual Monostable Multivibrator

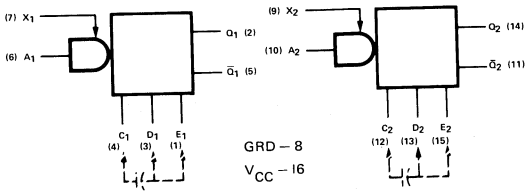
Features

- COMPLEMENTARY OUTPUT PULSES
- OUTPUT WIDTH INDEPENDENT OF TRIGGER PULSE WIDTH
- TIMING RANGE OF 100 NANOSECONDS TO SEVERAL SECONDS
- ON CHIP TIMING RESISTORS
- EXPANDER INPUTS
- ACTIVE PULLUP

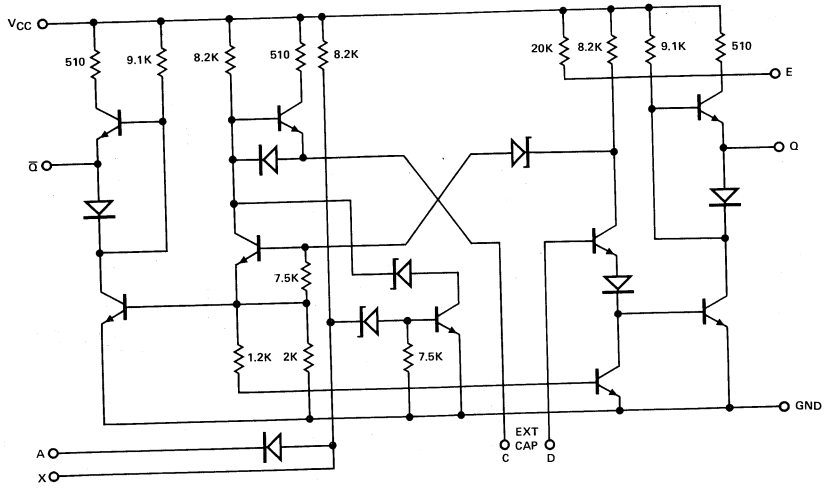
General Description

The 342 provides two one-shots that can be independently triggered and timed. Output pulse widths are timed by an external capacitor, making them independent of the input trigger pulse widths. Expander inputs and complementary, active pull-up outputs are provided. Applications include generation of stable control pulses as long as several seconds from short data pulses.

Logic Diagrams



Equivalent Circuit



14

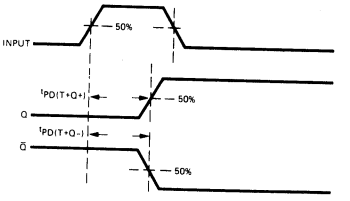
Specifications

342

I_{CC} (WORST-CASE)	17 mA @ 13V, 23 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	260 ns t+Q+	160 ns t+$\overline{Q}$–

NOTE:
I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and +16 for A type) and is guaranteed across the applicable temp range.
t_{PD} is guaranteed at V_{CC} ±1V and across the applicable temp range with the output loaded with 5 unit loads.
See page 12 for electrical summary data.

Switching Time Waveforms



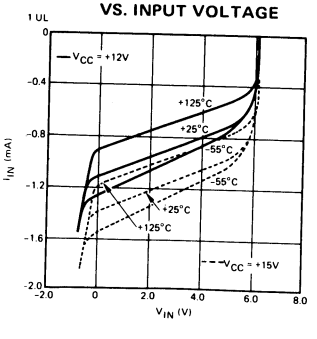
Loading Table

342

PINS	FUNCTION	LOADING
A	Trigger inputs	1 UL
C-E	Timing network	N.A.
X	Expanders	Each diode tied to X_1 or X_2 is 1 unit load.
Q,$\overline{Q}$	Outputs	5 UL

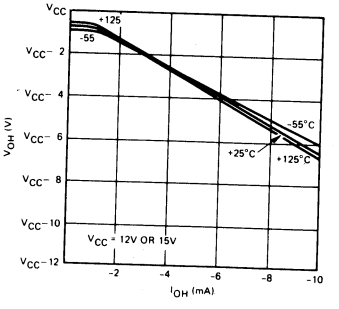
Typical Performance Characteristics

INPUT CURRENT VS. INPUT VOLTAGE

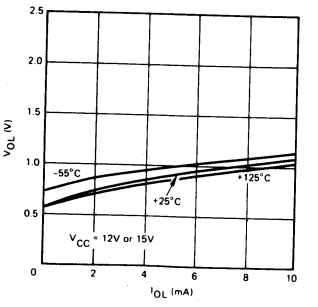


OUTPUT CURRENT VS OUTPUT VOLTAGE

OUTPUT HIGH



OUTPUT LOW



Typical Applications

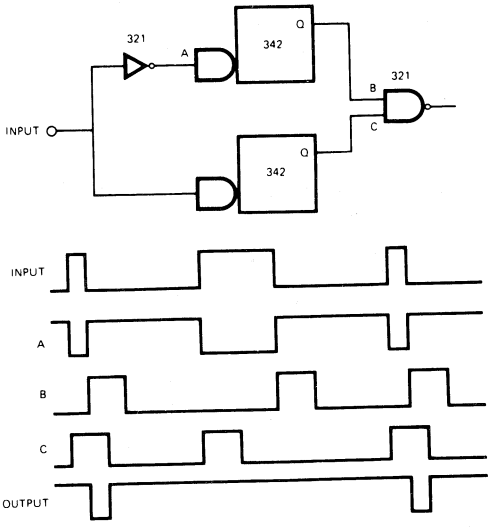
The 342 is triggered on the rising edge of a trigger pulse applied to an A or X input. It is not retriggerable until a cycle time of $P_W + T_R$ has elapsed, where P_W is output pulse width and T_R is the recovery time.

$P_W \cong 0.7$ RC. C is a capacitor externally connected between pins C and D. R may be the 20 kilohm resistor in the one-shot, used by shorting pins D and E together. This resistor is a diffused resistor with a tolerance of ±30% at 25°C. For critical timing applications, a precision resistor of 2 to 62 kilohms should be connected from V_{CC} to pin D. The external resistor size range allows a timing range from 200 nanoseconds to several seconds.

T_R = 3C in nanoseconds, with C in picofarads. This is the recovery time required for the circuit to charge C to 99% of its final value. T_R must be considered when calculating the allowable duty cycle.

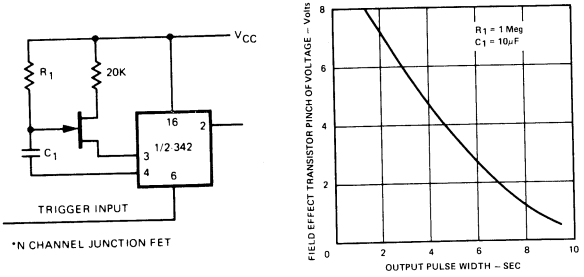
Any desired number of trigger inputs may be ANDed by adding 331 gate expanders or 1N914 diodes (or any 20-volt silicon diodes) to the expander inputs.

PULSE WIDTH DETECTOR



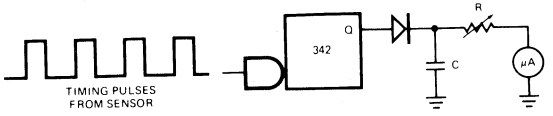
Only pulses shorter than a minimum produce an output pulse.

ONE-SHOT WITH LONG PULSE WIDTH



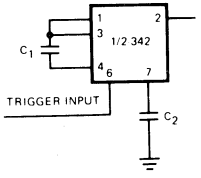
A field-effect transistor extends the time constant provided by a small capacitor, by allowing use of a high-value resistor. If a large capacitor is also used, very long delays can be obtained.

TACHOMETER

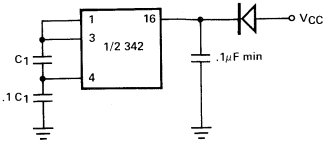


C and R determine the meter reading for a given input pulse rate. R may be used to calibrate the meter to show rpm or other rate of the equipment being monitored.

PULSE DELAY CIRCUIT



IMPROVED NOISE REDUCTION CIRCUIT



Recommended where excessive supply noise is present.

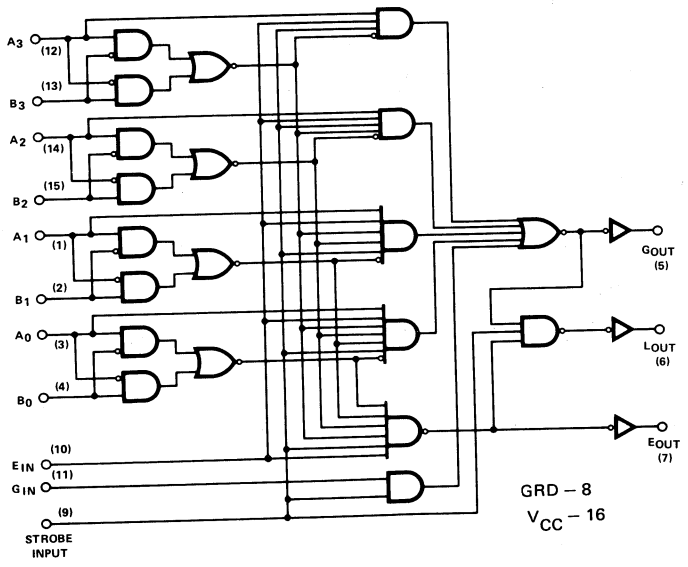
Features

- IDEAL FOR DIGITAL CONTROLS REQUIRING COMPARATORS
- CASCADES TO COMPARE LARGE BINARY OR BCD NUMBERS
- ACTIVE-HIGH OUTPUTS
- STROBE INPUT

General Description

The 343 compares two 4-bit binary numbers, A_8, A_4, A_2, A_1, and B_8, B_4, B_2, B_1. The comparison generates an active high output indicating whether A is greater than, equal to, or less than B. Longer binary numbers can be compared by operating a number of comparators in cascade. A strobe is provided to hold all outputs low.

Logic Diagram



Truth Table

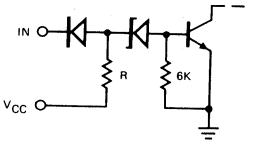
	INPUTS			OUTPUTS		
	E_{IN}	G_{IN}	STROBE	E_{OUT}	G_{OUT}	L_{OUT}
A > B	1	0	1	0	1	0
A = B	1	0	1	1	0	0
A < B	1	0	1	0	0	1
A > B	1	1	1	0	1	0
A = B	1	1	1	1	1	0
A < B	1	1	1	0	1	0
A > B	0	1	1	0	1	0
A = B	0	1	1	0	1	0
A < B	0	1	1	0	1	0
A > B	0	0	1	0	0	1
A = B	0	0	1	0	0	1
A < B	0	0	1	0	0	1

NOTE: If the device is being used correctly E_{IN} and G_{IN} will never be high at the same time. Whenever the strobe is low (logical "0"), all outputs will be low regardless of the input states.

14

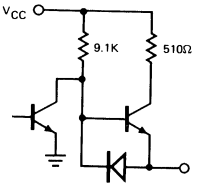
Equivalent Circuits

TYPICAL INPUT



R = 8.2K ON A,B
R = 16.4K ON G_{IN}
R = 4.1K ON E_{IN}, STROBE

TYPICAL OUTPUT



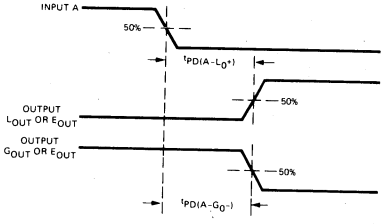
Specifications

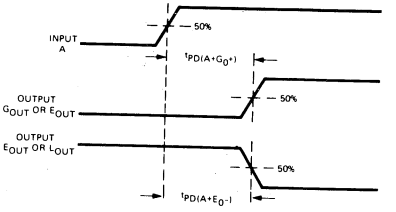
343

I_{CC} (WORST-CASE)	42 mA @ 13V, 56 mA @ 16V
t_{PD} I/O FUNCTION FOR t_{PD}	1 microsecond A+ or A– to G, E, or L+ or –

NOTE:
I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and 16V for A type) and is guaranteed across the applicable temp range. t_{PD} is guaranteed at V_{CC} ±1V and across the applicable temp range with the output loaded with 5 unit loads.

Switching Time Waveforms





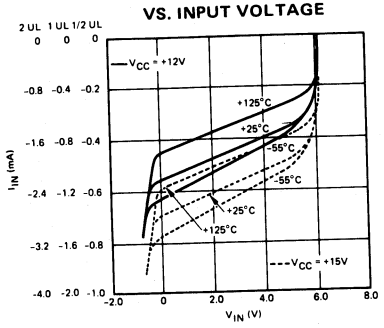
Loading Table

343

PINS	FUNCTION	LOADING
A,B	Data inputs	1 UL
E_{IN}	"Equal to" input	2 UL
G_{IN}	"Greater than" input	1 UL
Strobe	Strobe input	2 UL
E_{OUT}	"Equal to" output	5 UL
G_{OUT}	"Greater than" output	5 UL
L_{OUT}	"Less than" output	5 UL

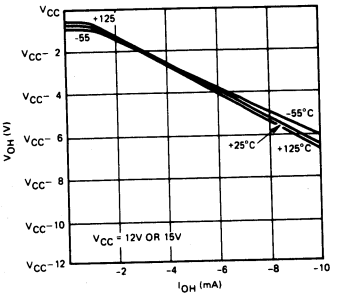
Typical Performance Characteristics

INPUT CURRENT VS. INPUT VOLTAGE

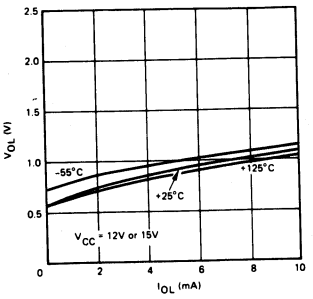


OUTPUT CURRENT VS OUTPUT VOLTAGE

OUTPUT HIGH



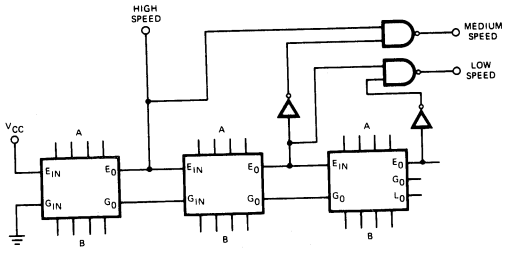
OUTPUT LOW



Typical Applications

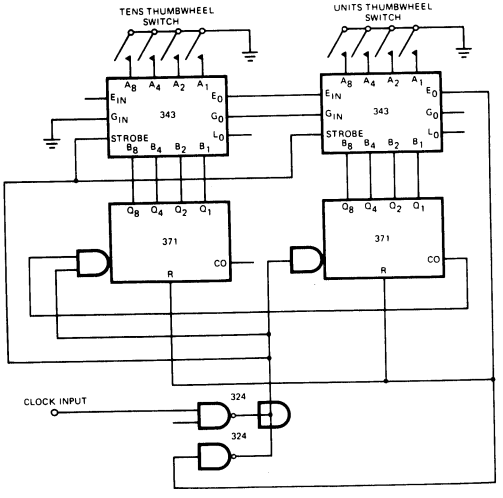
The "equal to" and "greater than" outputs can be connected to the corresponding inputs of another 343 to cascade the comparators. In this way, two binary or BCD numbers of any length can be compared. The final stage's outputs will indicate their relative magnitude. The unused "equal to" input should be left open, and the unused "greater than" input should be grounded.

SERVO OVERSHOOT CONTROL



Speed information is provided a servo positioning system by three comparators in cascade. The most significant digit of the control word is applied to the comparator at the left. If the device controlled is a long way from a new position, only the high speed output will be low. As the device approaches the new position, this output will go high and the medium speed output will go low. When the device is very close, only the low speed output will be low. This allows regulation of motor speed to limit device overshoot. The circuit shown is a simplified version that is intended only to show the general application of the 343 to servo positioning controls. The actual circuit is more involved since the possibility exists that the controlled device may be on the other side of the desired position.

MOD N COUNTER



In this example, the counter modulus is any number up to 99 set with two thumbwheel switches. When the counters reach this number, the second comparator's E_{out} resets the counters. The 343 strobe inputs are tied to the system clock to prevent the possibility of false comparisons being made when the counters are changing state.

14

TSC347
Dual Retriggerable Monostable Multivibrator

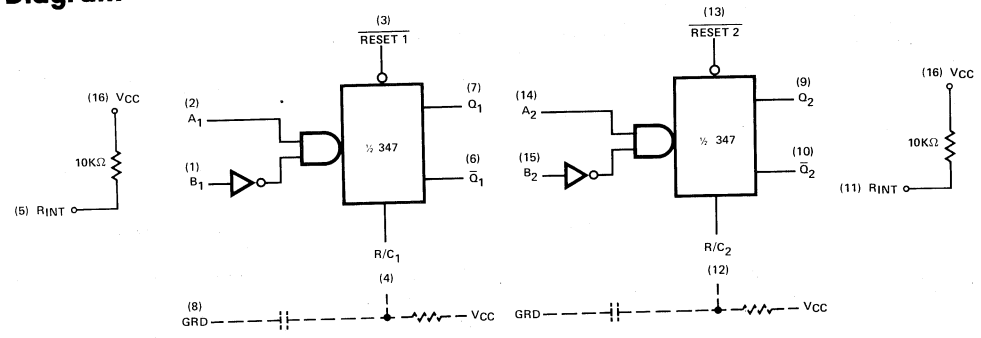
Features

- DELIVERS TIMED OUTPUT PULSES DETERMINED BY EXTERNAL COMPONENTS
- RETRIGGERABLE OPERATION
- HIGH IMMUNITY TO POWER TRANSIENTS
- ACTIVE PULLUP COMPLEMENTARY OUTPUTS
- INVERTING AND NON-INVERTING TRIGGER INPUTS
- 3.5 VOLTS (MIN) NOISE IMMUNITY

General Description

The Teledyne Semiconductor 347 Dual Retriggerable Monostable Multivibrator is a versatile monostable delivering timed output pulses when triggered. The output pulse width is determined by the RC time constant of externally connected components. For increased flexibility, provision has been made for inverting and non-inverting trigger inputs. Complementary active pullup outputs are also provided.

Logic Diagram



Equivalent Circuits

Specifications

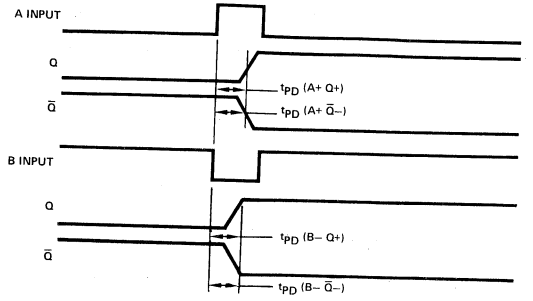
ICC (WORST CASE)	40 mA @ 13 V, 50 mA @ 16 V			
*tPD	500 ns	650 ns	650 ns	750 ns
I/O FUNCTION FOR tPD	A+ Q+	A+ Q̄−	B− Q+	B− Q̄−

*Add 30 C to these times for C ≥ .001μF

NOTE:
ICC is tested at VCC +1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temperature range. tPD is guaranteed at VCC ±1V and across applicable temperature range with the output loaded with 5 unit loads.

See page 12 for electrical summary data.

Switching Time Waveform



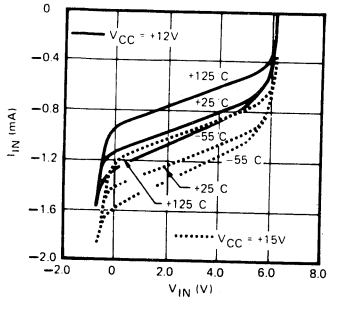
Loading Table

347

PINS	FUNCTION	LOADING
A,B	Trigger inputs	1 UL
RESET	Reset input	2 UL
Q, $\overline{Q}$	Outputs	5 UL

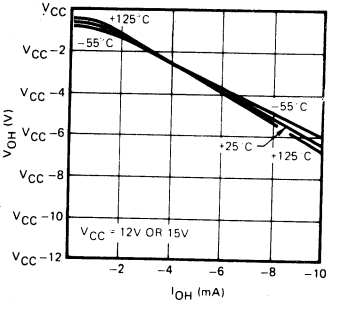
Typical Performance Characteristics

INPUT CURRENT VS. INPUT VOLTAGE

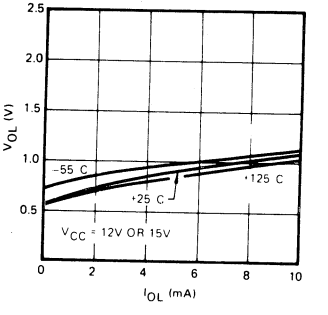


OUTPUT CURRENT VS. OUTPUT VOLTAGE

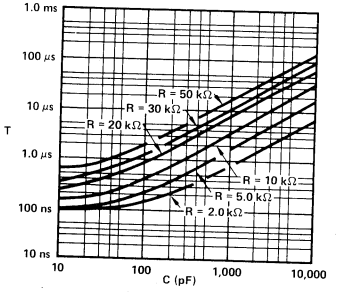
OUTPUT HIGH

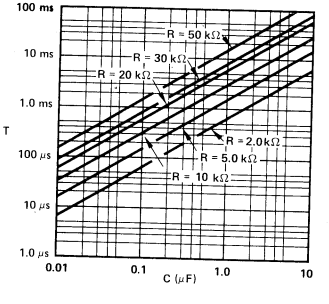


OUTPUT LOW

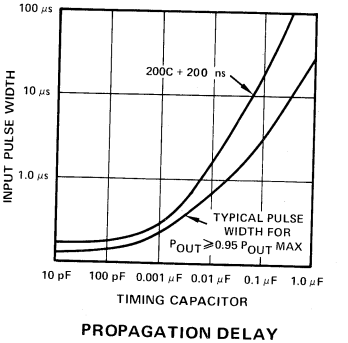


PULSE WIDTH VS. R/C VARIATION

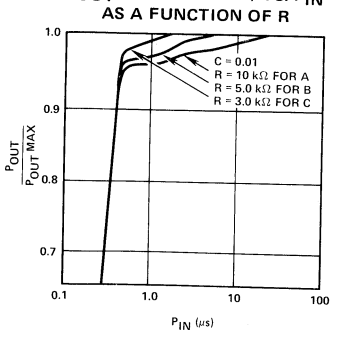




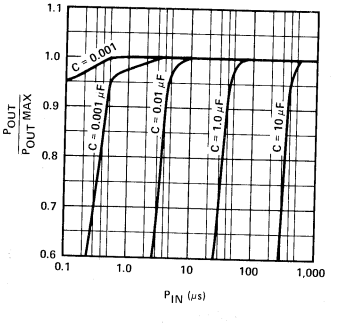
MINIMUM INPUT PULSE WIDTH VS. C



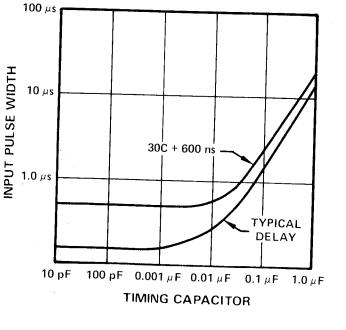
P_{OUT} (NORMALIZED) VS. P_{IN} AS A FUNCTION OF R



P_{OUT} (NORMALIZED) VS. P_{IN} AS A FUNCTION OF C



PROPAGATION DELAY VS. C



Typical Applications

FUNCTIONAL DESCRIPTION

The HiNIL 347 Dual Retriggerable Monostable Multivibrator, or more commonly a retriggerable one shot, delivers timed output pulses whose width is determined by external components. The pulse width of the output is given by $P_W \approx .31$ RC where R is the external resistor value in ohms and C is the timing capacitor value in farads.

Component limits:

$3K\Omega \leqslant R \leqslant 30K\Omega$

$0 \leqslant C \leqslant 10\mu F$

The 347 has provision for both inverting and non-inverting trigger inputs. In addition, the device is retriggerable—the output pulse can be extended by triggering the input before the output pulse is terminated simplifying the generation of output pulses of extremely long duration. The overriding RESET input permits termination of the output pulse at a predetermined time independent of the timing components R and C. The retrigger capability can be inhibited by connecting the Q output to the inverting input.

The 347 is provided with complementary active pullup outputs capable of sourcing 5 mA at 7 volts.

TIMING REQUIREMENTS

Minimum Time Required Between Input Pulses	300 ns
Minimum Input Pulse Width	$P \geqslant 200\ C + 200$ ns

DESIGNERS GUIDE

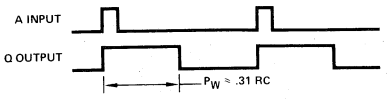
The pulse width of the output is determined by the RC time constant of externally connected components. The output pulse width is given by $P_W \approx .31$ RC.

Figures 1, 2 and 3 summarize the various I/O pulses for normal, retrigger and reset modes of operation. The retrigger capability can be inhibited by connecting the output to the inverting input.

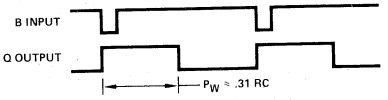
If $\overline{\text{RESET}}$ is allowed to go high while the trigger input is true (A high or B low), the device will retrigger as shown in Figure 3B.

The external resistor is connected to V_{CC} and the capacitor to ground. This configuration makes the 347 immune to power transients and overcomes false triggering tendency.

TYPICAL I/O PULSES
NORMAL ONE SHOT OPERATION ($P_W \approx .31$ RC)



NON-INVERTING TRIGGER INPUT



INVERTING TRIGGER INPUT

Figure 1

TYPICAL I/O PULSES
CONTROL UTILIZING RETRIGGER PULSE

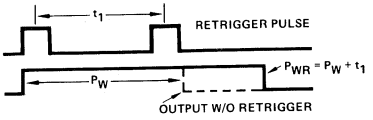


Figure 2

TYPICAL I/O PULSES
CONTROL UTILIZING RESET INPUT

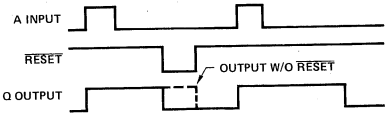


Figure 3A

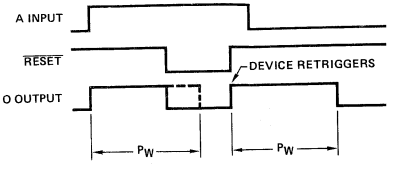


Figure 3B

14

APPLICATIONS

The circuits shown are some common one shot applications.

A. AC Line Detector

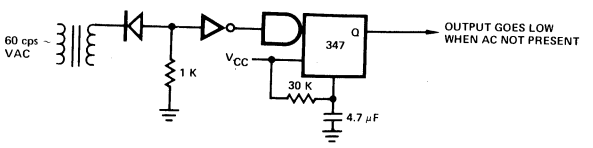
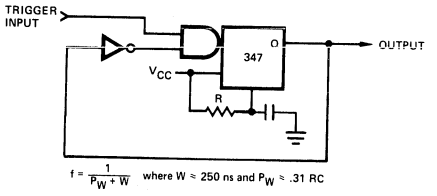
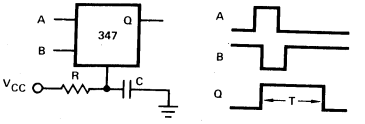


Figure A shows a method of monitoring an AC input source and generates a level to monitor the presence of the AC signals. The retrigger capability of the 347 is utilized when the output period is slightly longer than the 60 cps (or 120 or 240 cps) of the AC source. As long as the 60 cps clock is present, it re-triggers the one shot and extends the high state one more period. If the AC source goes away, no retrigger pulse will occur and the one shot will "time out" (go low) indicating loss of AC. This output could be used to initiate a counter whose output displays how long AC was not present.

B. Free-Running Multivibrator

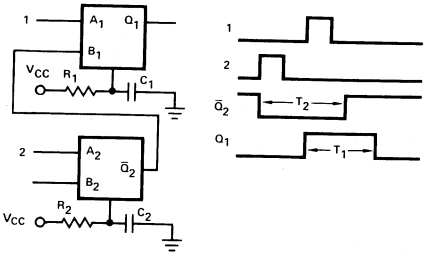


C. Coincidence Detector



If A is high at the same time B is low, an output pulse will occur. If both signals to be detected are positive-going, one must be inverted before applying it ot input B.

D. Envelope Coincidence Detector



Output Q1 occurs if input 1 is present within time, T_2, after the beginning of input 2.

An application note on the 347 is presently available and presents a detailed description of the operation of the monostable and presents additional applications data including voltage to frequency converters, frequency to voltage converters, and frequency division.

Features

Output Pulse Equals Input Pulse Plus Extension Determined By External R & C Components

Extends Positive- Or Negative-Going Pulse Inputs

Wide Power Supply Operating Voltage — 10 To 16V, CMOS Compatible

3.5 Volts (Minimum) Noise Immunity — Low Sensitivity To Power Supply Transients

Retriggerable Operation

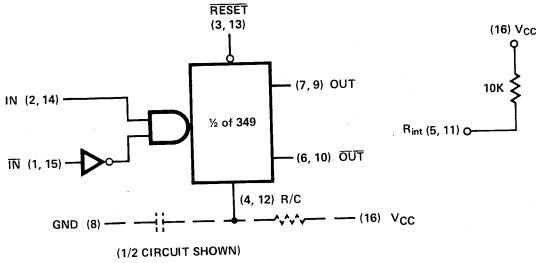
General Description

The Teledyne Semiconductor 349 Dual Retriggerable Pulse Stretcher delivers timed output pulses whose pulse width is equal to the sum of the input pulse width and a predetermined pulse extension. The pulse extension is determined by external R and C components.

The device features the characteristic 3.5 volts (minimum) noise immunity of the HiNIL family and operates over a wide 10 to 16 volt supply range, making it an ideal complement in CMOS designs.

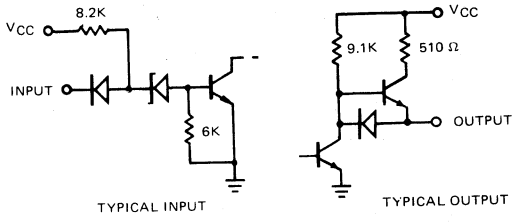
For increased design flexibility both positive and negative pulse inputs are provided. Each output is active pull-up and can source 5 mA.

Logic Diagram



(1/2 CIRCUIT SHOWN)

Equivalent Circuits



TYPICAL INPUT

TYPICAL OUTPUT

14

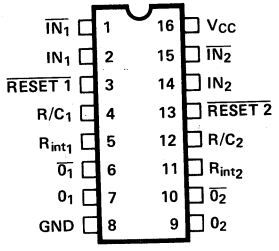
Connection Diagram

Order Part Numbers:

349AL
(V_{CC} = 15V ±1V,
$-30°C \leq T_A \leq +70°C$)

349CL
(V_{CC} = 12V ±1V,
$-30°C \leq T_A \leq +70°C$)

L Package
16 Lead Ceramic DIP



Absolute Maximum Ratings

	L Package
Continuous Supply Voltage	+16.5 V
Pulsed Supply Voltage (less than 100 ms)	+18.0 V
Input Voltage (any input)	−0.5 to + 18 V
Surge Sink Current (less than 100 ms at 25°C T_A)	20 mA
Storage Temperature	−65°C to +150°C
Lead Temperature (1/16 inch from case, 10 nsec MAX)	300°C

NOTE: Exceeding the absolute maximum ratings may cause permanent damage. Function of HiNIL devices at the absolute maximum ratings or beyond the conditions guaranteed is not implied.

Functional Description

The HiNIL 349 Dual Retriggerable Pulse Stretcher is used to extend an input pulse by a predetermined time interval whose duration is a function of external resistor and capacitor values. The pulse extension is given by $P_X = .31\ RC$ where R is the timing resistor in ohms and C is the external capacitor in farads.

Component limits:

$3K\Omega \leqslant R \leqslant 30K\Omega$

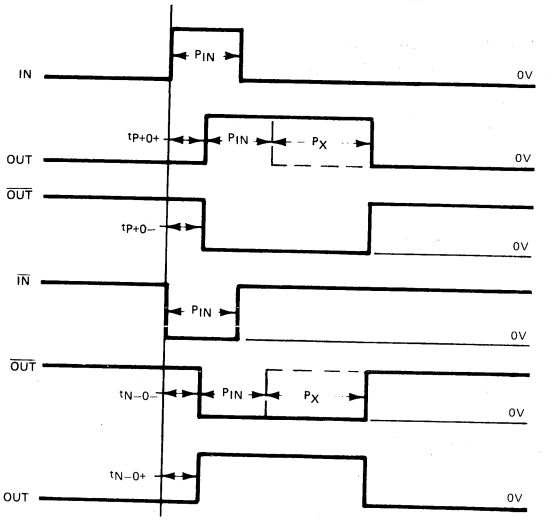
$0 \leqslant C \leqslant 10\mu F$

The 349 has provision to extend both positive and negative pulse inputs. Complementary outputs occur on the positive and negative output lines. In addition, the device can be retriggered; the output pulse can be extended by triggering the input line before the output has timed out. This allows extended time interval pulse outputs of extremely long duration.

An overriding RESET is provided to terminate the output pulse indepedent of the timing interval.

The active output configuration of the 349 is capable of sourcing 5 mA @ 7 volts.

Timing Diagrams



Loading Table

Pins	Function	Loading
In, $\overline{In}$	Input Trigger Pulse	1 U.L.
RESET	RESET Input	2 U.L.
Out, $\overline{Out}$	Output Pulse	5 U.L.

Timing Considerations

Pulse Extension . . . . . $P_X \approx .31\ RC$

Minimum Input Pulse Width . . . . . $P \geqslant 200\ C + 200$ ns

Minimum Time Required Between Input Pulses. . . . . 300 ns

I/O Function	t_{P+0+}	t_{P+0-}	t_{P-0-}	t_{P-0+}
t_{PD}	500 ns	650 ns	650 ns	750 ns

t_{PD} is guaranteed at $V_{CC} \pm 1$ V and across applicable temperature range with the output loaded with 5 unit loads.

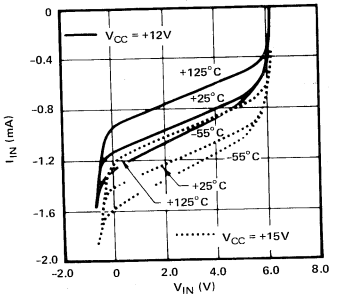
Electrical Characteristics

Parameter	Definition	Type C (V_{CC} = +12V ±1.0V) $-30°C \leq T_A \leq +85°C$	Type A (V_{CC} = +15V ±1.0V) $-30°C \leq T_A \leq +70°C$	Test Condition
V_{INL}	Input Threshold Voltage, Low	5.0 V Min	5.0 V Min	Guaranteed Input Low Threshold
V_{INH}	Input Threshold Voltage, High	6.5 V Max	6.5 V Max	Guaranteed Input High Threshold
I_{INL}	Input Current, Low	−2.1 mA Max	−2.6 mA Max	At V_{CC} Max with $V_{IN} = V_{OL}$
I_{INH}	Input Leakage Current	10μA Max	10μA Max	At V_{CC} Max with $V_{IN} = V_{CC}$ Max
V_{OL}	Output Low Voltage	1.5 V Max	1.8 V Max	I_{OL} = 5 U.L. (1 U.L. = I_{INL})
V_{OH}	Output High Voltage	10 V Min	13 V Min	I_{OH} = 5 U.L. (1 U.L. = I_{INH})
V_{OHL}	Output High Voltage, Loaded	7.0 V Min	9.5 V Min	At V_{CC} Nominal I_{OHL} = 5.0 mA
I_{CC}	Power Supply Current	40 mA	50 mA	At V_{CC} Max Worst Case Condition (Q Outputs Low)

NOTE: I_{CC} is tested at V_{CC} + 1 volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temperature range.

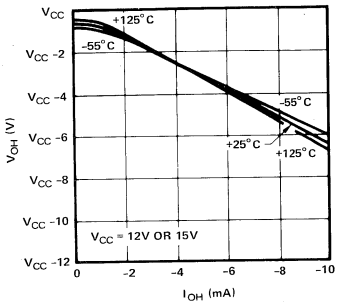
Typical Characteristics

Input Current Vs. Input Voltage

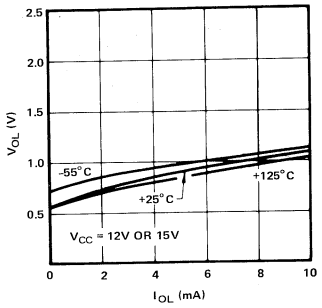


Output Current Vs. Output Voltage

Output High

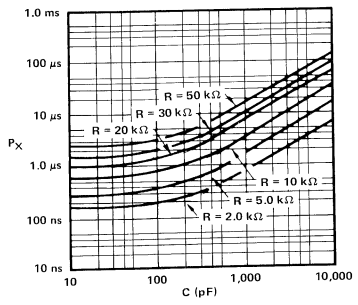


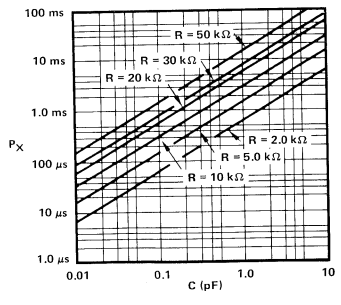
Output Low



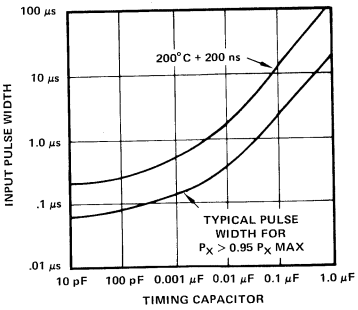
Typical Performance Characteristics

Pulse Extension (P_X) Vs. R/C Variation

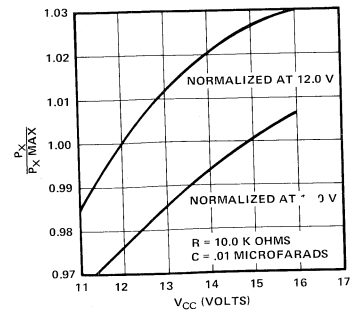




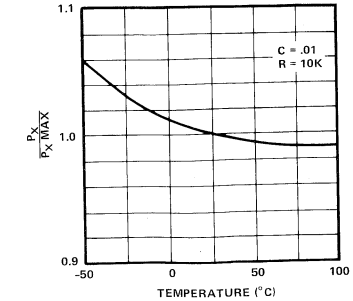
Minimum Input Pulse Width Vs. C



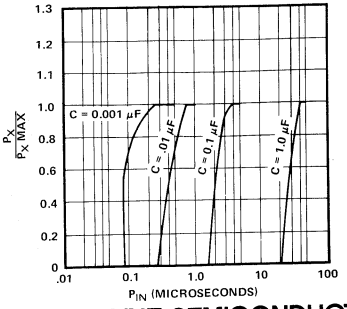
Normalized Output Pulse Width Vs. V_{CC}



Normalized Pulse Width Vs. Temperature



P_X (Normalized) Vs. P_{IN} As A Function Of C



14

Designer's Guide

The pulse extension is determined by the RC time constant of externally connected components. The output pulse width is given by $P_{IN} + P_X$, where $P_X \approx .31$ RC.

Figures 1, 2 and 3 below summarize the various I/O pulses for normal, retrigger and reset modes of operation. The retrigger capability can be inhibited by connecting the output to the inverting input.

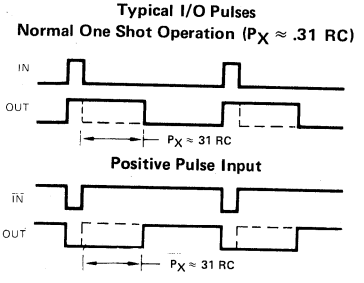


Figure 1

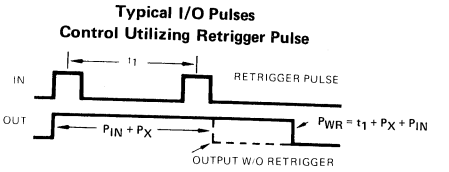


Figure 2

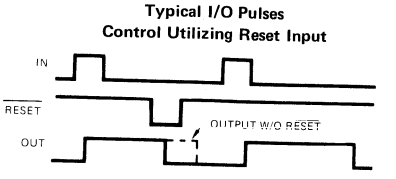


Figure 3

The external resistor is connected to V_{CC} and the capacitor to ground. This configuration makes the 349 immune to power transients and overcomes false triggering tendency.

Features

- VERSATILE DESIGN CONFIGURATION
- 3.5V (MIN) NOISE IMMUNITY
- ACTIVE PULLUP OUTPUTS – 12mA I_{OH} ENABLES LONG LINES TO BE DRIVEN
- SEPARATE ENABLE INPUTS (ON 351) – ALLOWS INDEPENDENT OPERATION
- COMPLEMENTARY OUTPUTS (ON 350) – FOR GREATER LOGIC FLEXIBILITY
- FULLY BUFFERED INPUTS – ONLY 1 UNIT LOAD (UL)
- INPUT ENABLE

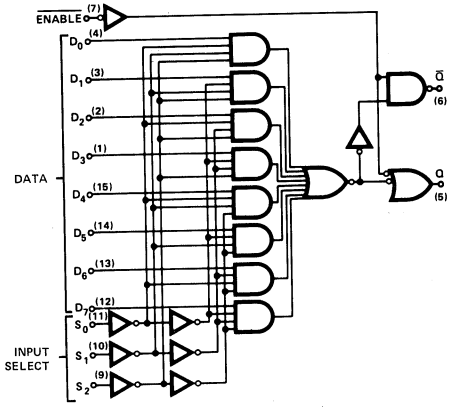
General Description

Teledyne Semiconductor 350 8-Bit, and 351 Dual 4-Bit Multiplexers were designed to enhance the functional capabilities of the high voltage logic designer. The devices exhibit the high noise immunity (3.5V min.) characteristic of the Teledyne HiNIL family.

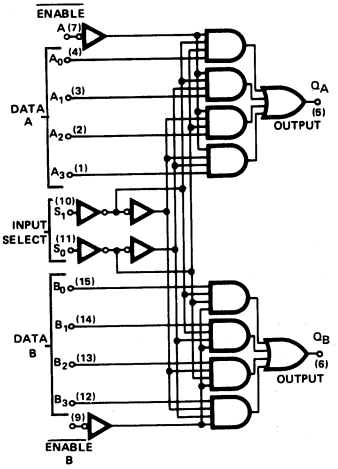
Each device is provided with an input enable line that allows the designer to control input and output timing. The input select lines determine the address of the input selected.

Logic Diagrams

350

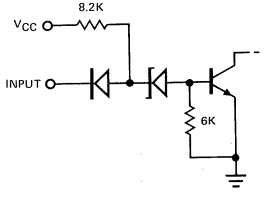


351

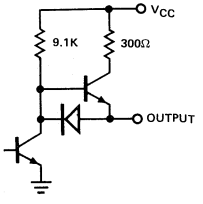


Equivalent Circuits

TYPICAL INPUT



TYPICAL OUTPUT



14

Truth Tables

350

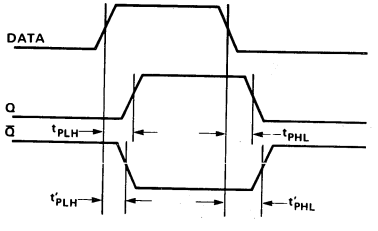
Enable	S_0	S_1	S_2	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Q	$\overline{Q}$
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	1	0	0	X	0	X	X	X	X	X	X	0	1
0	1	0	0	X	1	X	X	X	X	X	X	1	0
0	0	1	0	X	X	0	X	X	X	X	X	0	1
0	0	1	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
0	0	0	1	X	X	X	X	0	X	X	X	0	1
0	0	0	1	X	X	X	X	1	X	X	X	1	0
0	1	0	1	X	X	X	X	X	0	X	X	0	1
0	1	0	1	X	X	X	X	X	1	X	X	1	0
0	0	1	1	X	X	X	X	X	X	0	X	0	1
0	0	1	1	X	X	X	X	X	X	1	X	1	0
0	1	1	1	X	X	X	X	X	X	X	0	0	1
0	1	1	1	X	X	X	X	X	X	X	1	1	0
1	X	X	X	X	X	X	X	X	X	X	X	1	1

351

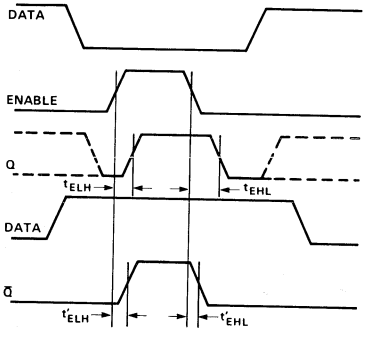
Enable	S_0	S_1	D_0	D_1	D_2	D_3	Q
0	0	0	0	X	X	X	0
0	0	0	1	X	X	X	1
0	1	0	X	0	X	X	0
0	1	0	X	1	X	X	1
0	0	1	X	X	0	X	0
0	0	1	X	X	1	X	1
0	1	1	X	X	X	0	0
0	1	1	X	X	X	1	1
1	X	X	X	X	X	X	0

Switching Time Waveforms

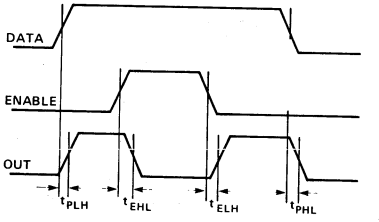
350



350



351



Specifications

I_{CC} (Worst Case) 33mA @ 13V, 40mA @ 16V

350

Parameter	Maximum
t_{PLH}	450ns
t_{PHL}	200ns
t'_{PLH}	400ns
t'_{PHL}	250ns

With enable input at low logic voltage.

350

Parameter	Maximum
t_{ELH}	400ns
t_{EHL}	250ns
t'_{ELH}	400ns
t'_{EHL}	250ns

High on enable input sets both Q and $\overline{Q}$ to high.

351

Parameter	Maximum
t_{PLH}	400ns
t_{PHL}	150ns
t_{ELH}	500ns
t_{EHL}	160ns

High on enable input sets output low.

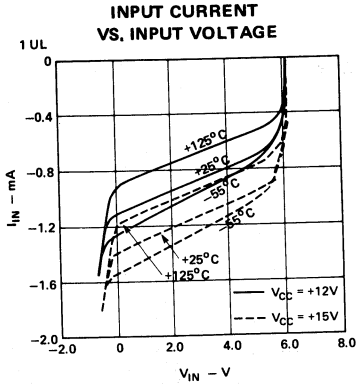
See page 12 for electrical summary data.

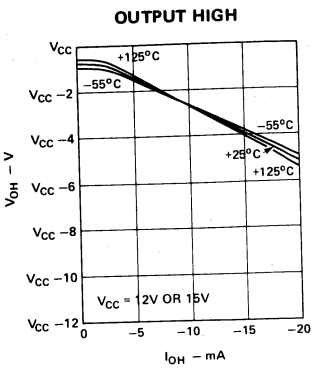
Loading Table

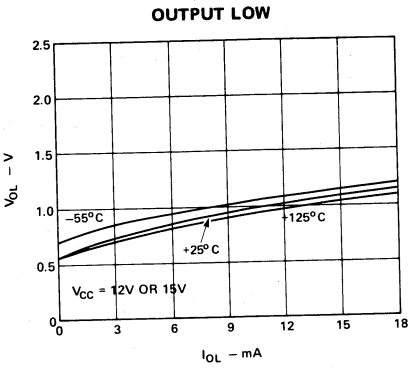
350, 351

PIN	LOADING
Input Select, All Data Inputs and Enable	1 UL
Output (Q or $\overline{Q}$)	8 UL

Typical Performance Characteristics





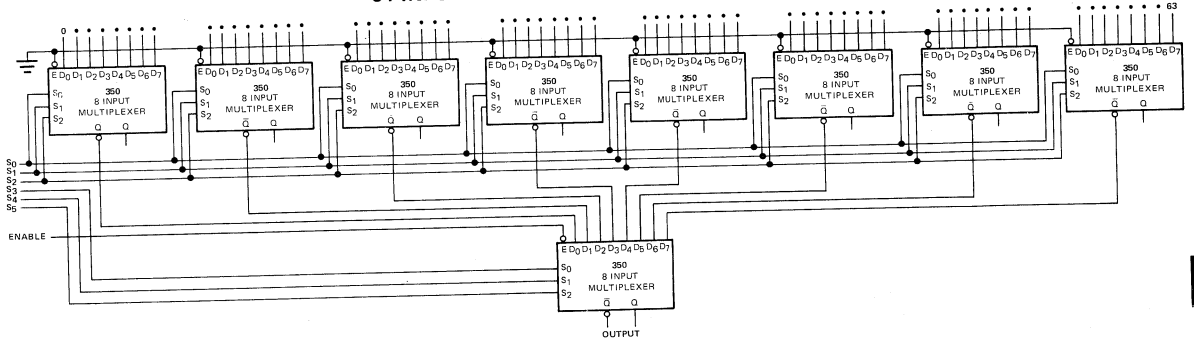


Typical Applications

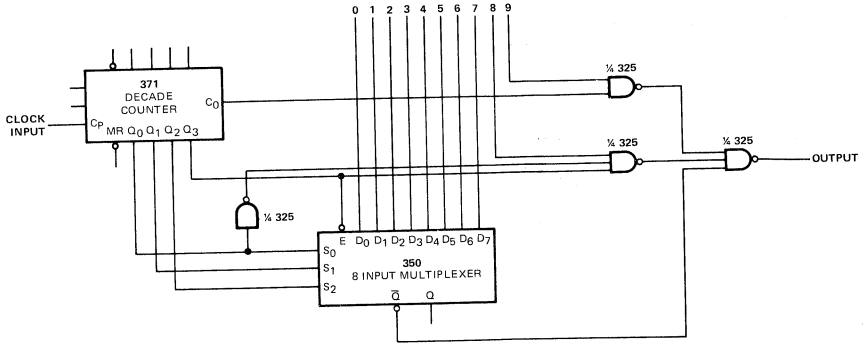
The 350 8-Bit Multiplexer is the electronic equivalent of a single-pole eight-position switch. It can serve as an 8-Bit parallel to serial converter, but differs from a shift register in that each input is selected by a 3-Bit binary number. High logic levels on the various input select lines S_0, S_1, and S_2, determine the active input. An active enable input expands the multifunctional capabilities of the device and allows inhibit operation. Complementary outputs are provided for greater logic flexibility.

The 351 Dual 4-bit Multiplexer is essentially an electronic two-pole four-position switch whose output is determined by the logic state of the two input select lines, S_0 and S_1. It features common input select lines and independent output enables for two-phase operation.

64 INPUT DIGITAL MULTIPLEXING SCHEME



DECADE MULTIPLEXER



14

Typical Applications (contd.)

REMOTE PARALLEL TO SERIAL DATA TRANSMISSION

The high output current (I_{OH}) of the 350/351 makes them ideal line driver circuits — no special drivers are required.

Figure A

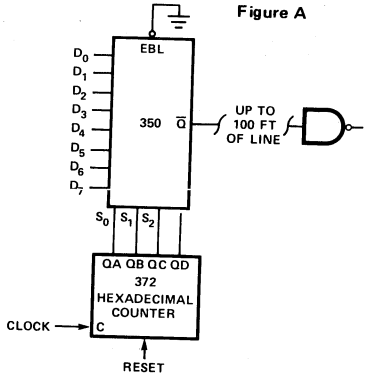
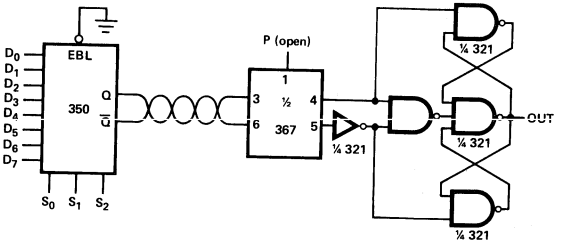
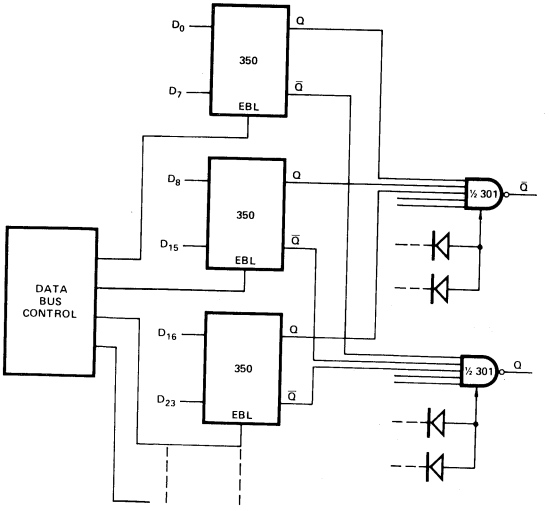


Figure B



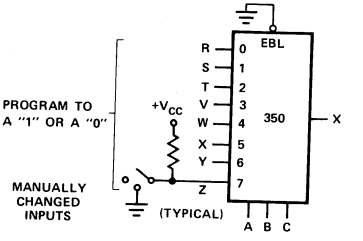
MULTI-CHANNEL DATA BUS

The enable function of the 350 (a low on ENABLE sets both Q and $\overline{Q}$ to logic "1") allows data busing of N channels of data to a single output. The 301 has expandable inputs and each additional input requires only the addition of a discrete diode on expanded input (i.e., 1N4148).



MINTERM GENERATION WITH 350 8 BIT MULTIPLEXER

The 350 and 351 Multiplexers resemble read-only memories in their basic functioning (i.e., the input select word, and data inputs can be considered an address generating some specific output). This similarity makes these devices practical in such applications as minterm generators or sequencers.



$$X = (R)(\overline{A}\,\overline{B}\,\overline{C}) + (S)(A\,\overline{B}\,\overline{C}) + (T)(\overline{A}\,B\,\overline{C}) + (V)(A\,B\,\overline{C}) + (W)(\overline{A}\,\overline{B}\,C) + (X)(A\,\overline{B}\,C) + (Y)(\overline{A}\,B\,C) + (Z)(A\,B\,C)$$

Features

- Timing – From Microseconds to Hours
- CMOS and HiNIL Compatible Inputs/Outputs
- High Current Drive Capability – 100 mA Source or Sink
- No Current Spiking on Output
- Pin Compatible With 555 Timer

General Description

The Teledyne Semiconductor 355 Timer is designed to be used as an accurate time delay device or as an astable oscillator in industrial control environments. Timing intervals of the 355 Timer are controlled by an external RC network.

The 355 triggers on the negative edge of the low going trigger pulse. Trigger pulse width must be shorter than the timing interval set by the RC combination. If the trigger is held low, the output will remain high until the trigger is driven high again.

Typical Applications

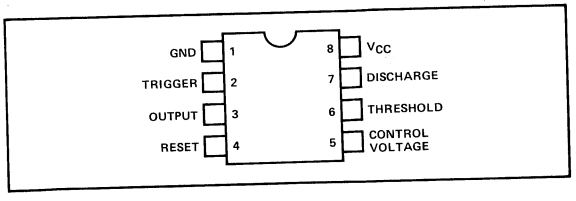
Time Delay Generation
Clock Generation
Pulse Generation
Pulse Shaping
Pulse Width Modulation
Missing Pulse Detector

Connection Diagram

Order Part Numbers:

L Package
8-Pin Ceramic DIP
($0°C \leq T_A \leq 70°C$)
355 AL/CL

J Package
8-Pin Plastic DIP
($0°C \leq T_A \leq 70°C$)
355 AJ/CJ

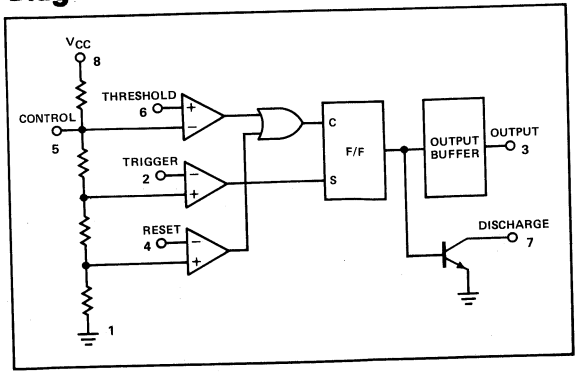


Absolute Maximum Ratings

Continuous Supply Voltage	16.5V
Pulsed Supply Voltage (<100ms)	18.0V
Input Voltage (Any Input)	−0.5V to +18V
Surge Sink Current (100ms at $T_A = 25°C$)	150mA
Storage Temperature (L Package)	−65°C to +150°C
(J Package)	−55°C to +100°C
Lead Temperature (1/16 inch from case, 10 seconds max)	300°C

NOTE: Exceeding the absolute maximum ratings may cause permanent damage. Function of HiNIL devices at the absolute maximum ratings or beyond the conditions guaranteed is not implied.

Diagram



14

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage	11		16	V
Free Air Operating Temperature Range – T_A	0	25	70	°C

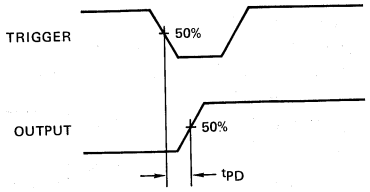
Electrical Characteristics

(Over recommended operating conditions unless otherwise noted).

Parameter	Conditions	Min	Typ	Max	Units
Supply Current	Low State Output (Note 1) V_{CC} = 16V, $R_L = \infty$		15	20	mA
Timing Error	R_A, R_B = 1KΩ to 100KΩ C = 0.1μF				
Initial Accuracy			1.0	3.0	%
Drift with Temperature					
(Monostable)	(Note 2)		300		ppm/°C
(Astable)			500		ppm/°C
Drift with Supply Voltage			0.4	0.7	%/V
Threshold Voltage	V_{CC} = 12V	7.5	8.0	8.5	V
	V_{CC} = 15V	9.5	10.0	10.5	V
Trigger Voltage	V_{CC} = 12V	5.0	5.4	5.8	V
	V_{CC} = 15V	6.3	6.75	7.2	V
Trigger Current	V_{CC} = 16V		1.3	10	μA
Reset Voltage	V_{CC} = 12V	4.3	4.8	5.3	V
	V_{CC} = 15V	5.5	6.0	6.5	V
Reset Current	V_{IN} = 1.5V		1.3	10	μA
Threshold Current	(Note 3) V_{IN} = 11V, V_{CC} = 15V V_{IN} = 9V, V_{CC} = 12V		200	400	nA
Control Voltage Level	V_{CC} = 12V	7.5	8.0	8.5	V
	V_{CC} = 15V	9.5	10.0	10.5	V
Low Output Voltage	V_{CC} = 15V				
	I_{SINK} = 13mA		1.0	1.5	V
	I_{SINK} = 75mA		1.4	2.0	V
	I_{SINK} = 100mA		2.0		
High Output Voltage	I_{SOURCE} = 50mA				
	V_{CC} = 12V	9.0	10.2		V
	V_{CC} = 15V	12.0	13.2		V
	I_{SOURCE} = 100mA, V_{CC} = 15V		12.7		V
	I_{SOURCE} = 50μA				
	V_{CC} = 11V	9.0	9.4		V
	V_{CC} = 14V	12.0	12.4		V
Discharge Leakage Current	V_{CC} = 16V $V_{DISCHARGE}$ = 15V		20	100	nA
Maximum Oscillator Frequency		100	300		kHz
Propagation Delay (t_{PD})	Trigger to Output		330		nsec

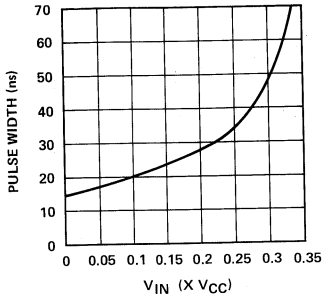
NOTES:
(1) Supply current when output is high is typically 1.0mA less.
(2) Tested at V_{CC} = 12V and V_{CC} = 15V.
(3) This will determine the maximum value of $R_A + R_B$. For 15V operation the maximum total is R = 10MΩ.

Switching Waveforms

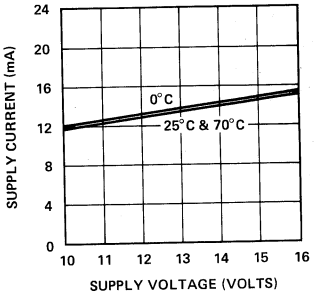


Typical Performance Characteristics

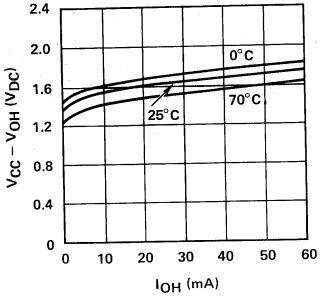
MINIMUM V_{IN} VS. INPUT PULSE WIDTH



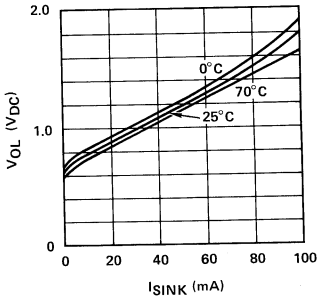
I_{CC} VS. V_{CC}



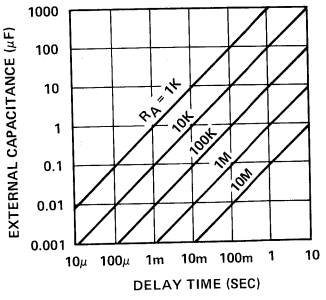
HIGH OUTPUT VOLTAGE



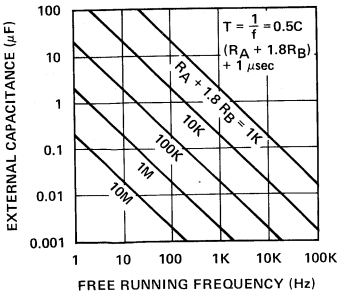
LOW OUTPUT VOLTAGE



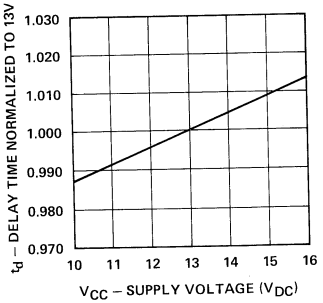
DELAY TIME VS. R_A, C



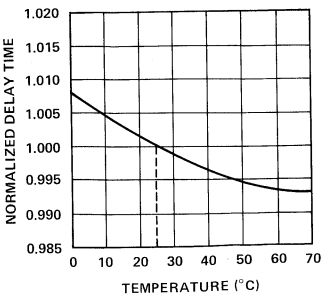
FREE-RUNNING FREQUENCY VS. R, C



DELAY TIME VS. SUPPLY VOLTAGE



NORMALIZED DELAY TIME VS. TEMPERATURE



14

Circuit Control Description

Output, Pin 3 – The output logic level is normally in a "low" state, and goes "high" during the timing cycle.

Trigger, Pin 2 – The timing cycle is initiated by lowering the dc level at the trigger terminal below V_{CC}. Once triggered, the circuit is immune to additional triggering until the timing cycle is complete, unless the succeeding trigger overlaps the normal end of the output pulse.

Threshold, Pin 6 – The timing cycle is complete when the voltage level at the threshold reaches $2/3V_{CC}$. At this point, the threshold comparator changes state, resets the internal flip-flop, and initiates the discharge cycle.

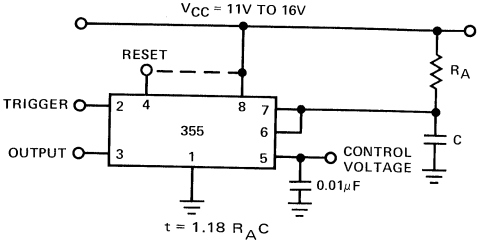
Control or FM, Pin 5 – The timing cycle or the frequency of oscillation can be controlled or modulated by applying a dc control voltage to pin 5. This terminal is internally biased at $2/3V_{CC}$. The control signal for frequency modulation or pulse-width modulation is applied to this terminal. When not in use, the control terminals should be ac grounded through 0.01μF decoupling capacitors.

Discharge, Pin 7 – This terminal corresponds to the collector of the discharge transistor. During the charging cycle, this terminal behaves as an open-circuit; during discharge, it becomes a low impedance path to ground.

Reset, Pin 4 – The timing cycle can be interrupted by grounding the reset terminal. When the reset signal is applied, the output goes "low" and remains in that state while the reset voltage is applied. When the reset signal is removed, the output remains "low" until retriggered. When not used, the reset terminal should be connected to V_{CC} in order to avoid any possibility of false resetting. When the timing circuit is operated in the astable mode, the reset terminal can be used for "on" and "off" keying of the oscillation.

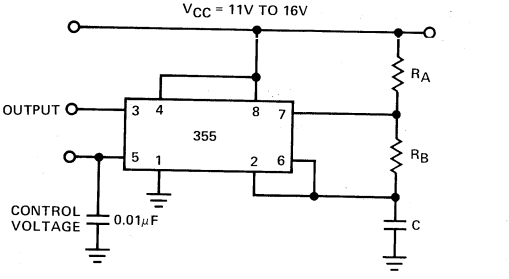
Applications Information

Monostable Operation



$t = 1.18\ R_A C$

Astable Operation



The charge time (Output High) is: $t_1 = 0.5\ (R_A + R_B)\ C$

The discharge time (Output Low) is: $t_2 = 0.4\ (R_B)\ C$

The total period is:

For < 5kHz: $T = t_1 + t_2 = 0.5\ (R_A + 1.8\ R_B)\ C$
For > 5kHz: $T = t_1 + t_2 = [0.5\ (R_A + 1.8\ R_B)\ C] + 1\mu sec$

The frequency of oscillation is: $f = \frac{1}{T} = \frac{2}{(R_A + 1.8\ R_B)\ C}$

The duty cycle is: $D = \frac{R_B}{R_A + 1.8\ R_B}$

Features

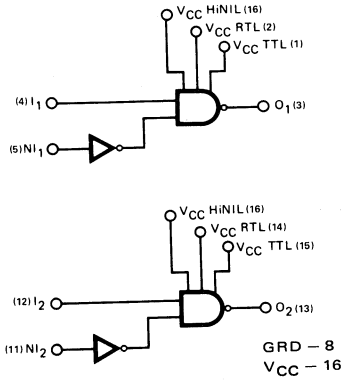
- DROPS HiNIL LOGIC LEVELS TO LOWER LOGIC LEVELS
- INVERTING AND NONINVERTING INPUTS AVAILABLE
- SPECIFIED TO RTL AND TTL CHARACTERISTICS
- IDEAL COMPANION TO 362 OUTPUT INTERFACE

General Description

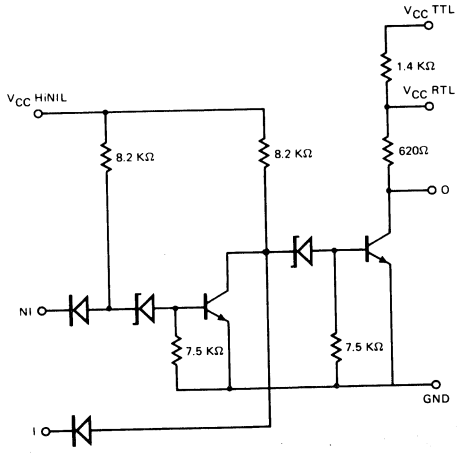
The 361 is used to convert HiNIL logic levels to DTL, TTL and RTL logic levels. It is very simple to use, merely requiring connection to the V_{CC} output level desired for adjustment of the output to the lower logic level.

See 362, 363 for applications information.

Logic Diagrams



Equivalent Circuit



Specifications

SPECIFICATION AS RTL INTERFACE:
V_{CC} (RTL) = 3.0 VOLTS

PARAMETER	TEMPERATURE (°C) -30	+25	+70/+85
I_A, min. available output current at V_{OUT} =	-2.3 mA 0.95V	-2.2 mA 0.85V	-2.0 mA 0.75V
V_{OL}, max. output low voltage	350 mV	300 mV	330 mV

SPECIFICATION AS TTL INTERFACE:
V_{CC} (TTL) = 4.5V

PARAMETER	TEMPERATURE (°C) -30	+25	+70/+85
V_{OL}, max. output low voltage I_{OL} = 6.4 mA	0.4V	0.4V	0.4V
V_{OH}, min. output high voltage I_{OH} = -160 μA	2.4V	2.4V	2.4V

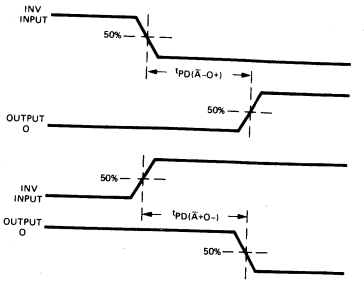
I_{CC} (WORST-CASE)	8 mA @ 13V, 11 mA @ 16V			
t_{PD}	230 ns	325 ns	260 ns	240 ns
I/O FUNCTION FOR t_{PD}	A–O+	A+O+	A–O–	$\overline{A}$+O–

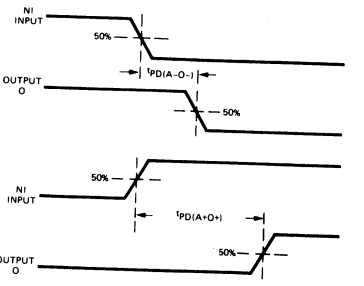
Note: I_{CC} is tested at V_{CC} + 1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range. t_{PD} is guaranteed at $V_{CC} \pm 1$V and across the applicable temp range.

See page 12 for electrical summary data.

14

Switching Time Waveforms



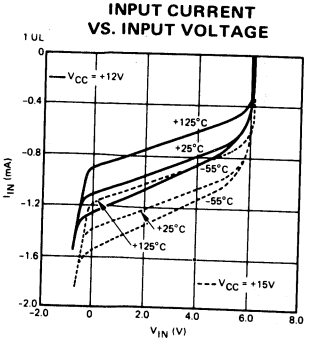


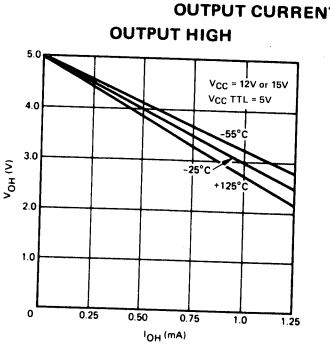
Loading Table

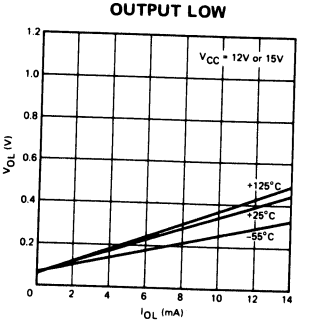
361

PINS	FUNCTION	LOADING
I	Inverting input	1 UL
NI	Noninverting input	1 UL
O	Output	See specifications

Typical Performance Characteristics







TSC362/363
5 Volt to 11-16V Interface
- Dual Translator
- Quad 2-Input NAND

Features

362

- CONVERTS, DTL, TTL OR RTL TO HiNIL LOGIC LEVELS
- INVERTING AND NONINVERTING INPUTS
- SPECIFIED TO TTL AND RTL CHARACTERISTICS
- IDEAL COMPANION TO 361 INPUT INTERFACE

363

- FANOUT UP TO 15
- VERSATILE TTL TO HiNIL INTERFACE
- EXPANDABLE
- COLLECTOR OR'able OUTPUTS
- EXCELLENT LINE DRIVER

General Descriptions

362

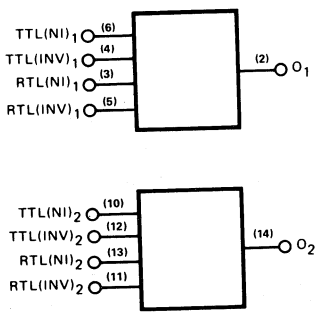
The 362 converts TTL or RTL logic levels to HiNIL logic levels. The converted data is available at the active pullup output in inverted or noninverted form, depending on the choice of input.

363

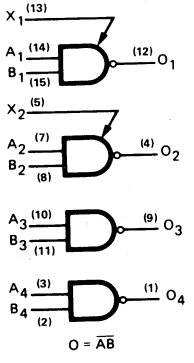
The 363 converts TTL logic levels to HiNIL levels and drives lines at the HiNIL levels. For applications flexibility, the 363 is configured as a quad NAND gate with passive pullup outputs and two expander inputs.

Logic Diagrams

362



363

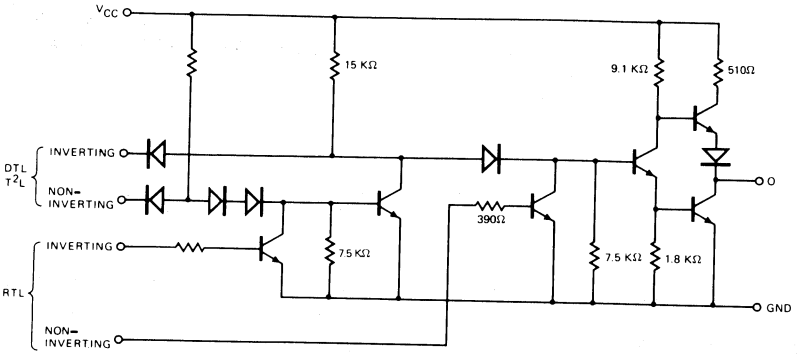


GRD – 8
V_{CC} – 16

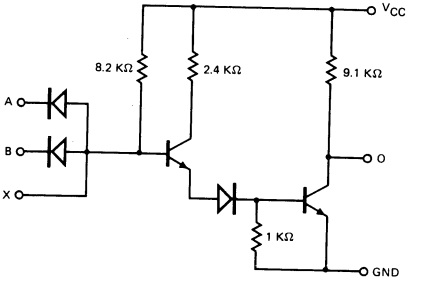
14

Equivalent Circuits

362



363



Specifications

V_{OHL}	6V min @ V_{CC} = 12V (Type C), 9V min @ V_{CC} = 15V (Type A)							
V_{OH}	9V min @ V_{CC} = 11V (Type C), 12V min @ V_{CC} = 14V (Type A)							
I_{CC} (WORST-CASE)	10 mA @ 13V, 13 mA @ 16V							
t_{PD} I/O FUNCTION FOR t_{PD}	160 ns RTLI+–	400 ns RTLI–+	335 ns RTLNI––	225 ns RTLNI++	100 ns TTLI+–	235 ns TTLI–+	125 ns TTLNI––	225 ns TTLNI++

Note: I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range. t_{PD} is guaranteed at $V_{CC} \pm 1V$ and across the applicable temp range with the output loaded with 5 unit loads.

See page 12 for electrical summary data.

362 SPECIFICATIONS FOR RTL INPUTS

	C and A Types		
Temp (°C)	–30	+25	+70/+85
I_{IN} (μA)	460	440	470
V_{INH} (V)	0.95	0.85	0.75
V_{INL} (V)	0.6	0.5	0.38

362 SPECIFICATIONS FOR TTL INPUTS

V_{INH} = 2.0V; I_{INH} = 10μA
V_{INL} = 0.8V; I_{INL} = 1.6 mA at V_{IN} = 0.4V
(these specs apply over full temperature range)

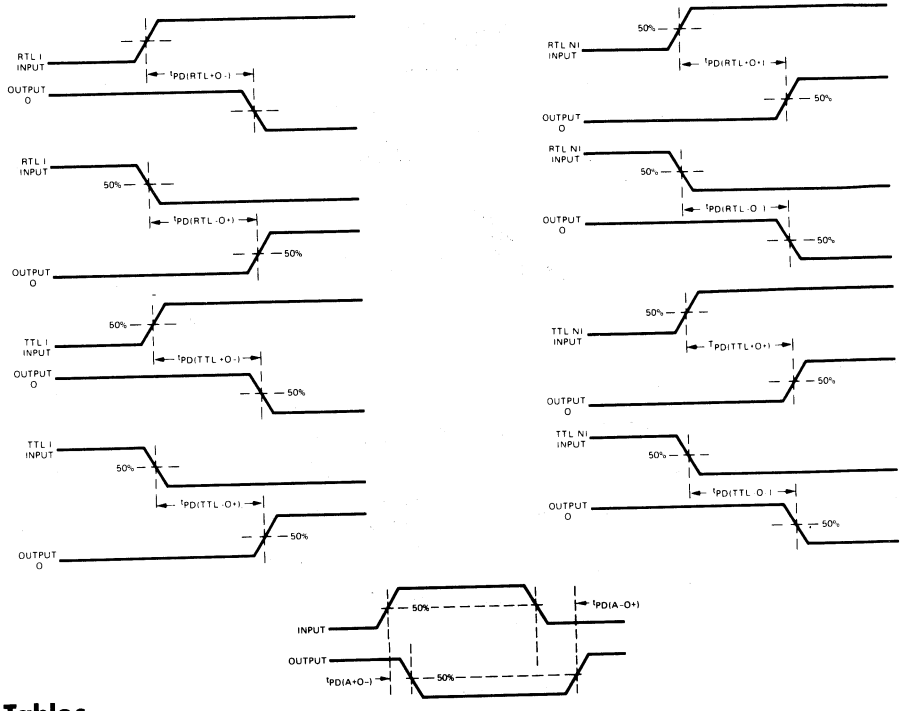
363

I_{CC} (WORST-CASE)	51 mA @ 13V, 64 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	240 ns A+O–	600 ns A–O+

363 SPECIFICATIONS FOR TTL INPUTS

V_{INH} = 2.0V; I_{INH} = 10μA
V_{INL} = 0.8V; I_{INL} = 2.4 mA @ V_{CC} = 13V, V_{IN} = 0.4V
V_{INL} = 0.8V; I_{INL} = 3.0 mA @ V_{CC} = 16V, V_{IN} = 0.4V

Switching Time Waveforms



Loading Tables

362

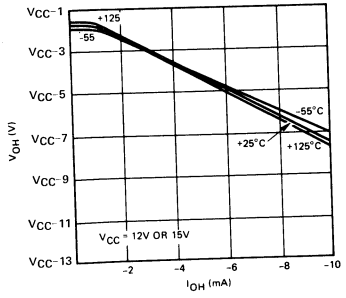
TTL, RTL O	Inputs Outputs	See specifications 5 UL

363

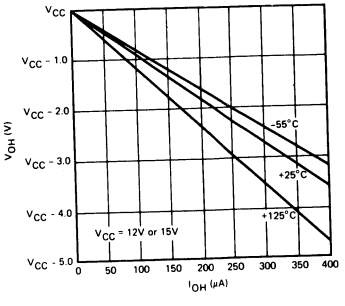
PINS	FUNCTIONS	LOADING
A, B X O	TTL inputs Expanders Outputs	1 TTL load TTL expander input loading applies 5 UL 15 UL with 8.2K supplemental pullup resistor

Typical Performance Characteristics

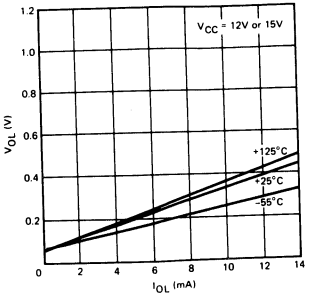
OUTPUT HIGH
362



OUTPUT CURRENT VS OUTPUT VOLTAGE
OUTPUT HIGH
363



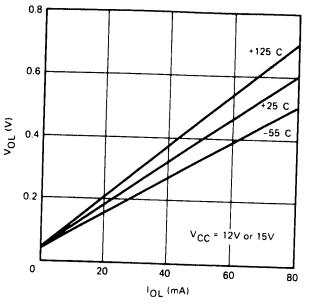
OUTPUT LOW
362



14

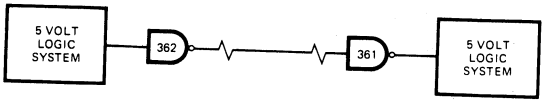
Typical Performance Characteristics (contd.)

OUTPUT LOW
363



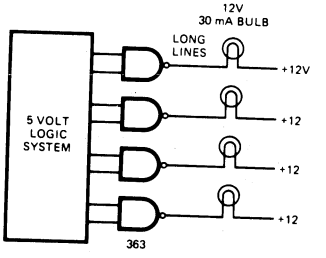
Typical Applications

LOW-NOISE DATA TRANSMISSION



When signal lines between two low-level logic systems pass through a noisy environment, use 362 and 361 transmit/receive pairs to prevent noise pickup by the receiving system.

INDICATOR DRIVER



Because of its higher output sink current and voltage, the 363 is an excellent output interface for 5V logic systems. Here, it allows a 5V logic system to control indicator lamps.

TSC367/368
Schmitt Trigger
- Quad (Active Pullup)
- Quad (Open Collector)

Features

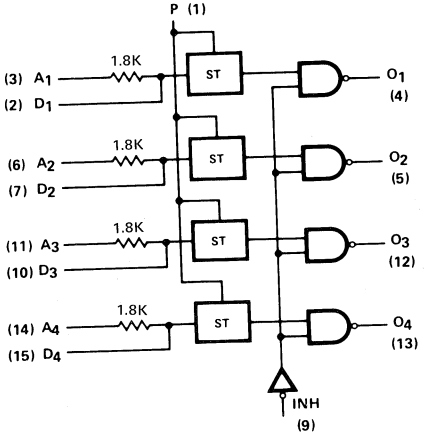
- 4.5V TYPICAL HYSTERESIS – 2.5V WORST CASE NOISE IMMUNITY, EVEN WHILE SWITCHING!
- 5.5V TYPICAL DC NOISE IMMUNITY – 4.5V WORST CASE
- OPTIONAL HOOKUP DOES NOT RECOGNIZE OPEN CIRCUITS – ELIMINATES FALSE COUNTS DUE TO CONTACT BOUNCE FROM SWITCHES AND RELAYS
- DELAY PINS ALLOW THE USE OF EXTERNAL SLOW-DOWN CAPACITORS – PROPAGATION DELAY INCREASES 2.5 ms/μF
- IDEAL FOR USE AS A LINE RECEIVER
- INHIBIT INPUT PERMITS INFORMATION TO BE ACCEPTED ONLY DURING PERIODS OF LOW NOISE IN THE SYSTEM CYCLE
- OVERVOLTAGE INPUT PROTECTION – WITHSTANDS ±100V, 1μSEC NOISE SPIKE OR –5V TO V_{CC} +5V STEADY-STATE

367 – DIRECTLY INTERFACES WITH HiNIL AND CMOS
368 – DIRECTLY INTERFACES WITH TTL

General Description

The Teledyne Semiconductor 367/368 Quad Schmitt Trigger has been designed as a universal input port for HiNIL logic blocks. Its unique truth table completely eliminates false counts due to contact bounce on switches, relays, etc. At the same time, its 6.5V DC noise immunity and the 4.5V dead zone provided by the Schmitt Trigger action totally eliminates noise problems occurring on long lines. Delay pins can be used with slowdown capacitors to slow the circuit down as far as needed, and still maintain 2.5V guaranteed noise immunity. An inhibit input can be used to accept input information only at certain times in the system cycle.

Logic Diagram

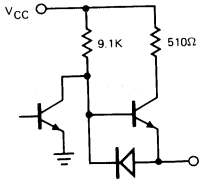


GRD – 8
V_{CC} –16

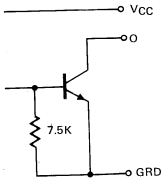
A – DATA INPUT
D – DELAY PIN
O – OUTPUT
INH – INHIBIT
P – PULL-UP

Equivalent Circuits

TYPICAL OUTPUT
367



TYPICAL OUTPUT
368



14

Truth Tables

367/368
PIN P OPEN

INPUTS		OUTPUT
A	INH	O
0	0	1
OPEN (was 0)	0	1
1	0	0
OPEN (was 1)	0	0
0	1	1
1	1	1
OPEN (was 0)	1	1
OPEN (was 1)	1	1

367/368
PIN P CONNECTED TO V_{CC}

INPUTS		OUTPUT
A	INH	O
0	0	1
1	0	0
0	1	1
1	1	1

Specifications

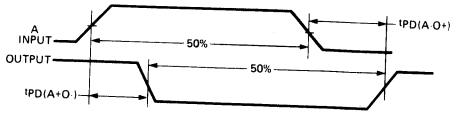
367

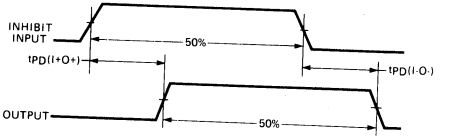
t_{PD} (Pull-up Open)	340ns	360ns	250ns	230ns
t_{PD} (Pull-up Closed)	300ns	400ns	250ns	230ns
I/O function for t_{PD}	A+O–	A–O+	I+O+	I–O–

368 WITH 10K PULLUP ON OUTPUT

t_{PD} (Pull-up Open)	340ns	550ns	450ns	300ns
t_{PD} (Pull-up Closed)	300ns	600ns	450ns	300ns

Switching Time Waveforms





Loading Table

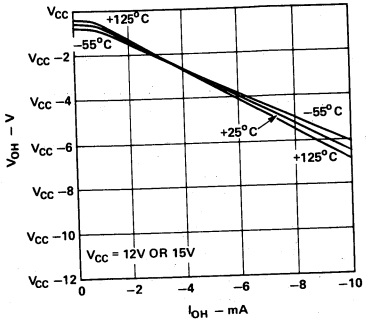
367/368

PINS	FUNCTION	LOADING
Inhibit O_1, O_2, O_3, O_4	Inhibit Outputs	1 UL 5 UL

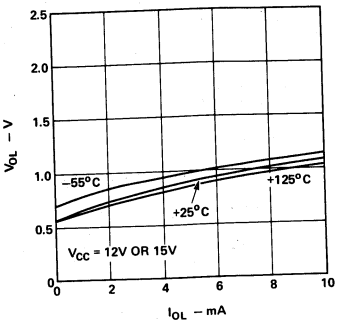
Typical Performance Characteristics

OUTPUT CURRENT VS. OUTPUT VOLTAGE

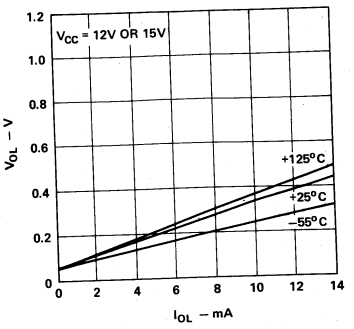
OUTPUT HIGH 367



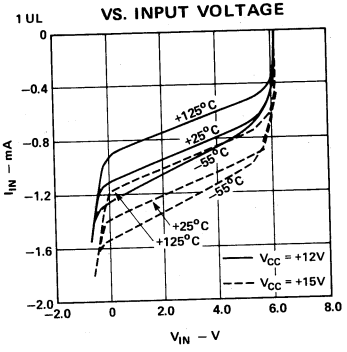
OUTPUT LOW 367



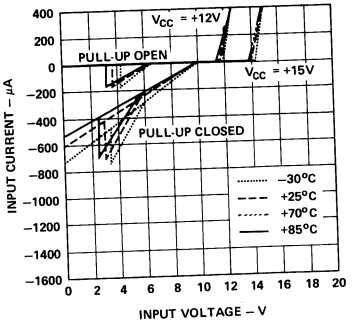
OUTPUT LOW 368



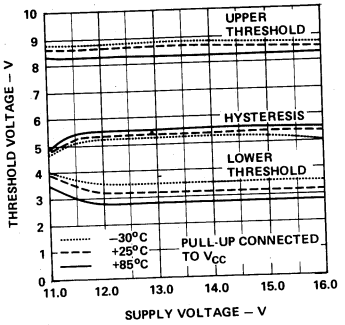
INHIBIT INPUT CURRENT VS. INPUT VOLTAGE



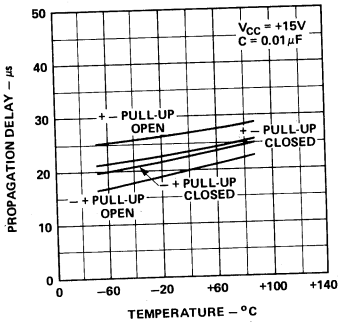
INPUT CURRENT VS. INPUT VOLTAGE



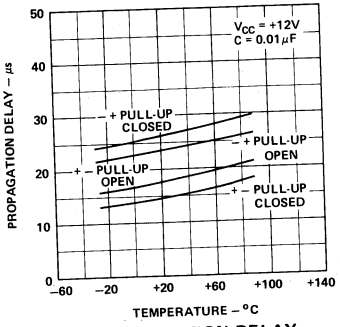
THRESHOLDS AND HYSTERESIS VS. SUPPLY VOLTAGE



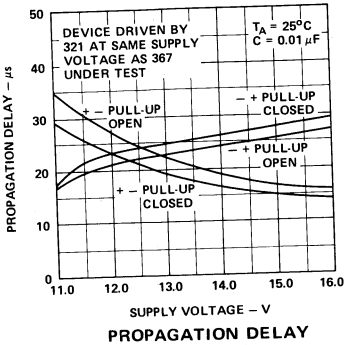
PROPAGATION DELAY VS. TEMPERATURE



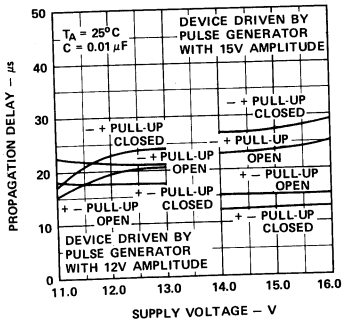
PROPAGATION DELAY VS. TEMPERATURE



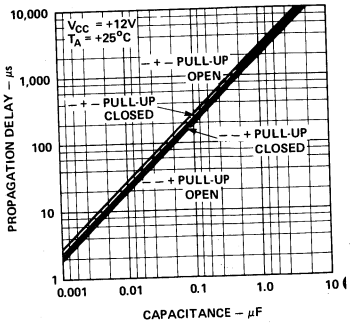
PROPAGATION DELAY VS. SUPPLY VOLTAGE



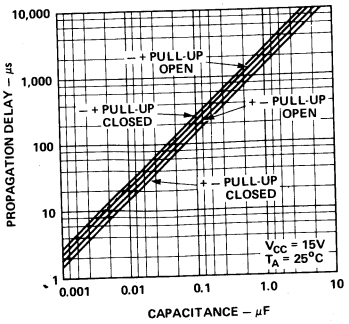
PROPAGATION DELAY VS. SUPPLY VOLTAGE



PROPAGATION DELAY VS. CAPACITANCE



PROPAGATION DELAY VS. CAPACITANCE



14

Electrical Characteristics

Parameter	Definition	$-30^oC \leq T_A \leq +85^oC$ Type C (V_{CC} = +12V ± 1V)	$-30^oC \leq T_A \leq +70^oC$ Type A (V_{CC} = +15V ± 1V)	Test Conditions
V_{INL} (Inhibit)	Input threshold voltage, low	5.0V min.	5.0V min.	Guaranteed input low threshold for Inhibit
V_{INH} (Inhibit)	Input threshold voltage, high	6.5V max.	6.5V max.	Guaranteed input high threshold for Inhibit
I_{INL} (Inhibit)	Input current, low	−2.1mA	−2.6mA	At V_{CC} max. with $V_{IN} = V_{OL1}$
I_{INH} (Inhibit)	Input leakage current	10μA	10μA	At V_{CC} max. with $V_{IN} = V_{CC}$ max.
V_T + (Data input-A) (pull-up open)	Positive going threshold voltage	8.0V min. 10.0V max.	7.5V min. 10.0V max.	Guaranteed positive going threshold for Data input (pull-up open)
V_T − (Data input-A) (pull-up open)	Negative going threshold voltage	2.0V min. 5.5V max.	2.0V min. 5.0V max.	Guaranteed negative going threshold for Data input (pull-up open)
V_T + (Data input-A) (pull-up closed)	Positive going threshold voltage	7.5V min. 9.5V max.	7.5V min. 9.5V max.	Guaranteed positive going threshold for Data input (pull-up closed)
V_T − (Data input-A) (pull-up closed)	Negative going threshold voltage	1.5V min. 5.0V max.	1.0V min. 4.5V max.	Guaranteed negative going threshold for Data input (pull-up closed)
I_T + (Data input-A) (pull-up open)	Input current at positive going threshold	40μA max.	40μA max.	Guaranteed input leakage current V_{IN} + 10V (pull-up open)
I_T − (Data input-A) (pull-up open)	Input current at negative going threshold	−1.0mA max.	−1.2mA max.	Guaranteed input low current. V_{IN} = 1.5V for C device and 1.8V for A device (pull-up open)
I_T + (Data input-A) (pull-up closed)	Input current at positive going threshold	40μA max.	40μA max.	Guaranteed input leakage current V_{IN} = 10V (pull-up closed)
I_T − (Data input-A) (pull-up closed)	Input current at negative going threshold	−2.1mA	−2.6mA	Guaranteed input low current V_{IN} = 1.5V forC device and 1.8V for A device (pull-up closed)
I_T (max)	Maximum input current	1.0mA	1.5mA	V_{IN} = 13V, V_{CC} = 13V for C device, V_{IN} = 16V, V_{CC} = 16V for A device
V_{OL}	Output low voltage	1.5V max.	1.8V max.	I_{OL}= 5 UL (1 UL = 2.1mA for C grade and 2.6mA for A grade)
V_{OL3} (368 only)	Output low voltage	0.4V max.	0.4V max.	At $V_{CC} = V_{CC}$ min, I_{OL} = 6.4mA (4 TTL UL)
V_{OH} (367 only)	Output high voltage	10.0V min.	13.0V min.	I_{OH} = 5 UL (1 UL = 10μA)
V_{OHL} (367 only)	Output high voltage loaded	7.0V min.	9.5V min.	At V_{CC} nominal I_{OH} = −5mA
I_{CC}	Power supply current (367) (368)	 36mA max. 33mA max.	 54mA max. 50mA max.	At V_{CC} maximum. Unit tested under worst case conditions
I_{CEX}	Output high leakage current (368)	25μA max.	25μA max.	At V_{CC} maximum, V_{INL} = 5.0V, $V_{CEX} = V_{CC}$ max
V_{MAX} (368 only)	Output high breakdown voltage	13.0V min.	16.5V min.	At I_{max} = 1.0mA, V_{INL} = 5.0V with I_{max} forced into output

Typical Applications

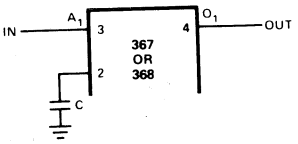
The HiNIL 367/368 Quad Schmitt Trigger has been designed to be a universal input port into HiNIL logic blocks. Its active outputs (367) are fully compatible with the rest of the HiNIL logic family and 12 or 15V CMOS. Although its inputs are not standard HiNIL, they can be used either with other HiNIL logic elements or with switch and relay contacts. The device is unique in that the user is presented with a choice of two truth tables, determined by whether an internal pullup resistor (pin P) is left open or is connected to V_{CC}. If Pin P is left open, the device will not recognize open circuits. By this we mean that the input will continue to see the logic state that was at the input before the connection was broken. It is this characteristic that eliminates errors due to contact bounce on relay or switch contacts. If Pin P is tied to V_{CC}, the device acts like a standard HiNIL circuit and considers an open input connection to be a logic one.

Occasionally a system is expected to be operable in extremely noisy environments where short noise pulses are expected in excess of 4.5V noise immunity. This problem can be eliminated by adding slow-down capacitors to special delay pins provided for this purpose. For each μF of capacitance added between the delay pin and ground the propagation delay will be increased by 2.5 ms.

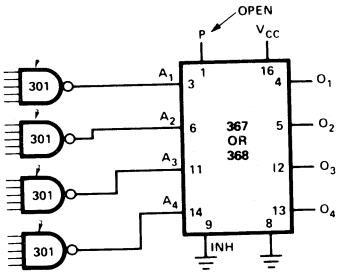
Typical Applications (contd.)

An inhibit pin is provided that forces all outputs high whenever it is high. This can be used to restrict the 367/368 so that it accepts input information only at certain points in the machine cycle. When used with pullup resistors, the open collector 368 allows direct interface to TTL, RTL, and low voltage CMOS, NMOS, or PMOS.

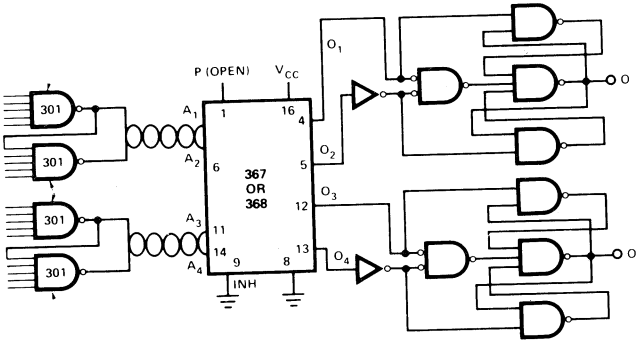
PULSE DELAY



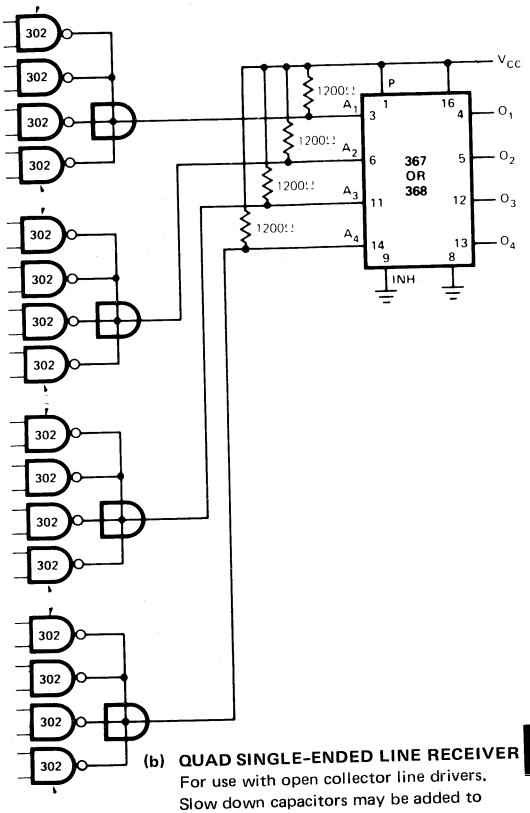
LINE RECEIVERS



(a) **QUAD SINGLE-ENDED LINE RECEIVER**
Slow down capacitors may be added to the delay inputs to improve noise-immunity.



(c) **DUAL DIFFERENTIAL LINE-RECEIVER**
Slow down capacitors may be added to the delay inputs to improve noise immunity.

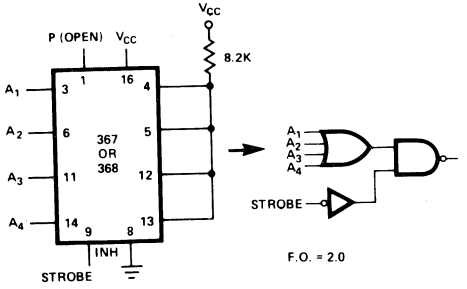


(b) **QUAD SINGLE-ENDED LINE RECEIVER**
For use with open collector line drivers. Slow down capacitors may be added to the delay inputs to improve noise immunity.

14

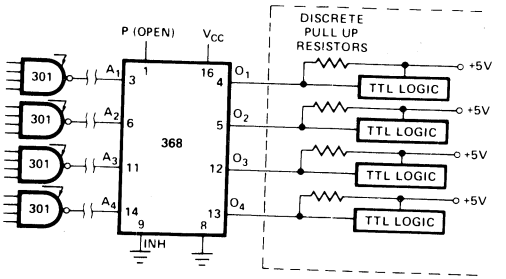
4 INPUT STROBED NOR GATE

The 368 can be used as a strobed 4 input NOR gate by tying all output pins (collector-ORing) to a common pull-up resistor, and connecting the strobe input to the INHIBIT line.



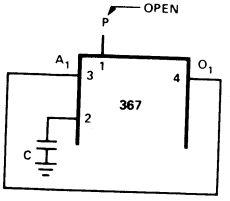
Typical Applications (contd.)

QUAD LINE RECEIVER/TTL INTERFACE



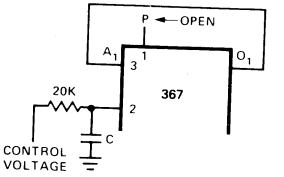
The 368 with open collector output allows direct drive interface to TTL logic.

FREE-RUNNING OSCILLATOR



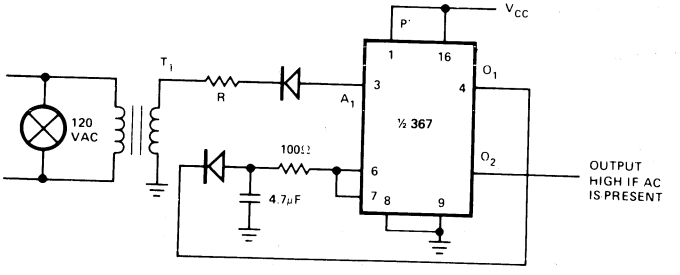
The 367 can be used to make four independent free-running oscillators. The frequency is set by the value of C tied to each delay input. The oscillators can all be started and stopped by using the inhibit input.

VOLTAGE CONTROLLED OSCILLATOR



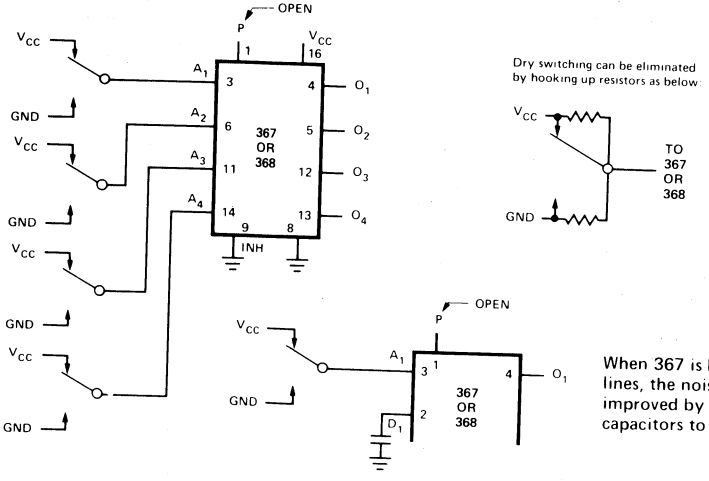
The 367 can be used to make four, independent voltage controlled oscillators.

AC LINE VOLTAGE DETECTOR



This circuit delivers logic one's whenever 120 VAC is present on the solenoid valve. Since only 1/2 of the 367 is used, two such circuits can be built with each device.

BOUNCE-FREE SWITCH



When 367 is being used with long lines, the noise immunity may be improved by adding slow-down capacitors to the delay input.

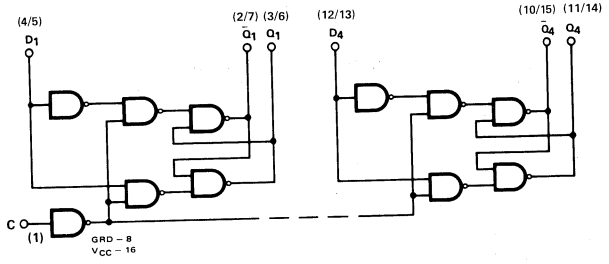
Features

- IDEAL FOR STORAGE APPLICATIONS
- COMPLEMENTARY DATA OUTPUTS
- COMMON CLOCK FOR SYNCHRONOUS OPERATION
- CLOCK ACTS AS ENABLE CONTROL WITH 1 UL
- PULLUP RESISTORS ON CHIP

General Description

The 370 contains four clocked D-type flip-flops with a common clock input acting as an enable line. Each stage has complementary outputs with passive pullup. Applications include quad latches and registers with parallel inputs and outputs.

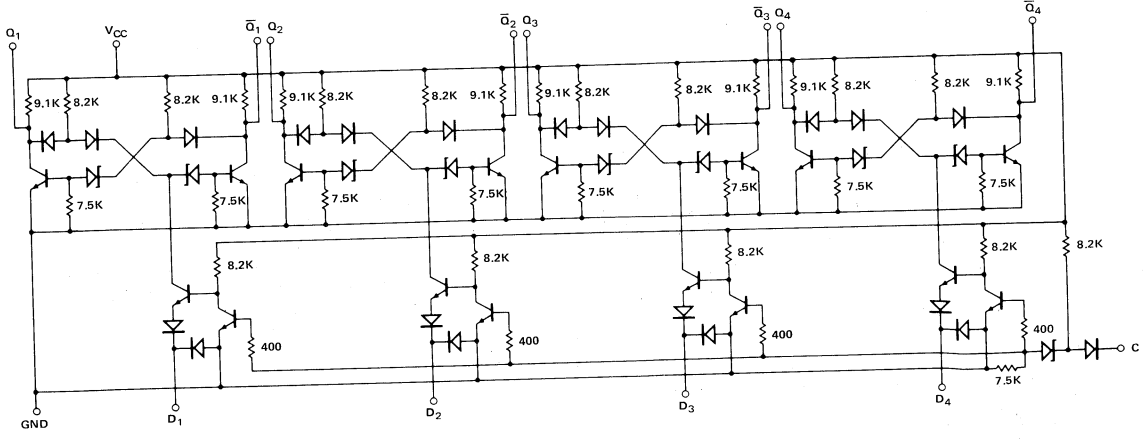
Logic Diagram



TRUTH TABLE

C	D	Q^{n+1}
1	1	Q^n
1	0	Q^n
0	1	1
0	0	0

Equivalent Circuit



14

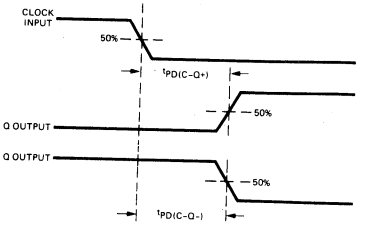
Key Specifications

I_{CC} (WORST-CASE)	38 mA @ 13V, 48 mA @ 16V	
t_{PD} I/O FUNCTION FOR t_{PD}	750 ns C–Q+	750 ns C–Q–

Note: I_{CC} is tested at V_{CC} + 1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range. t_{PD} is guaranteed at $V_{CC} \pm 1V$ and across the applicable temp range with the output loaded with 4 unit loads.

See page 12 for electrical summary data.

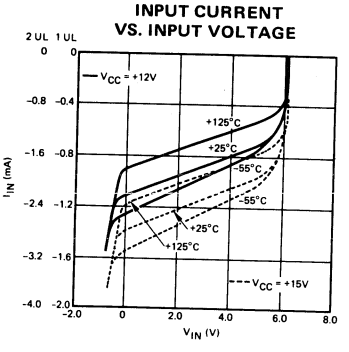
Switching Time Waveforms

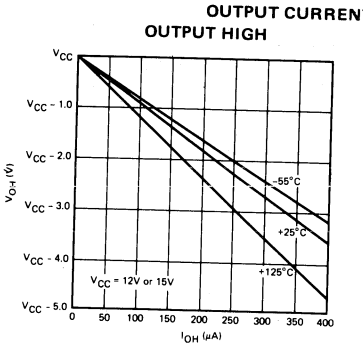


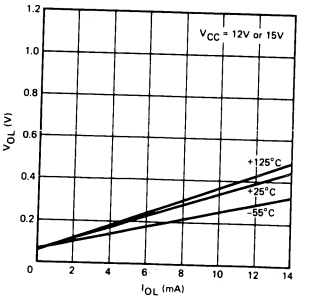
Loading Table

PINS	FUNCTION	LOADING
D	Data inputs	2 UL
C	Clock input	1 UL
Q, $\overline{Q}$	Outputs	4 UL

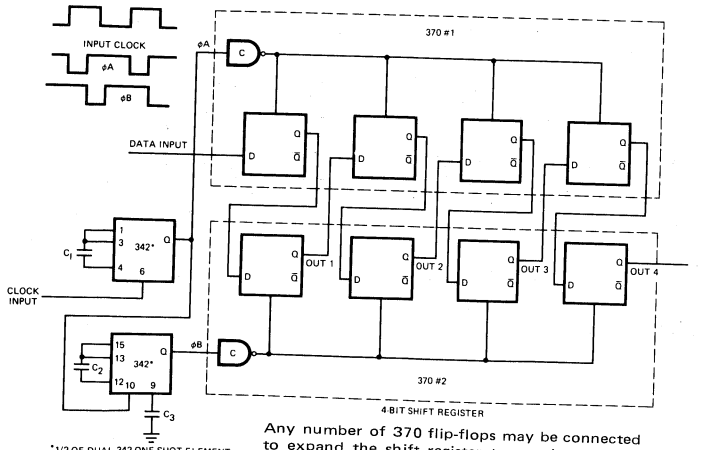
Typical Performance Characteristics







Typical Applications



*1/2 OF DUAL 342 ONE SHOT ELEMENT

Any number of 370 flip-flops may be connected to expand the shift register to any length. The 342 one-shots generate the two-phase clock signals.

Whenever the clock line is high, the flip-flops ignore the data on the D inputs, allowing the clock line to be used as a common input enable control. When the clock line is low, new data can enter the flip-flops and become available on the outputs,as shown by the truth table.

Features

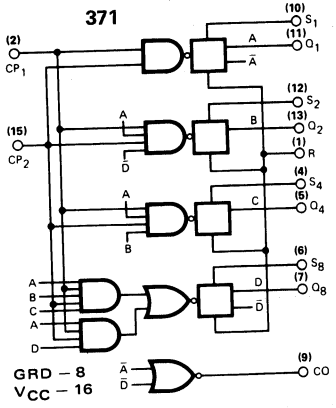
- DIRECT PRESET OR RESET TO ZERO
- TWO CLOCK LINES FACILITATE INPUT ENABLE
- NINTH COUNT (371) AND 15TH COUNT (372) OUTPUTS FOR CASCADING
- 1 MHz TYPICAL TOGGLE RATE

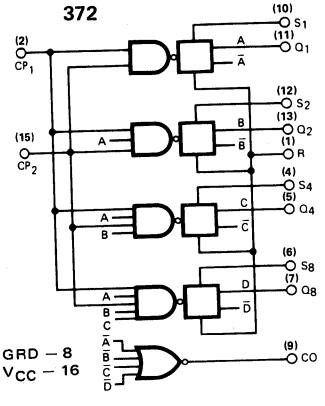
General Descriptions

The 371 is a master-slave decade counter that generates BCD outputs. It also provides two clock inputs to facilitate input enable control, direct set and reset inputs, and a ninth count output (carry output) so 371 cascades can generate counts of 100, 1,000, and so forth. Its outputs are ideal as inputs to the 380, 381, or 382 BCD to decimal decoders.

The 372 master-slave counter generates 4-bit binary outputs from 0 to 15 in the standard 1-2-4-8 binary code. It also provides two clock inputs to facilitate input enable control, direct set and reset inputs, and a 15th count output (carry output) to allow cascading to N binary stages.

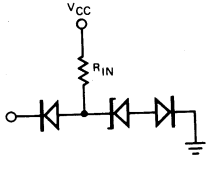
Logic Diagrams





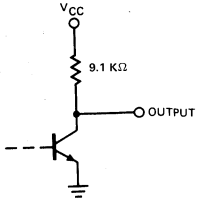
Equivalent Circuits

TYPICAL INPUT



INPUT	R_{IN}
CP_1 CP_2	5 KΩ TYP.
RESET	**20 KΩ TYP.**
ALL SETS	20 KΩ TYP.

TYPICAL OUTPUT



14

Truth Tables

371

CP_1 or CP_2	Q_1	Q_2	Q_4	Q_8	CO
0	0	0	0	0	0
1	0	0	0	0	0
0	1	0	0	0	0
1	1	0	0	0	0
0	0	1	0	0	0
1	0	1	0	0	0
0	1	1	0	0	0
1	1	1	0	0	0
0	0	0	1	0	0
1	0	0	1	0	0
0	1	0	1	0	0
1	1	0	1	0	0
0	0	1	1	0	0
1	0	1	1	0	0
0	1	1	1	0	0
1	1	1	1	0	0
0	0	0	0	1	0
1	0	0	0	1	0
0	1	0	0	1	0
1	1	0	0	1	0
0	0	1	0	1	0
1	0	1	0	1	0
0	1	1	0	1	0
1	1	1	0	1	1

372

CP_1 or CP_2	Q_1	Q_2	Q_4	Q_8	CO
0	0	0	0	0	0
1	0	0	0	0	0
0	1	0	0	0	0
1	1	0	0	0	0
0	0	1	0	0	0
1	0	1	0	0	0
0	1	1	0	0	0
1	1	1	0	0	0
0	0	0	1	0	0
1	0	0	1	0	0
0	1	0	1	0	0
1	1	0	1	0	0
0	0	1	1	0	0
1	0	1	1	0	0
0	1	1	1	0	0
1	1	1	1	0	0
0	0	0	0	1	0
1	0	0	0	1	0
0	1	0	0	1	0
1	1	0	0	1	0
0	0	1	0	1	0
1	0	1	0	1	0
0	1	1	0	1	0
1	1	1	0	1	0
0	0	0	1	1	0
1	0	0	1	1	0
0	1	0	1	1	0
1	1	0	1	1	0
0	0	1	1	1	0
1	0	1	1	1	0
0	1	1	1	1	0
1	1	1	1	1	1

Specifications

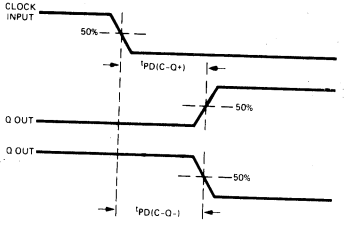
I_{CC} (WORST-CASE)	41 mA @ 13V, 53 mA @ 16V			
t_{PD} I/O FUNCTION FOR t_{PD}	600 ns S+Q+	200 ns R+Q−	800 ns C−Q+	300 ns C−Q−

TYPICAL TOGGLE RATE IS 1 MHz

Note: I_{CC} is tested at V_{CC} + 1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range. t_{PD} is guaranteed at $V_{CC} \pm 1$ V and across the applicable temp range with the output loaded with 5 unit loads.

See page 12 for electrical summary data.

Switching Time Waveforms



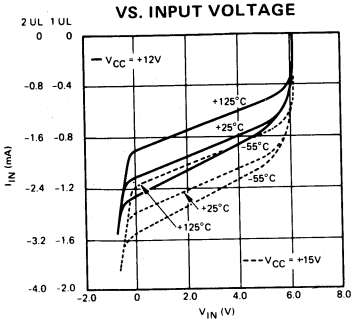
Loading Table

371/372

PINS	FUNCTION	LOADING
CP	Clock inputs	2 UL
R	Direct reset input	1 UL
S	Direct set input	1 UL
CO	Carry output	2 UL
Q	Outputs	5 UL

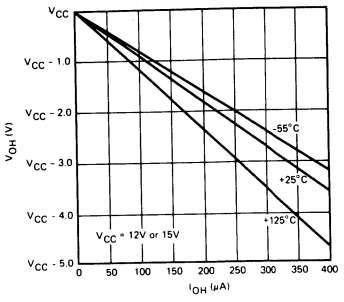
Typical Performance Characteristics

INPUT CURRENT VS. INPUT VOLTAGE

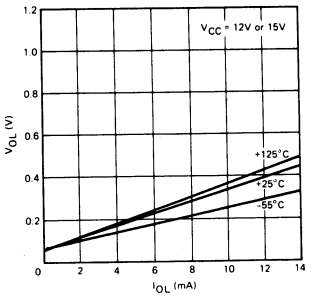


OUTPUT CURRENT VS OUTPUT VOLTAGE

OUTPUT HIGH



OUTPUT LOW



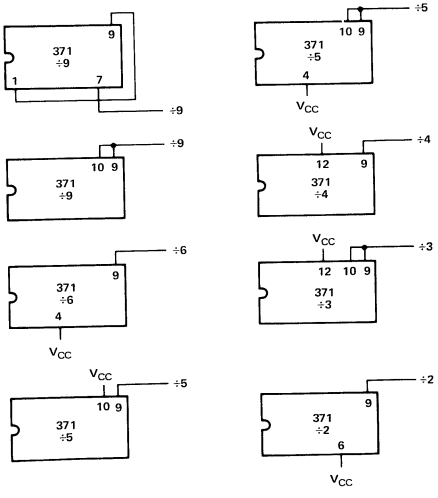
Typical Applications

The 371 counts as the clock goes from high to low. Setting or resetting must be done only with the clock line low (either clock). To set, or to reset the device to zero, the desired set or reset line is switched high. The count operation is inhibited by grounding either clock input, allowing one clock input to be an enable control. All unused direct set and reset pins should be grounded.

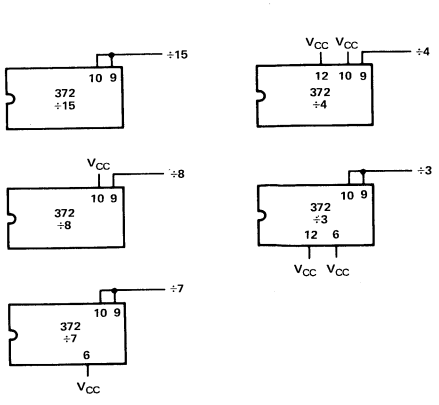
Except for the different internal gating, to provide hexadecimal counting, the operation of the 372 is the same as the operation of the 371.

COUNTER MODES

371



372



14

TSC373/374
Up-Down Counters
- Decade
- Hexadecimal

Features

Choice of Output – Decade (373)
Or Hexadecimal (374)

High Noise Immunity – 3.5 Volts Min

Carry And Borrow Outputs For N-Bit Cascading

Clear Input Is Independent Of Count And Load

Individual Preset To Each Flip-Flop

Synchronous Operation

General Description

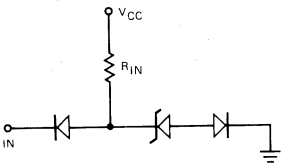
The 373/374 is a synchronous reversible (up/down) counter featuring master-slave flip-flops with active outputs. The outputs of the flip-flops are triggered by a low-to-high level transition of either of two clock inputs while the other is high. Pulsing one clock input causes the device to count up, while pulsing the other causes it to count down.

Provision has been made for setting information into the flip-flops. Whenever the load enable input is low, the flip-flop outputs will change to agree with the data inputs (independently of the count pulses). A master reset input resets all flip-flops to zero whenever it is high (regardless of the count and load inputs). Borrow and carry outputs are provided to allow cascading.

The 373 is a decade and the 374 a hexadecimal counter.

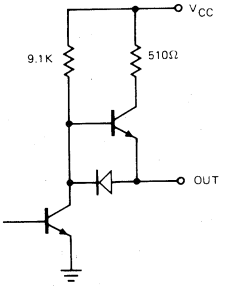
Equivalent Circuits

Typical Input



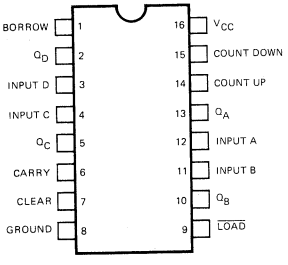
Input	R_{IN} (Typ)
CLEAR, LOAD	10K
DATA A, B, C, D	18K
CLOCK	10K

Typical Output



Connection Diagram

L Package
16 Lead Ceramic DIP



Order Part Numbers:
373AL, 374AL
(V_{CC} = 15V ±1V,
$-30°C \leq T_A \leq +70°C$)

373CL, 374CL
(V_{CC} = 12V ±1V, –30°
$-30°C \leq T_A \leq +85°C$)

14

Absolute Maximum Ratings

	Ceramic Package
Continuous Supply Voltage	16.5V
Pulsed Supply Voltage (less than 100 ms)	18V
Input Voltage (any input)	−0.5 to +18V
Surge Sink Current (less than 100 ms at 25°C T_A)	20mA
Storage Temperature	−65°C to +150°C
Lead Temperature (1/16 inch from case 10ns max)	300°C

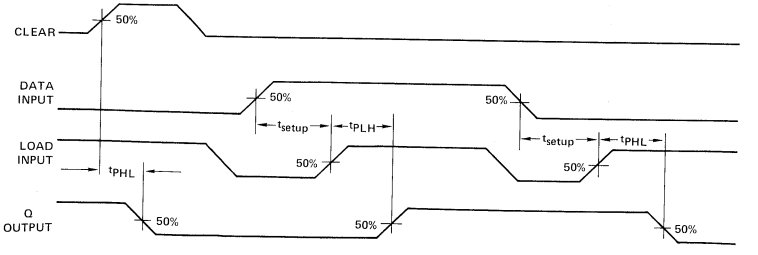
Note: Exceeding the absolute maximum ratings may cause permanent damage. Function of HiNIL devices at the absolute maximum ratings or beyond the conditions guaranteed is not implied.

Electrical Characteristics

Parameter	Definition	Type C V_{CC} = +12V ± 1.0V	Type A V_{CC} = +15V ± 1.0V	Test Condition
V_{INL}	Input Threshold Voltage, Low	5.0V Min	5.0V Min	Guaranteed Input Low Threshold
V_{INH}	Input Threshold Voltage, High	6.5V Max	6.5V Max	Guaranteed Input High Threshold
I_{INL}	Input Current, Low	−2.1mA Max	−2.6mA Max	At V_{CC} Max with $V_{IN} = V_{OL}$
I_{INH}	Input Leakage Current	10μA Max	10μA Max	At V_{CC} Max with $V_{IN} = V_{CC}$ Max
V_{OL}	Output Low Voltage	1.5V Max	1.8V Max	I_{OL} = 5 U.L. (1 U.L. = I_{INL})
V_{OH}	Output High Voltage	10V Min	13V Min	I_{OH} = 5 U.L. (1 U.L. = I_{INH})
V_{OHL}	Output High Voltage, Loaded	7.0V Min	9.5V Min	At V_{CC} Nominal, I_{OHL} = 5.0mA
I_{CC}	Power Supply Current	50mA Max	55mA Max	At V_{CC} Max Worst Case Condition (Q Outputs Low)
f_{MAX}	Max Input Count Freq.	1 MHz	1 MHz	Output Loaded with 5 U.L.
t_{setup}	Data to Load	250ns Min	250ns Min	
t_{PLH}	Count Up to Carry	425ns Max	425ns Max	t_{PLH} and t_{PHL} Based on Low to High (or High to Low) Transition of Output.
t_{PHL}		275ns Max	275ns Max	
t_{PLH}	Count Down to Borrow	525ns Max	525ns Max	
t_{PHL}		275ns Max	275ns Max	
t_{PLH}	Either Count to Q	725ns Max	725ns Max	
t_{PHL}		275ns Max	275ns Max	
t_{PLH}	Load to Q	725ns Max	725ns Max	
t_{PHL}		275ns Max	275ns Max	
t_{PHL}	Clear to Q	525ns Max	525ns Max	

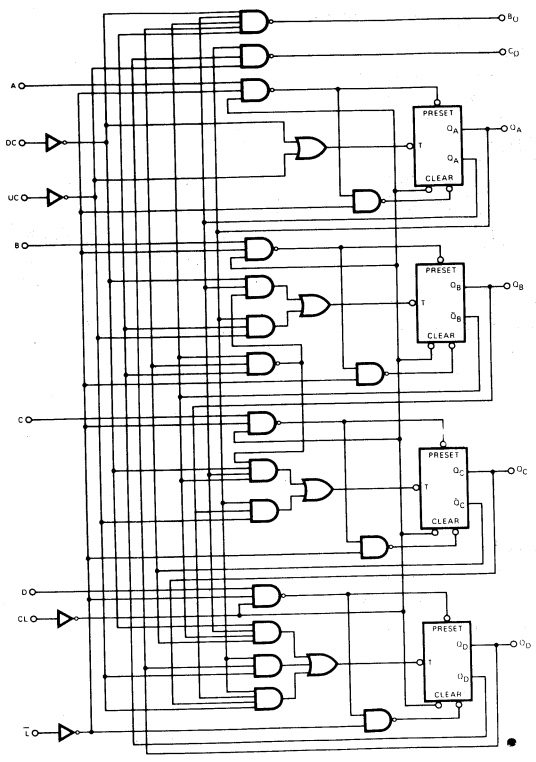
Note: I_{CC} is tested at V_{CC} (+13V for C type and +16V for A type) and is guaranteed across the applicable temperature range.

Switching Waveforms

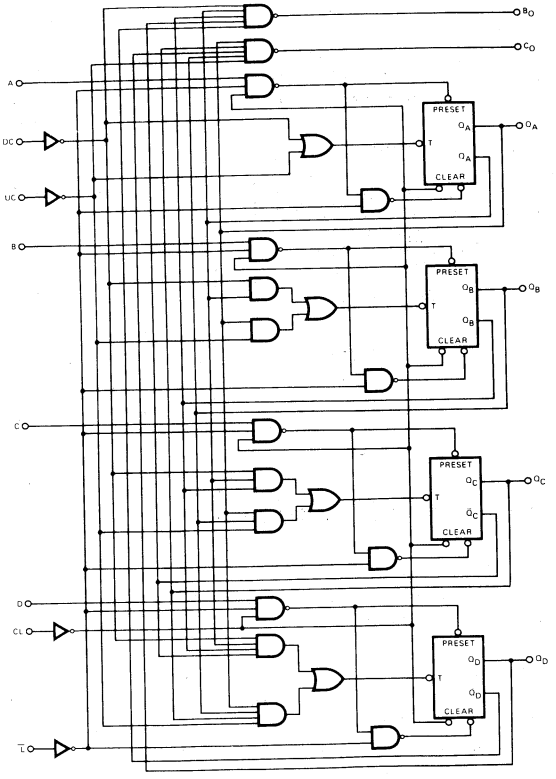


Logic Diagrams

373



374

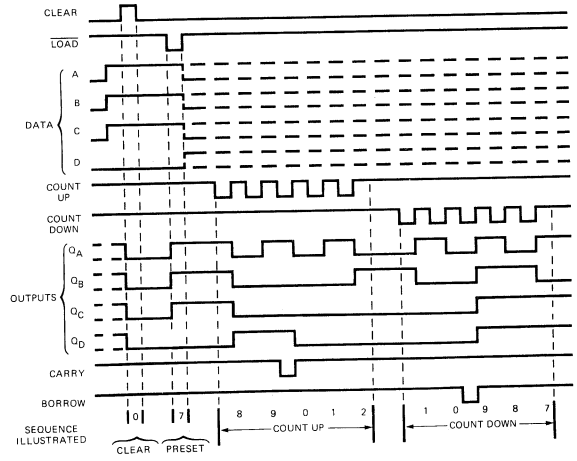


Timing Diagrams

373

The following sequence is illustrated below:

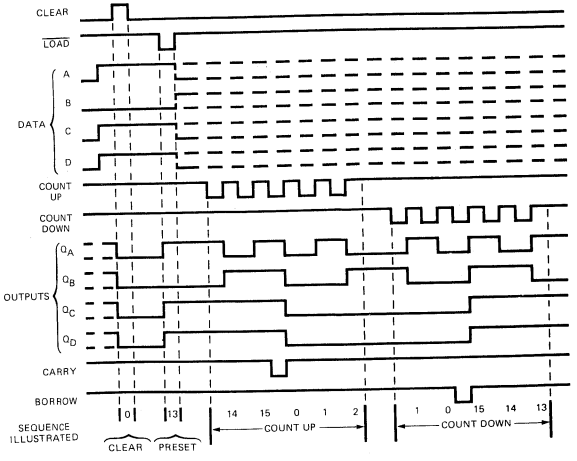
1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, (carry), zero, one, and two.
4. Count down to one, zero, (borrow), nine, eight, and seven.



374

The following sequence is illustrated below:

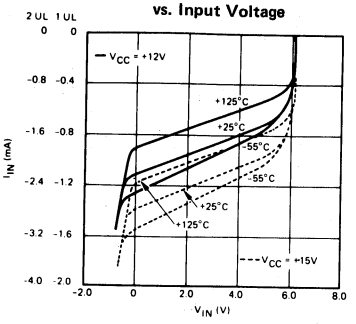
1. Clear outputs to zero.
2. Load (preset) to BCD thirteen.
3. Count up to fourteen, fifteen, (carry), zero, one, and two.
4. Count down to one, zero, (borrow), fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides loads, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

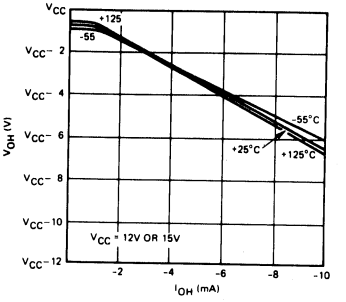
Typical Characteristics

Input Current vs. Input Voltage

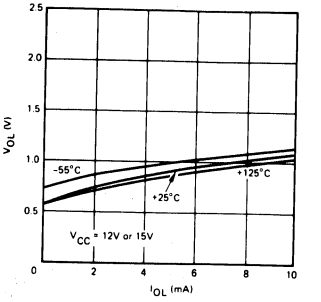


Output Current vs. Output Voltage

Output High



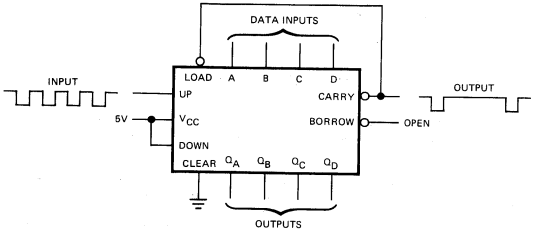
Output Low



Applications Information

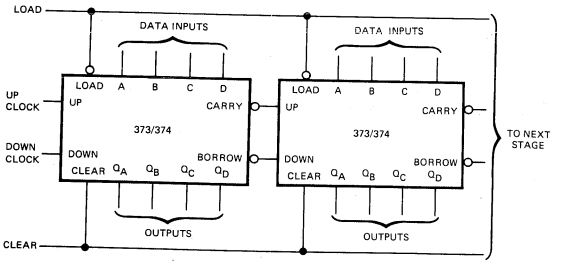
Modulo-N Divider

The 374 can be used to divide an incoming count frequency by any integral number (N) from one to 16. This is done by modifying the count frequency occurring at the carry output by presetting the data inputs to 16 minus N. Connect the carry output to the load input and the counter will count to the maximum state (15). The data inputs will then be enabled on the succeeding clock pulse. The counter outputs are then preset to the levels applied at the data inputs and the count sequence is repeated. The 373 may be used in the same manner to perform division by any number from 1 to 10.



Cascading

Circuitry is provided internally for cascading these counters. No external components are required. The mode shown below is ripple borrow/carry.



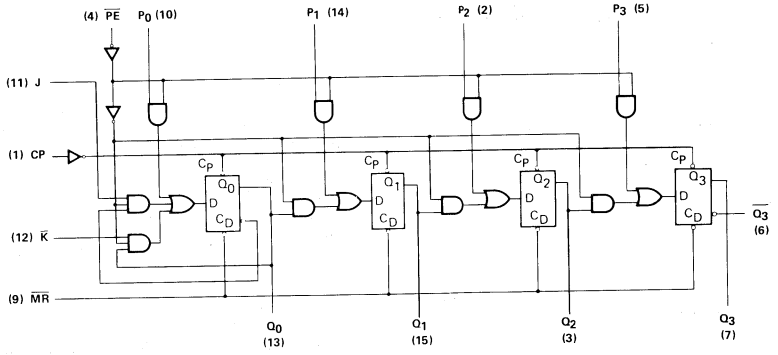
Features

- 3.5 WORST CASE NOISE IMMUNITY
- SERIAL IN, SERIAL OUT, PARALLEL IN, PARALLEL OUT MODES
- FULL SYNCHRONOUS OPERATION OF ALL DATA INPUTS
- J$\overline{K}$ FIRST STAGE INPUTS AND Q AND $\overline{Q}$ LAST STAGE OUTPUTS FOR EASY CASCADE OPERATION
- OVERRIDING ASYNCHRONOUS COMMON RESET
- BUFFERED CLOCK INPUT – ONLY 1 UNIT LOAD (UL)
- 3MHz TYPICAL SHIFT RATE
- CAN BE USED AS FOUR INDEPENDENT "D" CLOCKED FLIP-FLOPS

General Description

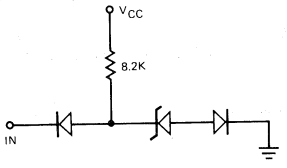
The 375 4-bit shift register is a universal shift register and storage element. It can be used with either serial or parellel inputs and either serial or parallel outputs. For increased flexibility, both parallels entry enable and master reset pins are provided. To facilitate serial entry and easy cascading to longer word lengths, J and $\overline{K}$ inputs have been provided as well as Q_3 and $\overline{Q}_3$ outputs.

Logic Diagram

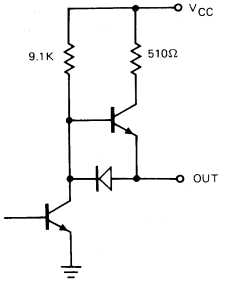


Equivalent Circuits

TYPICAL INPUT



TYPICAL OUTPUT



Truth Tables

	$\overline{PE}$	P_0	P_1	P_2	P_3	J	$\overline{K}$	$\overline{MR}$
SERIAL ENTRY	1	X	X	X	X	See Tables II and III		1
PARALLEL ENTRY	0	See Table I				X	X	1

NOTE: X = Don't Care

TABLE I
PARALLEL ENTRY
$\overline{PE}$ = 0, $\overline{MR}$ = 1

D – INPUT (P_0, P_1, P_2, or P_3)	OUTPUT Q AT t_{n+1} (Q_0, Q_1, Q_2, or Q_3)
0	0
1	1

NOTE: (n + 1) indicates output state after next clock transition.

TABLE II
SERIAL ENTRY
$\overline{PE}$ = 1, $\overline{MR}$ = 1

J	$\overline{K}$	Q_0 at t_{n+1}
0	0	0
0	1	Q_0 at tn (no change)
1	0	$\overline{Q}_0$ at tn (toggles)
1	1	1

TABLE III
SERIAL ENTRY
$\overline{PE}$ = 1, $\overline{MR}$ = 1

J and $\overline{K}$ CONNECTED	Q_0 at t_{n+1}
0	0
1	1

Specifications

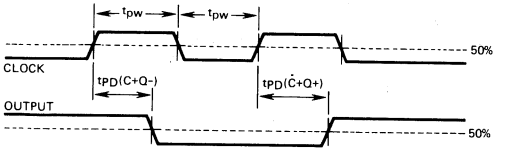
I_{CC} (worst case)	48 mA @ 13V, 64 mA @ 16V		
t_{PD}	550 ns	600 ns	600 ns
I/O Function for t_{PD}	CP+Q–	CP+Q+	$\overline{MR}$–Q–

NOTE: t_{PD} is guaranteed at $V_{CC} \pm 1$ V and across the applicable temp range with the output loaded with 3 unit loads.

See page 12 for electrical summary data.

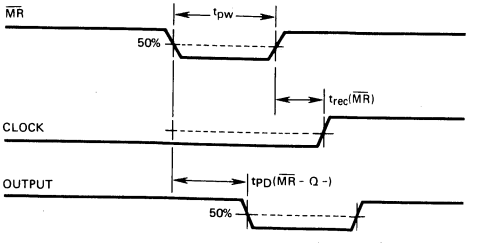
Switching Time Waveforms

Clock to Output Delays and Clock Pulse Width.



OTHER CONDITIONS: $J = \overline{PE} = \overline{MR} = H$
$\overline{K} = L$

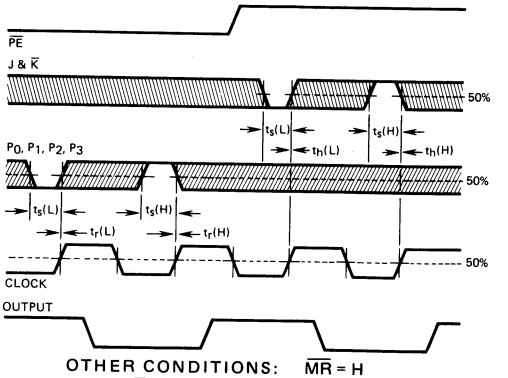
Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time.



OTHER CONDITIONS: $\overline{PE} = L$
$P_0 = P_1 = P_2 = P_3 = H$

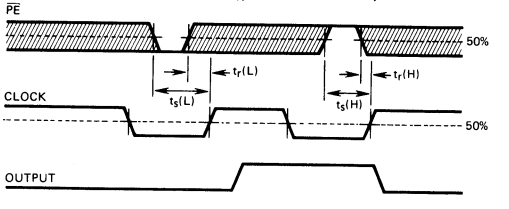
NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

Setup (t_s) and Hold (t_h) Time for Serial Data (J and $\overline{K}$) and Parallel Data (P_0, P_1, P_2 and P_3)



OTHER CONDITIONS: $\overline{MR} = H$
*J & $\overline{K}$ SETUP TIME AFFECTS Q_0 ONLY

Setup (t_s) and Hold (t_h) Time for $\overline{PE}$ Input.



OTHER CONDITIONS: $\overline{MR} = H, J = \overline{K} = L$
$P_0 = P_1 = P_2 = P_3 = H$

Switching Time Waveforms (contd.)

TIMING REQUIREMENTS

The following timing requirements apply across the applicable temperature range and V_{CC} spread:

CLOCK PULSE WIDTH t_{pw} (CP)	500 ns min.
DATA INPUT SETUP TIME t_s (DATA)	210 ns min.
DATA INPUT RELEASE TIME t_r (DATA)	0 ns min.
$\overline{PE}$ INPUT SETUP TIME t_s ($\overline{PE}$)	250 ns min.
$\overline{PE}$ INPUT RELEASE TIME t_r (PE)	0 ns min.
$\overline{MR}$ PULSE WIDTH t_{pw} ($\overline{MR}$)	300 ns min.
$\overline{MR}$ RECOVERY TIME t_{rec} ($\overline{MR}$)	220 ns min.

SETUP TIME is the minimum time required for the logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order for the flip-flops to respond.

RELEASE TIME is the minimum time that the logic level is required to be present at the logic input after the clock transition from LOW to HIGH in order for the flip-flops to respond.

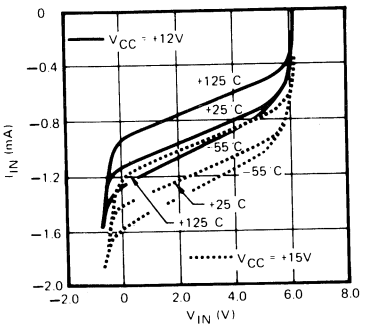
RECOVERY TIME is defined as the minimum time required between the end of the Reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH data to the Q outputs.

Loading Table

PINS	FUNCTION	LOADING
J, $\overline{K}$, P_0, P_1, P_2, P_3	Data Inputs	1 UL
$\overline{MR}$	Master Reset	1 UL
$\overline{PE}$	Parallel Enable	1 UL
CP	Clock	1 UL
Q_0, Q_1, Q_2, Q_3, $\overline{Q_3}$	All Outputs	3 UL

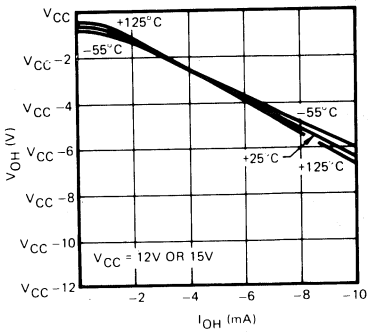
Typical Performance Characteristics

INPUT CURRENT VS. INPUT VOLTAGE

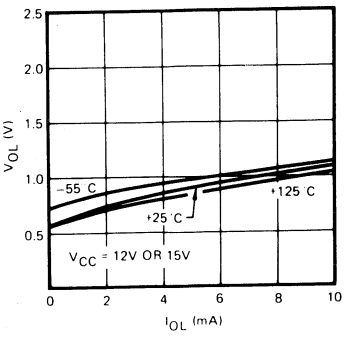


OUTPUT CURRENT VS. OUTPUT VOLTAGE

OUTPUT HIGH



OUTPUT LOW



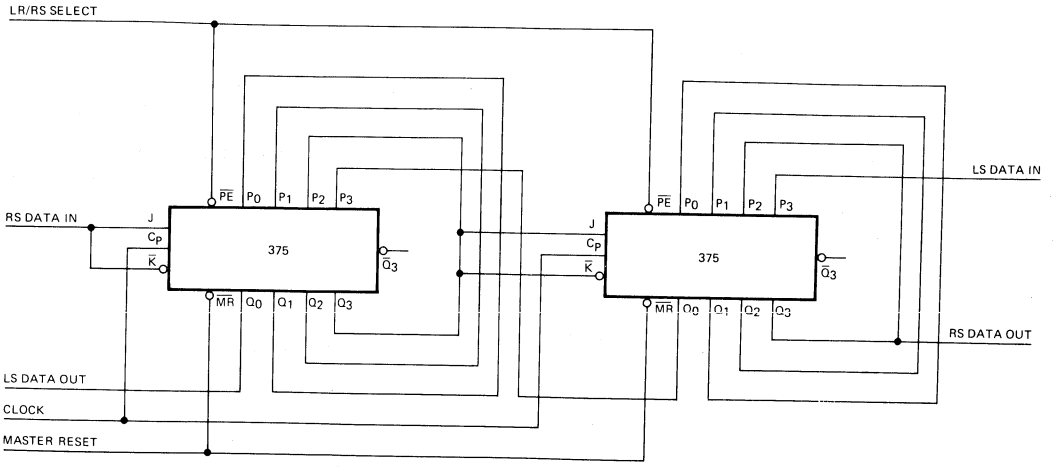
Typical Applications

The HiNIL 375 4-bit shift register is a universal shift register/storage register. It consists of four master-slave type D flip-flops and some gating circuits to make the device more flexible. The flip-flops are designed so that they will only change on a low-to-high transition of the clock signal. The D inputs of the flip-flops can be logically connected in one of two ways, determined by the state of the $\overline{PE}$ input. When PE is low, the inputs are controlled by the state of P_0, P_1, P_2, and P_3 inputs. Thus with $\overline{PE}$ low, the flip-flops are loaded directly through the parallel inputs. When $\overline{PE}$ is high, the D inputs of stages Q_1, Q_2, and Q_3 are connected to the outputs of Q_0, Q_1, and Q_2 respectively. The input of Q_0 is connected through suitable gating to provide $J\overline{K}$. Thus with $\overline{PE}$ high, the 375 operates as a shift right shift register. The $\overline{MR}$ input resets all flip-flops regardless of the clock and other input states. By wiring J and $\overline{K}$ together this set of inputs becomes a type D input for easy serial input. For similar reasons, a complementary output has been provided on the last flip-flop.

14

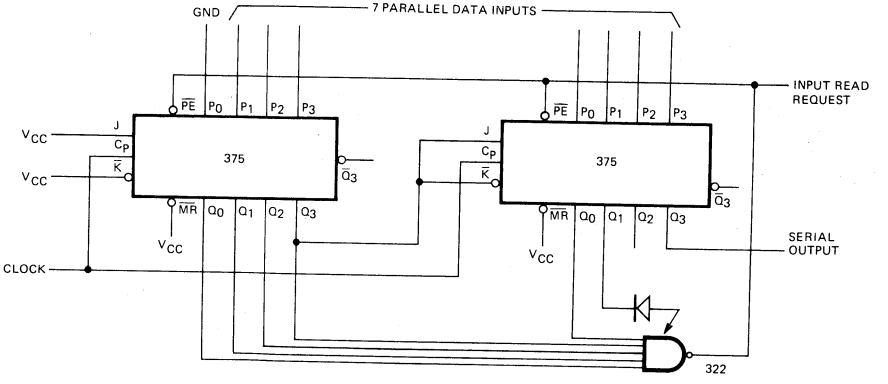
Typical Applications (contd.)

EIGHT BIT LEFT/RIGHT SHIFT REGISTER



This register uses the $\overline{PE}$ pin to select a left shift or a right shift mode. If this input is high, the normal shift-right operation is performed. If $\overline{PE}$ is low, the J$\overline{K}$ inputs are overriden and the flip-flops are loaded (through the parallel inputs) by the outputs of the following flip-flop, which corresponds to a shift-left operation.

SEVEN BIT PARALLEL TO SERIAL CONVERTER



This circuit operates with a continuous logic low on the P_0 input. Thus when the flip-flops are loaded through the parallel inputs, at least one of them will be in the low state and the output of the 322 will be forced high. This disables $\overline{PE}$ so further inputs will be through the serial J$\overline{K}$ inputs. Since both of these inputs are high, each clock pulse will load a logic ONE into the front end of the register. Thus the information previously loaded in the flip-flops will be shifted out, bit-by-bit, until the "0" bit loaded through P_0 reaches Q_2. The last bit of data is now at Q_3 (and hence the entire seven-bit word has been shifted out), and the 322 is now in a logic ZERO state. The next clock pulse will thus load another seven-bit word into the parallel inputs and the cycle will begin again.

TSC380/381
BCD-to-Decade Decoder/Drivers
- Lamp Driver
- Logic Driver

Features

- IDEAL LAMP DRIVER (380)
- NO AMBIGUOUS OUTPUTS
- OPEN COLLECTOR OUTPUTS OPERATE UP TO 24V (380)
- EACH OUTPUT CAN SINK UP TO 30 mA (380)
- USEFUL AS OCTAL DECODER, DEMULTIPLEXER AND COMMUTATOR
- COLLECTOR OR'ABLE

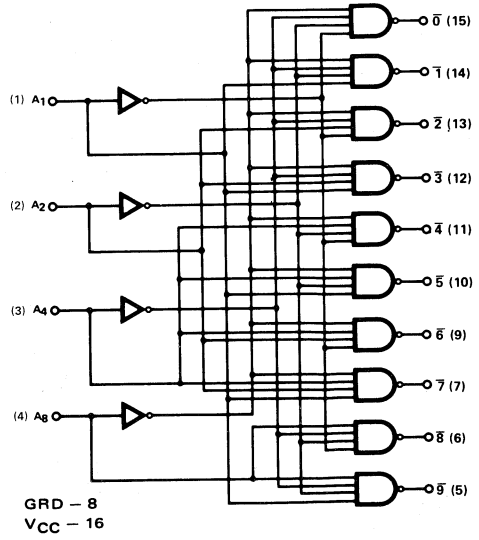
General Descriptions

The 380 decodes BCD inputs (1-2-4-8 code) and drives lamps and other devices requiring decoder outputs with high sink current at moderately high voltage.

The 381 decodes BCD inputs and provides active low outputs for low current lamps. Open collector outputs make the 381 useful in "wire-OR" logic systems and for interfacing with other logic families.

Since the 380/381 produce no ambiguous outputs, input codes for 10 to 15 will hold all outputs high. The 381 should be used with a pullup resistor. The outputs of the 371 decade counter are ideal 380/381 inputs. For high performance applications, use the 380 device.

Logic Diagram



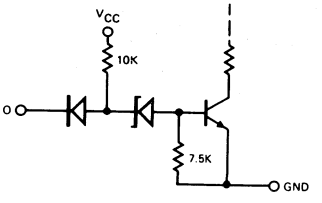
14

Truth Table

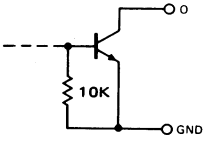
INPUTS				OUTPUTS									
A_1	A_2	A_4	A_8	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
0	1	0	0	1	1	0	1	1	1	1	1	1	1
1	1	0	0	1	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	1	1	0	1	1	1	1	1
1	0	1	0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
1	1	1	0	1	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
0	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

Equivalent Circuits

TYPICAL INPUT



TYPICAL OUTPUT



Specifications

380

I_{CC} (WORST-CASE)	24 mA @ 13V, 31 mA @ 16V

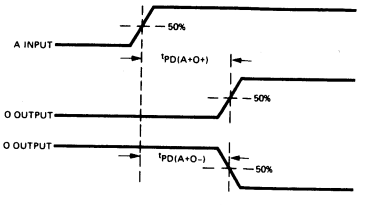
NOTE:
I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range.
See page 12 for electrical summary data.

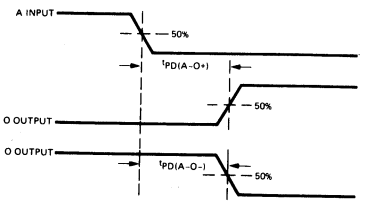
381

I_{CC} (WORST-CASE)	30 mA @ 13V, 38 mA @ 16V			
t_{PD} I/O FUNCTION FOR t_{PD}	500 ns A+Q+	400 ns A–Q+	500 ns A–Q–	300 ns A+Q–

NOTE:
I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range. t_{PD} os guaranteed at V_{CC} ±1V and across the applicable temp range with the output loaded with 8 unit loads.

Switching Time Waveforms





Loading Tables

380

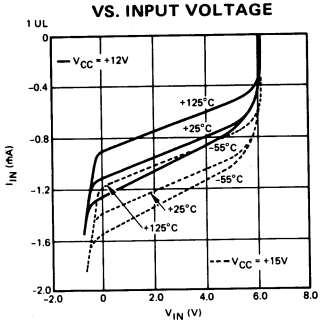
PINS	FUNCTION	LOADING
A 0-9	BCD inputs Outputs	1 UL Unit loading does not apply

381

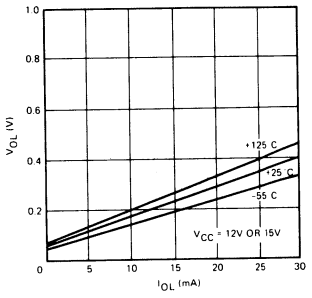
PINS	FUNCTION	LOADING
A O	BCD inputs Outputs	1 UL 8 UL with 8.2 KΩ pullup resistor

Typical Performance Characteristics

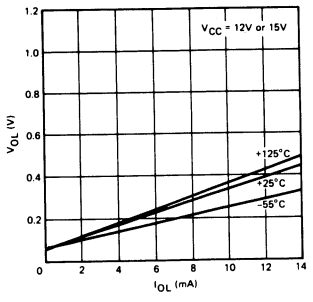
INPUT CURRENT VS. INPUT VOLTAGE



OUTPUT CURRENT VS OUTPUT VOLTAGE OUTPUT LOW 380



OUTPUT CURRENT VS OUTPUT VOLTAGE OUTPUT LOW 381

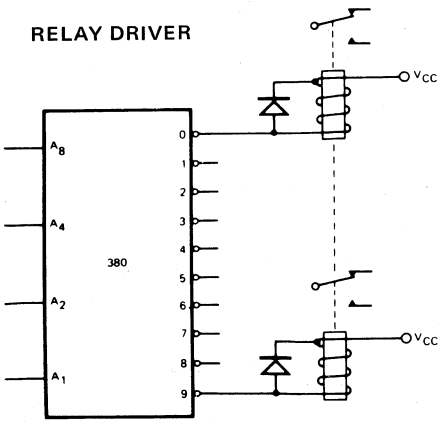


Typical Applications

The typical input and output circuits may be used to calculate interface designs. General instructions for using external resistors and calculating fanout with collectors OR'd are given in the applications notes. External resistors may be connected to a voltage other than V_{CC} to adjust the output voltage level.

In addition to straightforward BCD to decimal decoding, the 381 is useful in applications such as hexadecimal (1 of 16) decoding, octal decoding, demultiplexing, and controlling MOS analog switches. Its high noise immunity and adjustable output level makes it an excellent interface on noisy data communications lines.

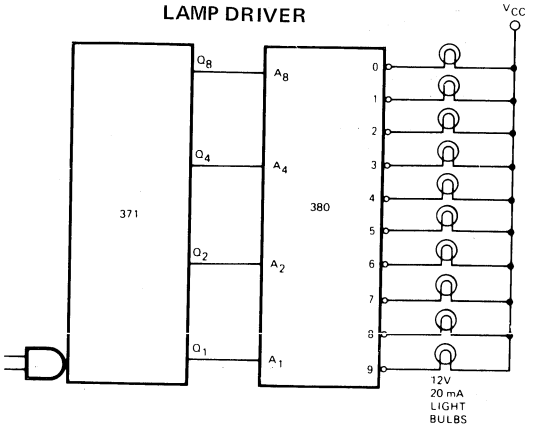
RELAY DRIVER



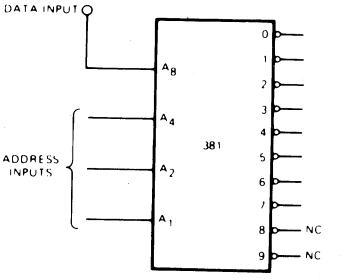
14

Typical Applications (contd.)

LAMP DRIVER

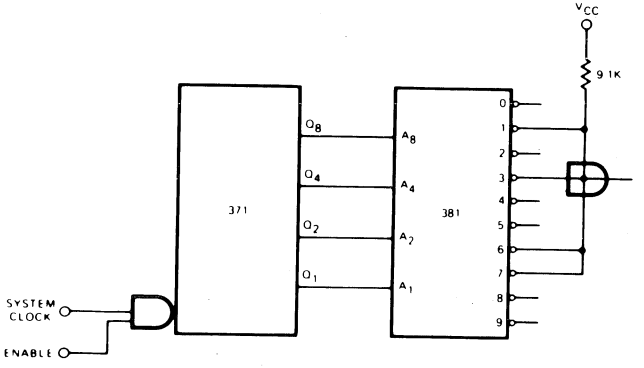


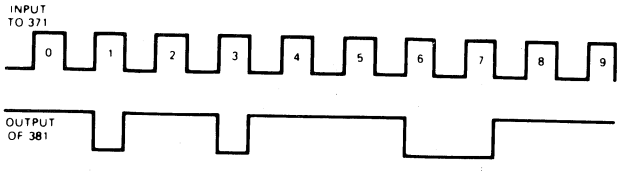
EIGHT-CHANNEL DEMULTIPLEXER



If data is applied to the A_8 input in the octal decoding mode, the outputs 0 through 7 selected by A_1, A_2 and A_4 will have the same states as the data. Thus, the serial output of an 8-channel multiplexer may be demultiplexed by using A_1–A_4 as address inputs synchronized with the multiplexer channel-select signals.

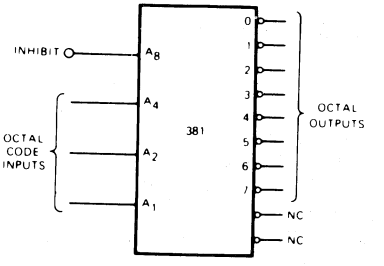
MINTERM AND TIMING PULSE GENERATORS





When several outputs of the 381 are collector-OR'd a low level on any of the OR'd outputs will produce a low output. Thus, it operates as a minterm generator governed by the states of the A_1 through A_8 inputs. If the inputs are cycled by a counter, as shown above, the 381 generates pulse trains with pulse trains with lengths governed by the clock frequency and the number of adjacent outputs OR'd. This is an extremely flexible way of generating odd combinations of control timing pulses.

OCTAL DECODER



Since outputs 8 and 9 are continuously high if the A_8 input is low, grounding A_8 converts the 381 to an octal decoder.

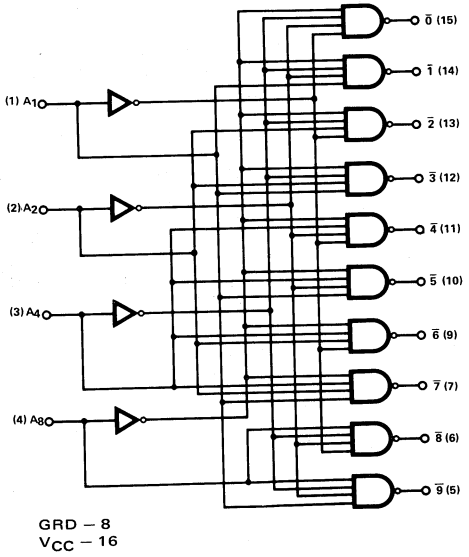
Features

- NO AMBIGUOUS OUTPUTS
- BLANKING MODE
- 70 VOLT OUTPUT CAPABILITY
- 7 mA CATHODE CURRENT CAPABILITY

General Description

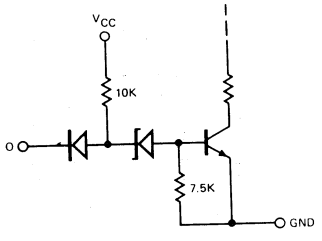
The 382 decodes BCD inputs (1-2-4-8 code) and drives the 10 segments of a gas filled, cold cathode indicator tube. Since the 382 produces no ambiguous outputs, input codes for 10 to 15 will blank the tube. The outputs of a 371 decade counter are ideal as 382 inputs for display control.

Logic Diagram

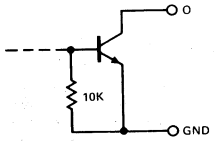


Equivalent Circuits

TYPICAL INPUT



TYPICAL OUTPUT



14

Truth Table

INPUTS				OUTPUTS									
A_1	A_2	A_4	A_8	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
0	1	0	0	1	1	0	1	1	1	1	1	1	1
1	1	0	0	1	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	1	1	0	1	1	1	1	1
1	0	1	0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
1	1	1	0	1	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
0	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
$\bar{0}$	$\bar{1}$	$\bar{1}$	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

Specifications

I_{CC} (WORST-CASE)	24 mA @ 13V, 31 mA @ 16V

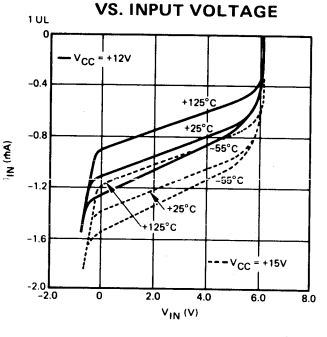
NOTE:
I_{CC} is tested at V_{CC} +1 Volt (+13V for C type and +16V for A type) and is guaranteed across the applicable temp range.
See page 12 for electrical summary data.

Loading Table

PINS	FUNCTION	LOADING
A	BCD inputs	1 UL
0-9	Outputs	Unit loading does not apply

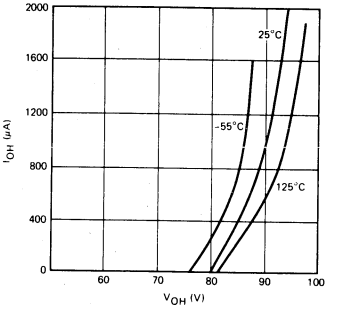
Typical Performance Characteristics

INPUT CURRENT VS. INPUT VOLTAGE

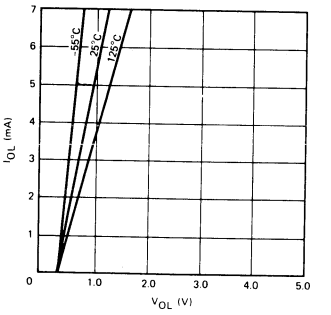


OUTPUT CURRENT VS OUTPUT VOLTAGE

OUTPUT HIGH



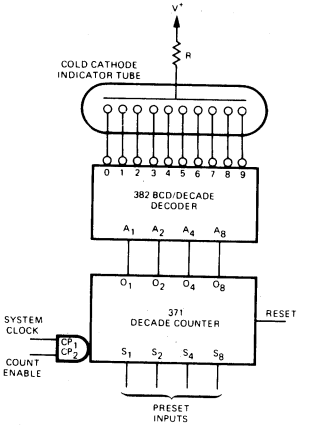
OUTPUT LOW



Typical Applications

The typical input and output circuits may be used to calculate interface designs.

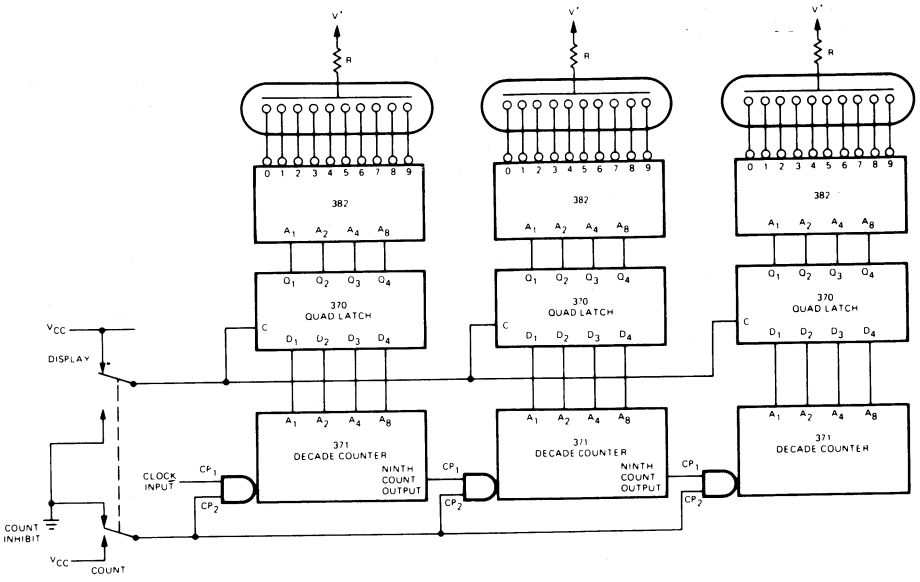
COUNTING-DISPLAY SYSTEM



The 382 is used here to drive a cold cathode indicator tube. The circuit will count system clock pulses as long as the count enable line is held high. The counter can be reset, or a number preset into the counter by taking the reset/preset inputs high. During normal operation they should be held low. This setting/presetting operation should be done only with the count enable line low. The values for V^+ and R can be determined from the manufacturer's literature published on the indicator tube.

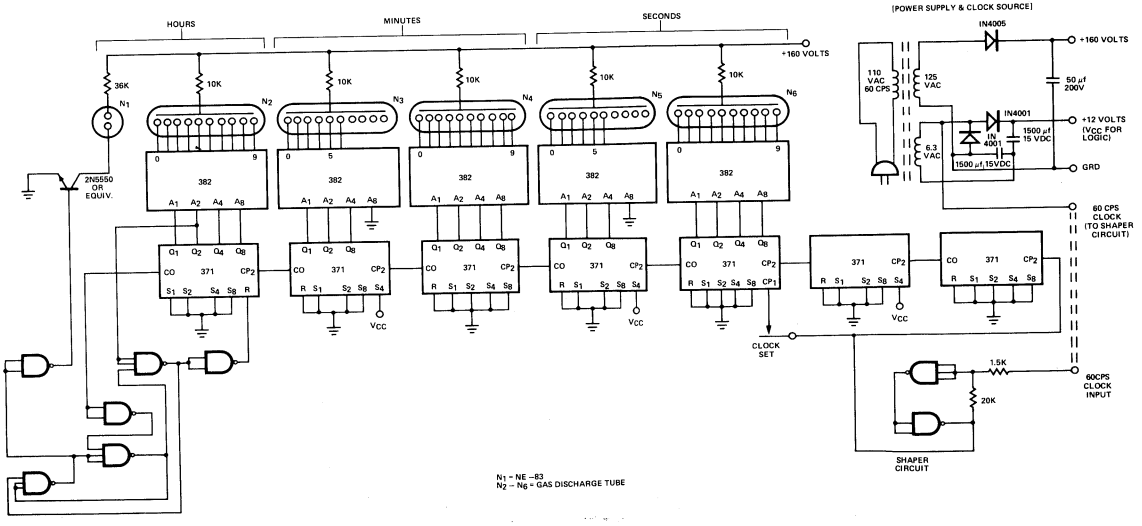
Typical Applications (con't)

SAMPLE AND HOLD DISPLAY SYSTEM



This circuit counts, stores, and displays the count. When the switch is in the count position, the decade counters count clock pulses and the indicator tubes display the count being held in the quad latches. When the switch is moved to the display/count inhibit position the counters stop counting; the number at which they were stopped is transferred to storage and the display tubes change to the new number. If the switch is then returned to its original position the circuit will resume counting.

MINIMUM LOGIC DIGITAL CLOCK



14

Features

- 40 mA OUTPUT SINK CAPABILITY
- BLANKING CAPABILITY PROVIDED
- LAMP TEST INPUT
- PIN AND FUNCTION EQUIVALENT OF TTL 7447A

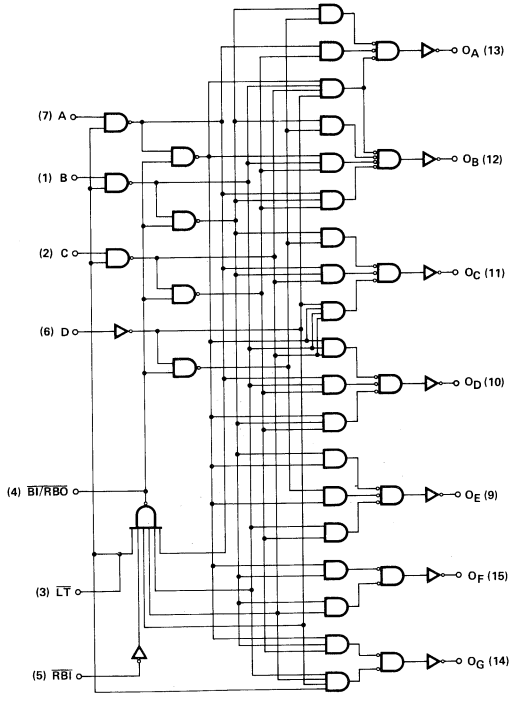
General Description

This device is characterized by seven open-collector outputs corresponding to the segments in LED display units such as the Monsanto Man-1. A 4-bit binary code applied to the data inputs causes the outputs to turn on in the conventional 7 segment code.

A blanking input is provided that turns all of the outputs off whenever it is low (regardless of the state of any other inputs). Also provided is a lamp test input that can be operated whenever the blanking input is high. A logical zero on the lamp test input will turn all seven outputs on. A ripple-blanking input is provided that has no effect except when each of the four data inputs are at logic zero. Then if the ripple-blanking input is at zero, when (and only when) the four data inputs are at zero, all seven outputs will be at logic one (display off). If the ripple-blanking input is at logic one (and the four data inputs are at zero), all outputs except O_G will be at zero ("0" displayed). If any of the data inputs are at logic one, the ripple-blanking input will have no effect.

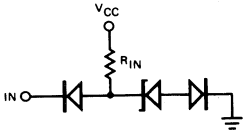
One pin brought out from the internal logic of the device can be used as either an input or an output. If the blanking input/ripple-blanking output is tied low (treating the pin as an input), all seven outputs will be at logic one. If the lamp test input is at one and the ripple-blanking input and the four data inputs are at zero, the ripple-blanking output will be at zero and the seven other outputs will be high.

Logic Diagram

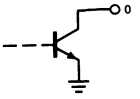


Equivalent Circuits

TYPICAL INPUT



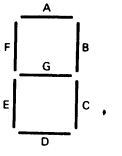
TYPICAL OUTPUT



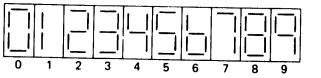
14

Truth Table

DECIMAL OR FUNCTION	INPUTS $\overline{LT}$	$\overline{RBI}$	D	C	B	A	$\overline{BI}$/RBO	OUTPUTS O_A	O_B	O_C	O_D	O_E	O_F	O_G
0	1	1	0	0	0	0	1	0	0	0	0	0	0	1
1	1	X	0	0	0	1	1	1	1	1	1	0	0	1
2	1	X	0	0	1	0	1	0	0	1	0	0	1	0
3	1	X	0	0	1	1	1	0	0	0	0	1	1	0
4	1	X	0	1	0	0	1	1	0	0	1	1	0	0
5	1	X	0	1	0	1	1	0	1	0	0	1	0	0
6	1	X	0	1	1	0	1	1	1	0	0	0	0	0
7	1	X	0	1	1	1	1	0	0	0	1	1	0	1
8	1	X	1	0	0	0	1	0	0	0	0	0	0	0
9	1	X	1	0	0	1	1	0	0	0	1	1	0	0
10	1	X	1	0	1	0	1	1	1	1	0	0	1	0
11	1	X	1	0	1	1	1	1	1	0	0	1	1	0
12	1	X	1	1	0	0	1	1	0	1	0	1	0	0
13	1	X	1	1	0	1	1	0	1	0	0	1	0	0
14	1	X	1	1	1	0	1	1	1	1	0	0	0	0
15	1	X	1	1	1	1	1	1	1	1	1	1	1	1
$\overline{BI}$	X	X	X	X	X	X	0	1	1	1	1	1	1	1
$\overline{RBI}$	1	0	0	0	0	0	0	1	1	1	1	1	1	1
$\overline{LT}$	0	X	X	X	X	X	1	0	0	0	0	0	0	0



SEGMENT IDENTIFICATION



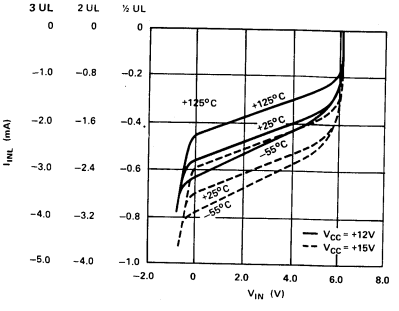
Loading Table

PINS	FUNCTION	LOADING
A,B,C,D	Inputs	1 UL
$\overline{RBI}$	Ripple-Blanking Input	1 UL
$\overline{LT}$	Lamp Test	3 UL
$\overline{BI}$	Blanking Input	2 UL
$O_{A\text{-}G}$	Outputs	See Electrical Characteristics
RBO	Ripple-Blanking Output	2 UL

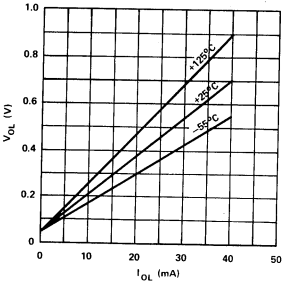
See page 20 for general electrical characteristics.

Typical Performance Characteristics

INPUT CURRENT VS. INPUT VOLTAGE



OUTPUT CURRENT VS. OUTPUT VOLTAGE OUTPUT LOW



Typical Applications

This device is characterized by seven open-collector outputs corresponding to the segments in LED display units such as the Monsanto Man-1. A 4-bit binary code applied to the data inputs causes the outputs to turn on in the conventional 7-segment code.

CURRENT LIMITING RESISTORS

LED displays require that the current through them be limited by series resistors. The maximum current flow may be determined by either the LED display or the 383. Since the 383 is specified for 20 mA max. continuous duty (40 mA max. 50% duty cycle), displays that require their current to be held to 20 mA or less should have their resistor values calculated on the basis of the max. display current. Displays that must be limited to currents greater than 20 mA should have their resistor values calculated on the basis of the 20 mA max. current of the 383 (strobed applications will be considered separately).

Sample calculation — Monsanto MAN-1 has a 20 mA max. forward current and a voltage drop per segment of 3.4V typ.

$$R_{LIM} = \frac{V_{CC} - V_F - V_{OL}}{I_F} = \frac{13.0V - 3.4V - 0.7V}{20\ mA} = 445\Omega \quad \text{(Fig. 1)}$$

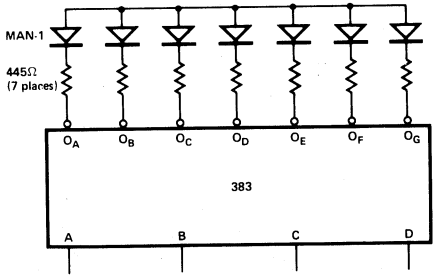
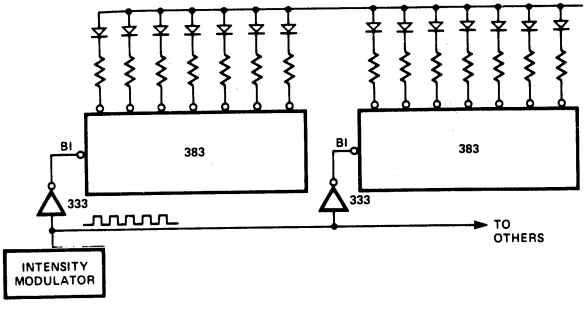


Figure 1.



STROBING OPERATION

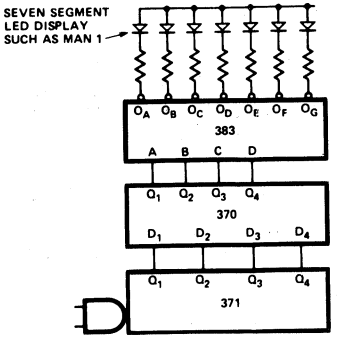
One popular technique for increasing the apparent brightness of displays is to pulse the displays with high currents and "average down" the power dissipation by lowering the duty cycle accordingly. The display manufacturers should be consulted as to the max. current vs. duty cycle that should be used with their units. The 383 should not be used with a display current of more than 40 mA NO MATTER WHAT THE DUTY CYCLE! Failure to observe this precaution can cause permanent damage to the device. In addition, the 40 mA figure should not be used unless the duty cycle is 50% or less. Limiting resistor values should be calculated on the basis of the strobed current.

Sample Calculation — Assume the MAN-1 display is to be run at the max. current allowed by the 383 — 40 mA @ 50% duty cycle.

$$R_{LIM} = \frac{V_{CC} - V_F - V_{OL}}{I\ STROBE} = \frac{13.0V - 3.6V - 1.2V}{40\ mA} = 205\Omega$$

The strobing operation itself is accomplished by use of the Blanking Input (Figure 2).

A suggested circuit for an intensity modulator is shown in Figure 3.



This application demonstrates the use of the 383 to drive seven-segment displays such as the man-1. Since each output of the 383 will sink 20 mA, the display can be driven directly without external components other than current limiting resistors. Also illustrated is the 370 quad latch and 371 decade counter being used to acquire and store the number to be displayed.

Figure 3. Intensity Modulator Circuit — Output duty cycle varies from 0% — 100% depending on switch setting.

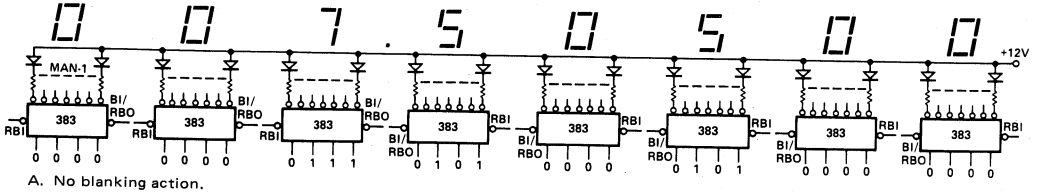
14

Typical Applications (contd.)

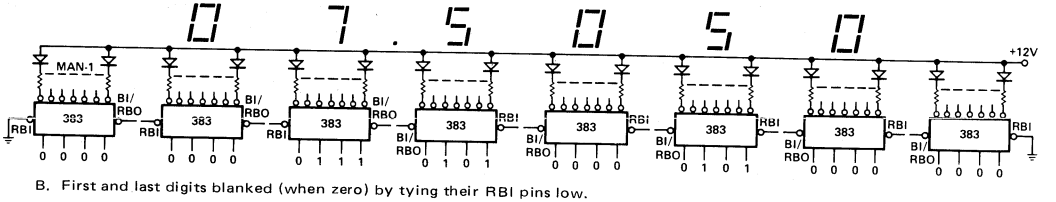
RIPPLE BLANKING

Provision has been made on the 383 for blanking out insignificant zeroes to increase legibility. Thus 007.50500 would be displayed at 7.505 if the ripple-blanking provisions were used. If the RBI pin is tied low, the display will be blanked every time a BCD zero is applied to the data inputs. This is normally done for the first and last digits of a display. In the previous example, 007.50500 would be displayed at 07.5050, the first and last digits being blanked since they are zero.

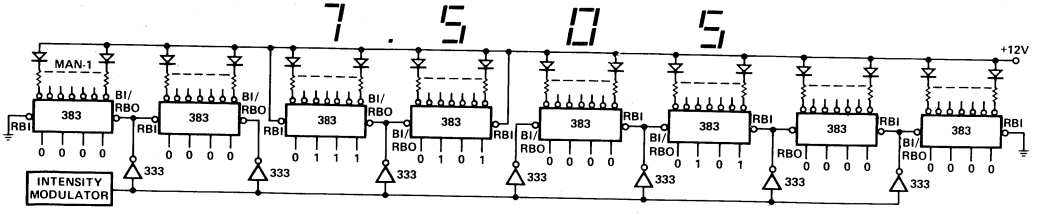
This scheme cannot be applied directly to all of the digits since it would cause 007.50500 to be displayed at 7.5_5. This problem is eliminated by the RBO output pin which delivers a logic zero whenever a BCD zero is on the data inputs. By feeding this information to the RBI inputs of the next 383, blanking will be accomplished only on nonsignificant zeroes. The RBO pin must be used with an 8.2k discrete pullup resistor.



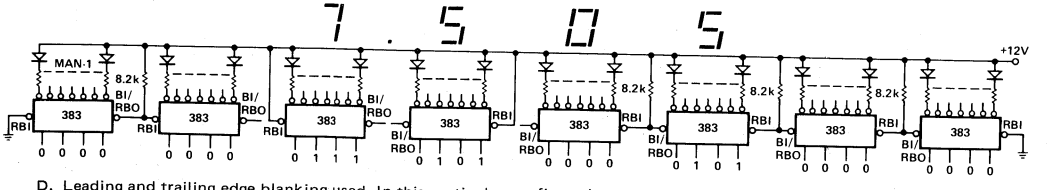
A. No blanking action.



B. First and last digits blanked (when zero) by tying their RBI pins low.



C. Leading and trailing edge blanking, combined with intensity modulation. Notice the 333's supply pullup resistors to the RBO pins, eliminating the need for discrete resistors.



D. Leading and trailing edge blanking used. In this particular configuration the digits adjacent to the decimal point will be displayed even if zero. This is usually considered desirable.

TSC390/391/392/393 394/395 Dual Interface Buffers

- Dual 2-Input NAND/AND/OR/NOR
- Dual 4-Input AND/NAND with Expander

Features

High Current Sink Capability – 250mA – Drives Relays, Lamps, Solenoids, Memories, Clock Lines

CMOS Compatible Inputs – $I_{IL} < 0.6mA$ at $V_{CC} = 10V$

Wide Operating Supply Range – 10 to 16V

High Noise Immunity – 3.5V Min at $V_{CC} = 11V$

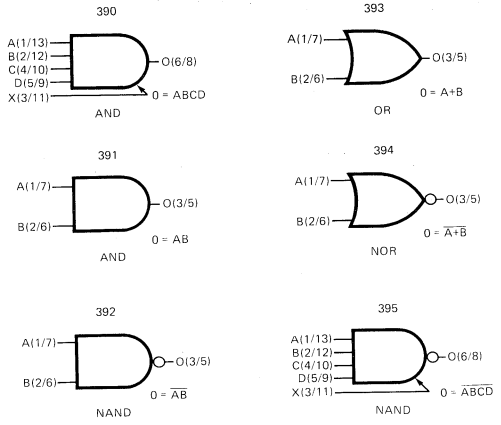
Full Range of Logic Functions Available

Dual Configuration – Saves Board Space, Package Count

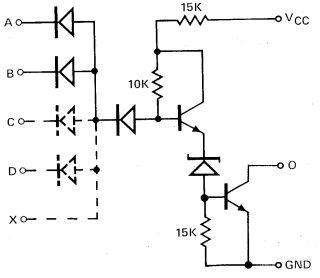
General Description

The HiNIL 390 to 395 Dual Interface Buffers offer open collector NPN transistor outputs with 20V sustaining voltage and high current sink capacity. Low input current and wide supply voltage range make these buffers ideal for interfacing with CMOS or with other HiNIL logic.

Logic Diagram (½ Circuit Shown)



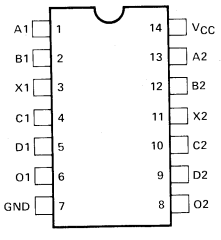
Equivalent Circuit



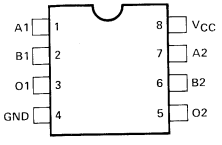
Connection Diagrams

Order Part Numbers:
390AL/CL, 395AL/CL
($-30°C \leq T_A \leq +70°C$)

L Package
14 Lead Ceramic DIP



L Package
8 Lead Ceramic DIP



Order Part Numbers:
391AL/CL, 392AL/CL
393AL/CL, 394AL/CL
($-30°C \leq T_A \leq +70°C$)

14

Absolute Maximum Ratings

Continuous Supply Voltage, V_{CC}	16.5V
Operating Supply Voltage Range, V_{CC}	10 to 16V
Pulsed Supply Voltage (less than 100ms)	18.0V
Output Voltage to GND (I_O less than 100μA)	30V
Input Voltage (any input)	−0.5 to +18V
Continuous Output Sink Current	250mA
Surge Output Sink Current (less than 100ms at 25°C T_A)	300mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−30°C to +70°C

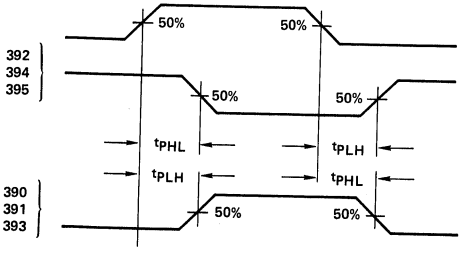
Electrical Characteristics (V_{CC} = 10 to 16V across applicable temperature range, unless otherwise specified)

Parameter	Definition	Limit	Conditions
V_{IH}	Input High Voltage	6.5V Max	V_{CC} = 10–16V
V_{IL}	Input Low Voltage	5V Min	V_{CC} = 10–16V
V_{OL}	Output Low Voltage	0.7V Max	I_{OL} = 250mA, V_{CC} = 10V, with V_{INH} = 6.5V and V_{INL} = 5.0V
I_{IH}	Input High Current	10μA Max	V_{CC} = 16V, V_{IN} = 16V
I_{IL}	Input Low Current	−1mA Max −0.6mA	V_{CC} = 16V, V_{IN} = 1.5V V_{CC} = 10V, V_{IN} = 1.5V
I_{CC}	Supply Current	40mA Max	V_{CC} = 16V
I_{CEX}	Open Collector Cutoff Current	100μA Max	V_{CC} = 16V, V_{CEX} = 30V
$V_{(BR)CER}$	Output Transistor Sustaining Voltage	20V Min	V_{CC} = 16V, I_{OH} = 10mA

AC Characteristics

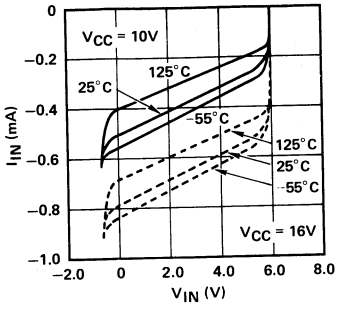
t_{PLH}	Propagation Delay, Output low to high	500ns Max	I_O = 200mA, R_L = 50Ω C_L = 15pF
t_{PHL}	Propagation Delay, Output high to low	200ns Max	I_O = 200mA, R_L = 50Ω C_L = 15pF

Switching Waveforms

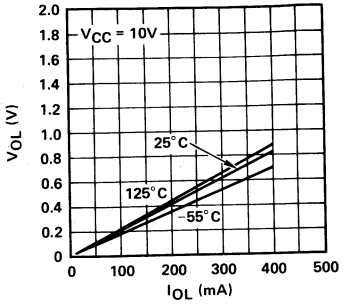


Typical Performance Characteristics

INPUT CURRENT
VS INPUT VOLTAGE



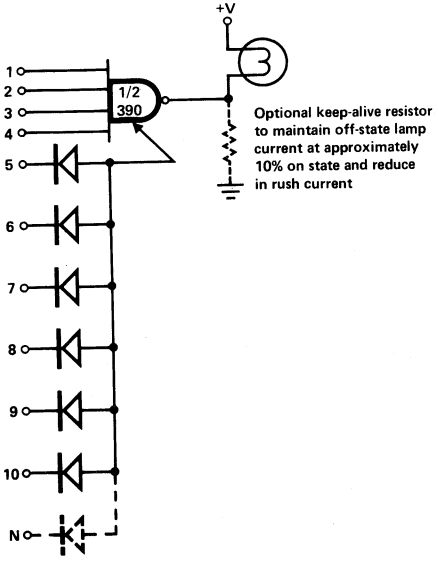
OUTPUT VOLTAGE LOW VS
OUTPUT CURRENT LOW



Typical Applications

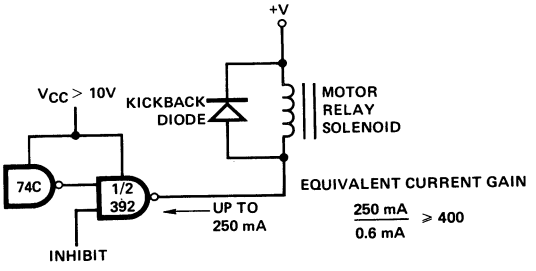
Multi-Input Short Circuit Indicator

If any of the N inputs are short circuited to ground the indicator lamp will turn on.



CMOS Super Output Buffer

390 series devices can be used to add extra output drive to CMOS circuitry. With inductive loads a kickback diode is recommended to prevent high voltage surges from damaging the device when it switches high.



14

TSC396
Line Driver/Receiver
• Dual Differential

Features

Differential Inputs and Outputs

Internal Bias, Reference and Hysteresis Sources

Low Output Impedance

Useful for Single-Wire Input/Output Applications

MOS Compatible Inputs

Power Supply Range of 11V to 16V

Applications

Differential Line Driver or Line Receiver

Line Repeater

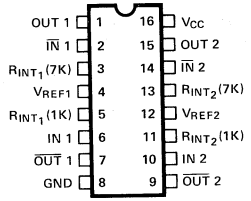
Single-Ended Line Driver or Line Receiver

Alternate to Motorola MC696

General Description

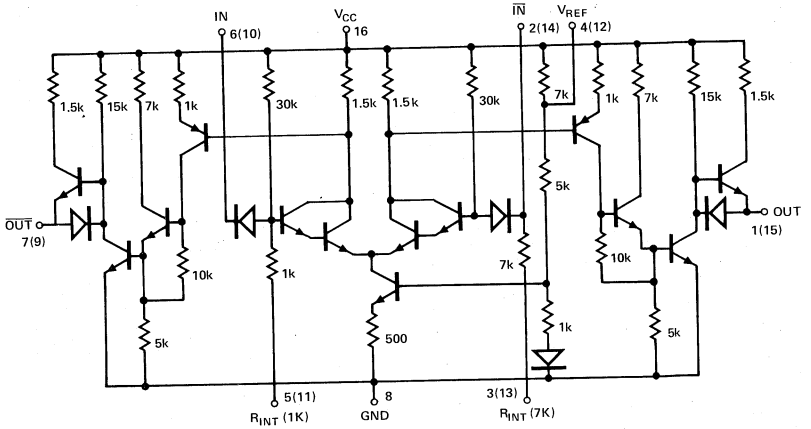
The 396 dual differential line driver/receiver is designed for industrial logic applications requiring high immunity to electrical noise. The 396 has an extremely flexible hysteresis capability, allowing the user to adjust the switching threshold. Thus the 396 is also useful for single-wire input/output applications.

Connection Diagram

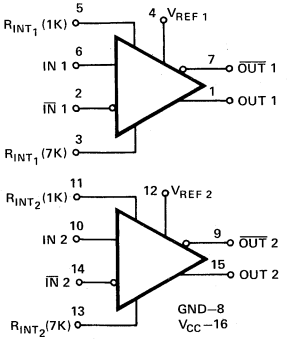


16-LEAD DIP

Schematic Diagram



Block Diagram



14

Absolute Maximum Ratings

Continuous Supply Voltage	16.5V
Pulsed Supply Voltage (less than 100ms)	18V
Input Voltage (any input)	-0.5 to +18V
Storage Temperature	-65°C to +150°C
Lead Temperature (1/16 inch from case 10 sec max.)	300°C

Recommended Operating Conditions

(Normal operating range is 12 to 15 volts ±1 volt)

Parameter	Min.	Typ.	Max.	Unit
Supply Voltage	11		16	V
Operating Free-Air Temperature, T_A	-30		85	°C

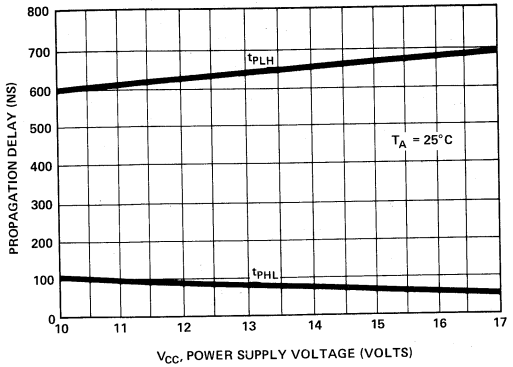
Electrical Characteristics

Over Recommended Operating Conditions Unless Otherwise Noted.
(L and J package temperature range is -30 to +85°C)

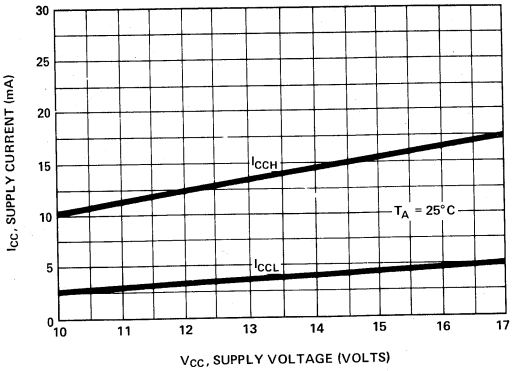
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Output High Voltage	V_{OH}	I_{OH} = -30μA, V_{IL} = 4V, V_{CC} = 11V	8.5			V
		I_{OH} = -30μA, V_{IL} = 6.5V, V_{CC} = 16V	14.5			V
Output Low Voltage	V_{OL}	I_{OL} = 12mA, V_{IL} = 6.0V, V_{CC} = 11V			1.5	V
		I_{OL} = 15mA, V_{IH} = 8.5V, V_{CC} = 14V			1.5	V
Reference Voltage	V_{REF}	I_{REF} = 0μA, V_{CC} = 12V	4.0		6.0	V
		I_{REF} = 0μA, V_{CC} = 15V	6.5		8.5	V
Input High Current	I_{IH}	V_{IH} = 16V, V_{CC} = 16V			10	μA
Input Low Current	I_{IL}	V_{IL} = 0.4V, V_{CC} = 11V			-0.4	mA
		V_{IL} = 1.5V, V_{CC} = 16V			-1.0	mA
Output Leakage Current	I_{CEX}	V_{CEX} = 16, V_{CC} = 16V			25	μA
Output Short Circuit Current (High state only)	I_{SC}	V_{CC} = 11V	-3.9		-10	mA
		V_{CC} = 16V	-6.5		-16	mA
Supply Current	I_{CCL}	V_{CC} = 16V (All Inputs Grounded)			12	mA
Supply Current	I_{CCH}	V_{CC} = 16V (Inverting Inputs Tied to V_{REF})			25	mA
Common Mode Voltage Range			1.5		V_{CC} -1.5	V
Differential Voltage Range			±12			V
Switching Characteristics	t_{PHL}	T_A = 25°C, R_L = 1.5K, C_L = 100pf		80		nsec
	t_{PLH}	T_A = 25°C, R_L = 1.5K, C_L = 100pf		650		nsec

Typical Performance Curves

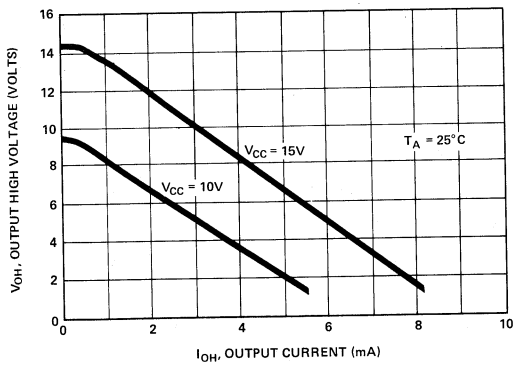
PROPAGATION DELAY TIME VS. POWER SUPPLY VOLTAGE



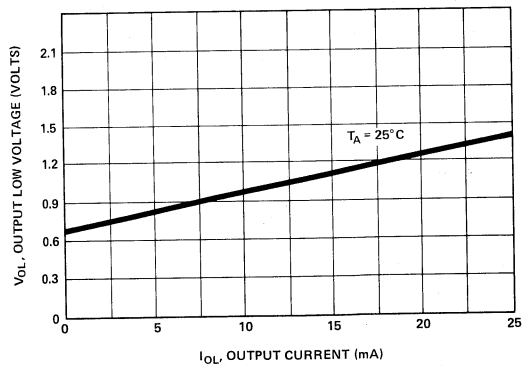
SUPPLY CURRENT VS. SUPPLY VOLTAGE



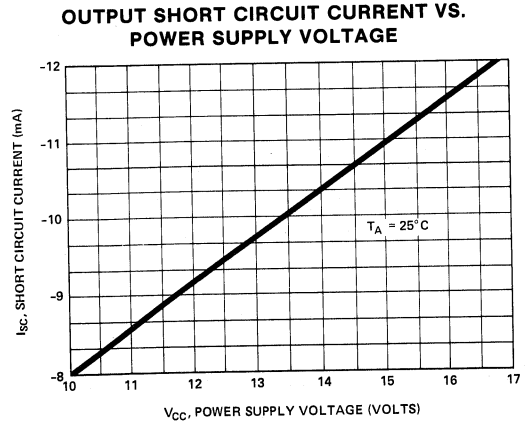
OUTPUT HIGH VOLTAGE VS. OUTPUT CURRENT



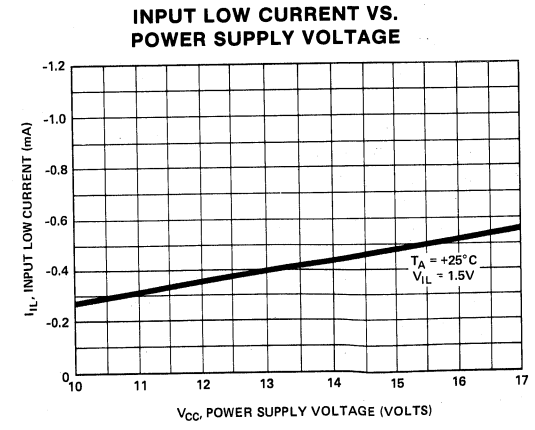
OUTPUT LOW VOLTAGE VS. OUTPUT CURRENT



OUTPUT SHORT CIRCUIT CURRENT VS. POWER SUPPLY VOLTAGE

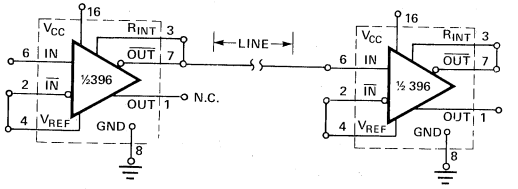


INPUT LOW CURRENT VS. POWER SUPPLY VOLTAGE

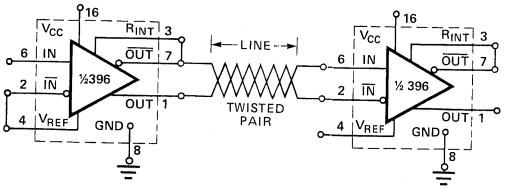


14

CONNECTION DIAGRAMS



Single Ended



Differential

Hysteresis Modes of the 396

The 396 has very flexible hysteresis capability, enabling the designer to adjust the switching thresholds (and thus the noise immunity) of the device to suit his needs. The hysteresis thresholds (V_{IL}, V_{IH}) and widths (V_{HW}) for various feedback resistor values of the test circuit shown in Figure 1 are plotted in Figure 2. The power supply is set at 15V, so that with the inverting input tied to the internal reference voltage of the circuit (approximately 1/2 V_{CC}), the high level and low level switching points of the device are centered about the 7.5 volt level.

Note that both switching points change symmetrically about that reference level until the feedback resistor is decreased below 5.5K ohm, giving a very wide range of widths. The variation of hysteresis width with changes in the power supply voltage is quite linear over the operating range as shown in Figure 3; the internal 7.0K resistor is used in that test for the hysteresis feedback.

The hysteresis center point level (V_L) can be changed by varying the reference voltage level as shown in Figure 4, giving complete control over the setting of the hysteresis levels. The only limitation is that the levels must remain within the common-mode range (CMR) of the device (1.5V above ground to 1.5V less than V_{CC}).

The hysteresis widths for the test circuit shown in Figure 4 are plotted in Figure 4A.

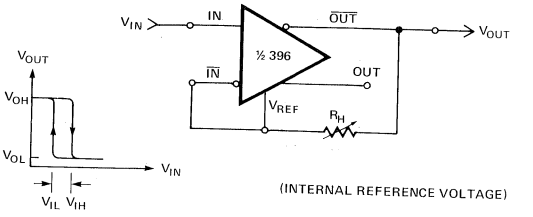


Figure 1. Variable Hysteresis Width Circuit

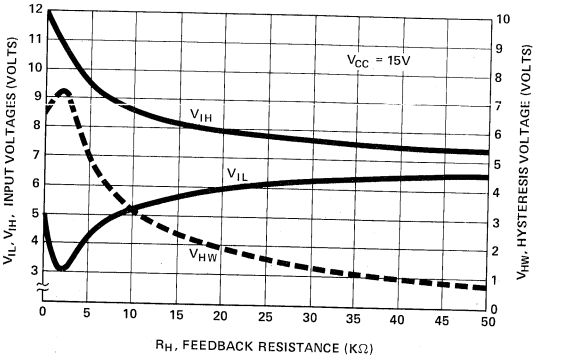


Figure 2. Typical Hysteresis Voltage (V_{IL}, V_{IH}) vs. Feedback Resistance (R_H)

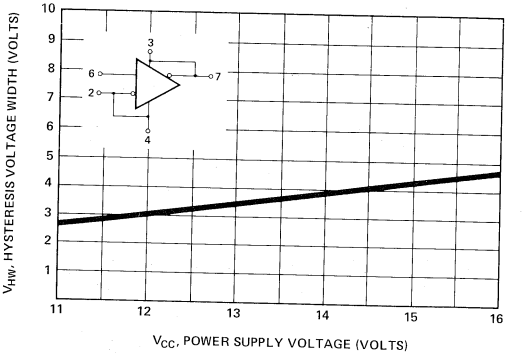


Figure 3. Hysteresis Width vs. Power Supply Voltage (Using Internal 7.0kΩ Resistor)

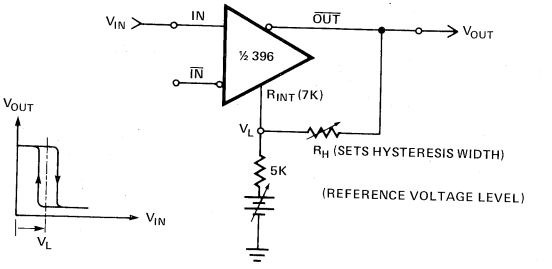


Figure 4. Hysteresis Level Variable

Applications Information

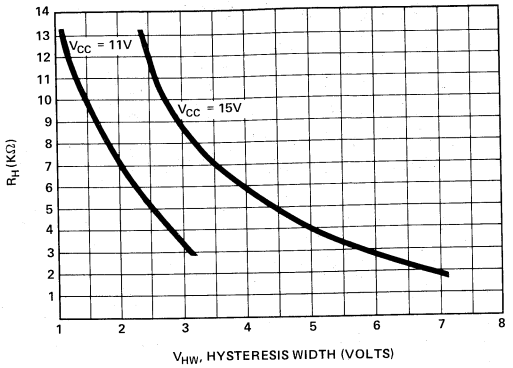
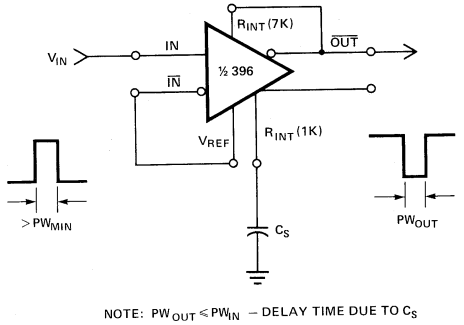


Figure 4A. Feedback Resistances vs. Hysteresis Widths

396 Slow-Down Receiver

The 396 can be used as a single-ended slow-down receiver as shown in Figure 5. By connecting a capacitor to the internal 1.0K resistor, the device can be made insensitive to pulses with widths shorter than a predetermined value. The graph in Figure 6 shows the minimum input signal pulse width necessary to trigger the circuit versus capacitance.



NOTE: $PW_{OUT} \leq PW_{IN}$ – DELAY TIME DUE TO C_S

Figure 5. 396 as Single-Ended Slow-Down Receiver

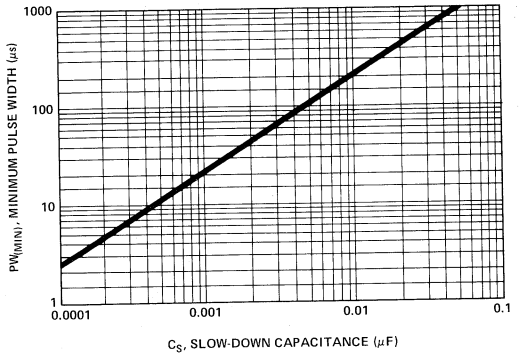


Figure 6. Minimum Pulse Width vs. Slow-Down Capacitance

396 as Line Driver/Receiver/Repeater

One of the best applications of the 396 is, of course, as a line driver/receiver/repeater, and because of its low frequency operation, (<500 kHz), many of the complicated effects associated with line driving and receiving can be ignored and calculations become straight-forward.

In Figure 7, one device is used as a twisted-pair line driver and another as a line receiver. The balanced series resistance, R_S, adds some series damping and limits the current through the line at high power supply levels while setting the voltage levels at the input of the receiver for maximum common-mode noise rejection (i.e., bias the input differential voltage in the middle of the common-mode range). R_O merely terminates the line in its characteristics impedance (≈ 100 ohm for 30 turns/ft, AWG24-2B; twisted pair) so that capacitive effects on the line may effectively be ignored.

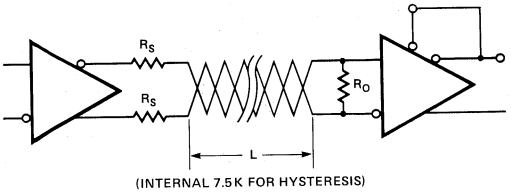


Figure 7. Using 396 as Differential Line Driver/Receiver

The worst-case limits of the series resistor can be calculated roughly by looking at the dc equivalent circuit shown in Figure 8. The three major constraints are:

1. $V_{diff} < V_{diff}$ min. ≈ 50mV
   (For safety margin use V_{diff} = 150mV)
2. $I_L < I_{SC}$ max.
3. Receiver input common-mode voltage centered in common-mode range (1.5V < CMR < V_{CC} — 1.5V)

For V_{CC} = 15V, these constraints require R_S to be about 5.0K.

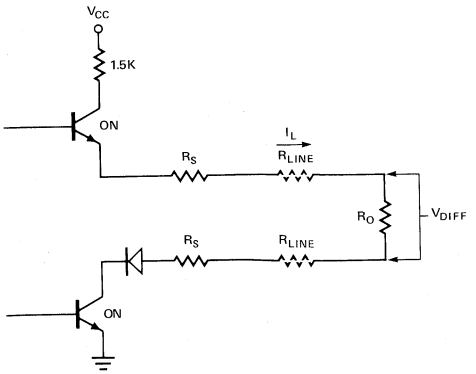


Figure 8. DC Equivalent Circuit

14

Applications Information

If necessary, hysteresis can be added to the receiver to improve switching characteristics, and for upgrading the signal along extremely long lines, the 396 can be used in a repeater configuration as shown in Figure 9.

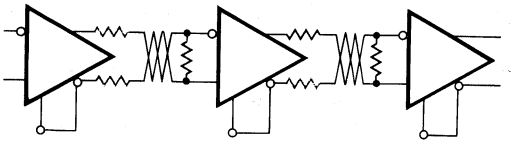


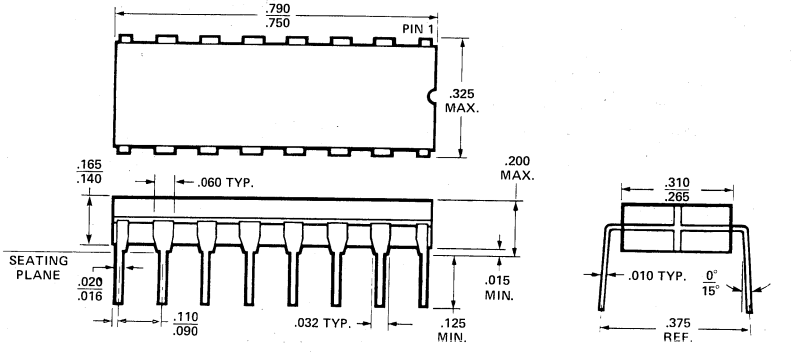
Figure 9. Using 396 as Line Repeaters

Ordering Information

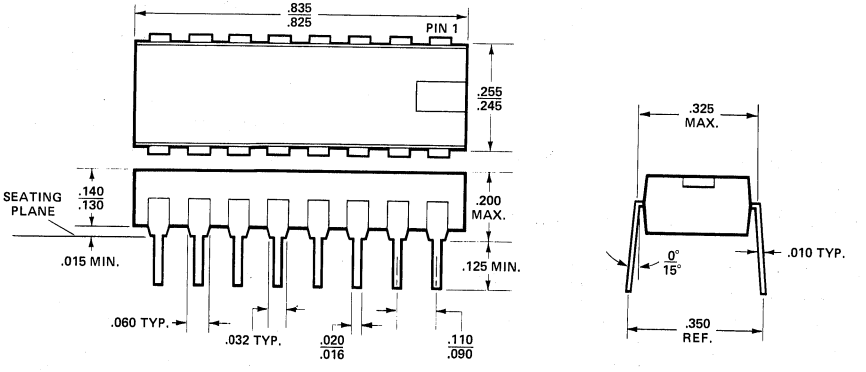
Order Part Numbers:

- L Package 16-Pin Ceramic DIP ($-30°C \geq T_A \leq 85°C$) 396AL/CL
- J Package 16-Pin Plastic DIP ($-30°C \geq T_A \leq 85°C$) 396AJ/CJ

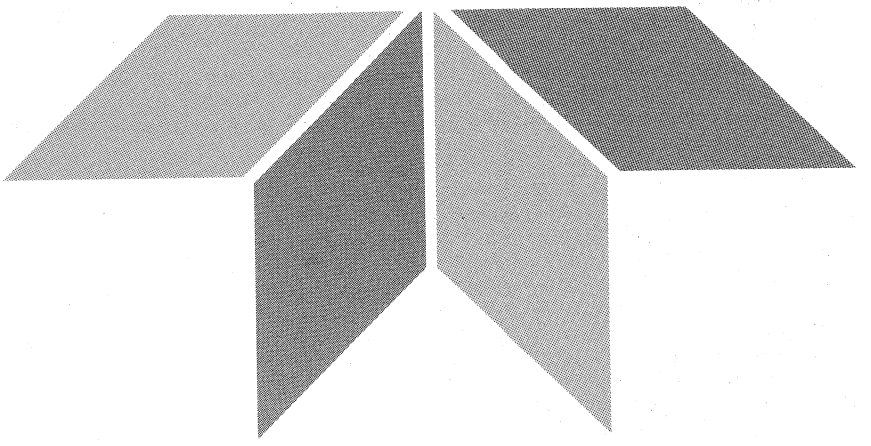
Physical Dimensions



16-PIN CERAMIC DIP



16-LEAD PLASTIC DIP



SECTION 15

Application Notes

Section 15
Application Notes 15-1

Application Note 1 Using High Noise Immunity Logic 15-3
Application Note 2 Design Techniques with HiNIL Schmitt Trigger 367 Quad 15-11
Application Note 3 Designing Programmable Controllers with HiNIL 15-15
Application Note 4 HiNIL 375 Universal Shift Register 15-19
Application Note 5 High Noise Immunity Logic — Powerful, Versatile and Growing 15-29
Application Note 6 The HiNIL 347 Dual Retriggerable One-Shot Theory and Applications 15-35
Application Note 7 Using Bipolar Logic to Improve Performance in CMOS and Microprocessor Systems 15-41
Application Note 8 Interfacing the 8700 A/D with the 8080 μP System 15-45
Application Note 9 Applications of the 8700 Series A/D Converters 15-51
Application Note 10 Applications of the 9400 V/F, F/V Converters 15-67
Application Note 11 7106/7107 Digital Meter Applications 15-77
Application Note 12 A Single IC Digital Thermocouple Thermometer Using the 7106 15-85
Application Note 16 TSC7135 Microprocessor Interface 15-87
Application Note 17 Simplify A/D Converter Interface w/Software 15-91
Application Note 18 TSC7211AM/TSC7212AM Display Driver Microprocessor Interface 15-95
Application Note 19 BCD A/D Converter Interface to Dot Matrix LEDs 15-99
Application Note 20 Two Digit Serial Input LED Display Driver Using TSC9404 15-101
Application Brief 1 Combining HiNIL and CMOS — an Optimum Design Technique 15-103
Application Brief 2 Protecting Logic Inputs 15-107
Application Brief 3 The 355 Timer Solves Noise Problems 15-109
Application Brief 4 Keeping the Bugs Out of Microprocessor Systems with High Noise Immunity Logic 15-111
Application Brief 5 HiNIL Interface Summary 15-113
Application Brief 6 Typical Applications for Bipolar Interface Logic 15-115

Application Note 1 Using High Noise Immunity Logic

HiNIL, the High Noise Immunity Logic family developed by Teledyne Semiconductor, is a remarkably simple solution to the problems created by electrical noise and system interface requirements in electronics equipment. HiNIL is particularly effective in control applications, where the ultra-high speed of computer logic is generally not required and indeed often compounds these problems. HiNIL was developed to make logic systems virtually immune to voltage transients and other sources of electrical noise and to operate at higher, more convenient voltage levels.

The HiNIL family has been enlarged to provide numerous logic, driver and interface devices with a choice of operating voltages, operating temperature ranges and package styles. Originally, the family was specified to operate at V_{CC} = 12V. Now, each device is also available with 15V operation, thus providing logic that will operate at the supply levels most commonly used for non-logic functions in instrumentation and control equipment. Newer devices are specified over a supply range from 10V to 16V, allowing easy interfacing with CMOS at its most popular operating level.

A noise immunity about 10 times better than conventional logic (such as TTL) is provided by HiNIL—even under worst-case operating conditions. Also noteworthy is the V_{CC} tolerance of ±1V at both 12V and 15V operation. In many cases, this allows the use of filtered but unregulated voltage fed directly to the HiNIL logic from the transformer rectifier of the system power supply. (For example, see the digital clock design in the 371 data pages.)

Worst-case operating conditions and guaranteed performance of HiNIL are given in the family and device specifications tables. These notes explain the design philosophy behind the specifications and provide information on how to design HiNIL equipment destined for use in electrically noisy environments, for instance, near machine tools and metal or plastics welding equipment. Typical equipment designs are given in the device data pages.

Noise Immunity of TTL

Although TTL and DTL are solidly entrenched in industrial and other control applications, these 5-volt logic families have good noise immunity only in computers and similar systems that are relatively quiet electrically.

TTL's 400 millivolts of noise immunity is simply not enough for many applications. For want of a better solution in the past, designers have relied on jury-rigged methods of improving noise immunity. That is, instead of having high noise immunity inherent in the logic circuits, the circuits have been protected from noise by extensive shielding, filter capacitors on the supply lines of each PC board, spot regulators on each board, heavily regulated and expensive power supplies, and other techniques in that vein.

Designers have come to think of these techniques as mandatory when monolithic logic is used, when actually they are not. As shown in Figure 1A, the basic problem is the narrow spread between the output voltage levels and the input logic thresholds of TTL.

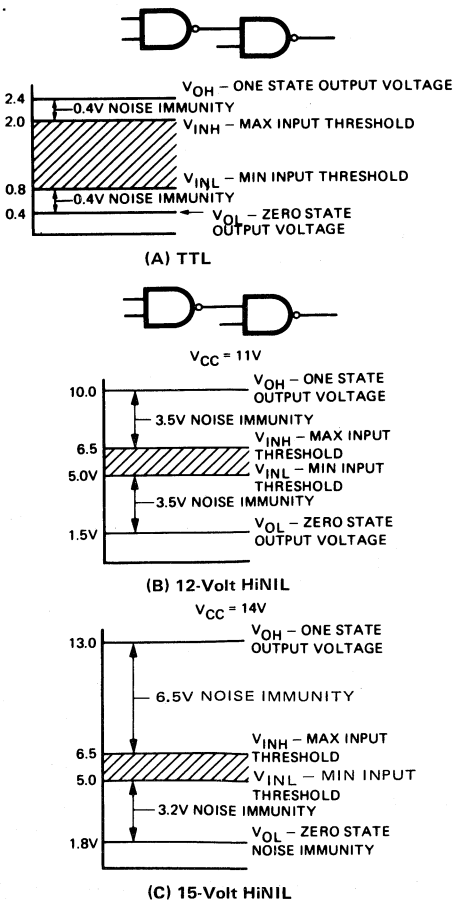


Fig. 1. Comparison of TTL noise immunity (A) with the noise immunities of HiNIL 12-volt and 15-volt devices (B and C).

15

HiNIL Noise Immunity

The solution employed in High Noise Immunity Logic is to trade off some speed and power against noise immunity by increasing the voltage levels. This is quite a favorable tradeoff in most applications outside the computer field, since high speed is not usually required, the power is relatively inexpensive once the need for tight regulation is eliminated, and the voltage levels are generally more compatible with those of other elements in the system.

Input thresholds are raised by a 5.8V zener diode on the chip (as in the NAND gate shown in Figure 2). The results, indicated in Figure 1B and 1C, are guaranteed worst-case noise immunities of 3.5V at V_{CC} = 12V ±1V and 3.2V at V_{CC} = 15V ±1V. In fact, these immunities can be guaranteed across a temperature range of -55° C to +125° C.

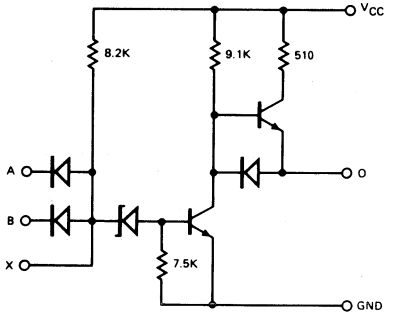


Fig. 2. Typical HiNIL logic circuit, the 321 NAND gate, showing location of zener diode that raises the threshold voltage.

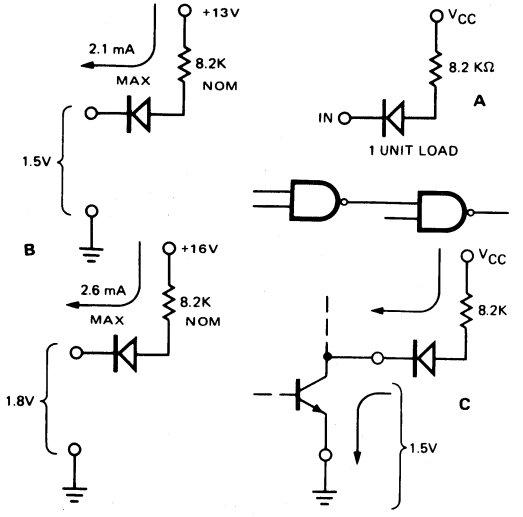


Fig. 3. Unit loads presented by the standard HiNIL input. The guaranteed maximum current flows and voltage drop across the output in the "0" state are shown.

Loading Rules

A HiNIL unit load is defined in Figure 3, which shows the family's standard input and an output transistor. A current flows down the 8.2 kilohm resistor when the gate driving the input is at logical "0". The output stage of the driving gate must sink this current.

Logical "0" or low voltage is equal to or less than 1.5V for 12V HiNIL devices or 1.8V for 15V devices. Therefore, the sink current is guaranteed to be less than 2.1 mA or 2.6 mA, respectively (see Family Characteristics table).

As the current passes through the driving gate's output transistor, it causes a voltage drop across the transistor. The larger this drop, the lower the noise immunity will be. As Figure 1 indicates, a drop larger than 1.5V or 1.8V would narrow the respective noise immunity margins.

Teledyne Semiconductor guarantees the above drops as V_{OL}, a general family spec for the maximum drop at the fanout specified for each device in UL. That is, if the device unit loading is specified as 5 UL at V_{OL}, that device will sink the currents from five inputs under worst-case conditions, without greater voltage drop in any output.

"1" State Loading

Input leakage currents in the high or logical "1" state must also be taken into account. Each input unit load might have as much as 10 microamperes leakage (I_{INH} max) flowing into it, which the driving output must source through its pullup resistor. Active pullup outputs can easily supply this leakage current with very little voltage drop across the output, so let's consider what happens in a passive pullup output.

In Figure 4, a passive pullup output is shown driving a single gate and sourcing the 10 μA maximum leakage. A voltage drop of 91 mV occurs across the 9.1K resistor. At the lowest specified V_{CC} of 11V for a 12V device, the minimum output voltage in the high state could be $V_{CC} - 0.091 = 10.909V$. Every input driven decreases this value, which is the output high voltage, or V_{OH}.

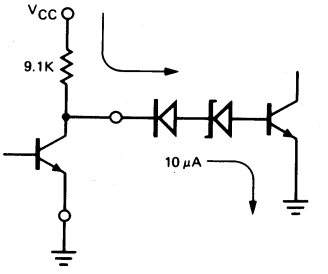


Fig. 4.

HiNIL loading rules have been worked out carefully so that V_{OH} can be guaranteed to provide at least the specified "1" state noise margin while an output is working at maximum fanout at the worst-case voltage-temperature relationship.

Passive Pullup Loading

One can ignore the current through the internal 9.1K resistor of a passive pullup HiNIL device when calculating loading of a collector OR'd assembly of these devices. The internal current flow is allowed for in the specs.

For simplicity, each external device connected to the data line can be considered one unit load. Thus, gate C in Figure 5 is driving four unit loads in either configuration. If three 324 NAND gates were collector OR'd, they could drive three inputs, if five were OR'd they could drive one input and so forth.

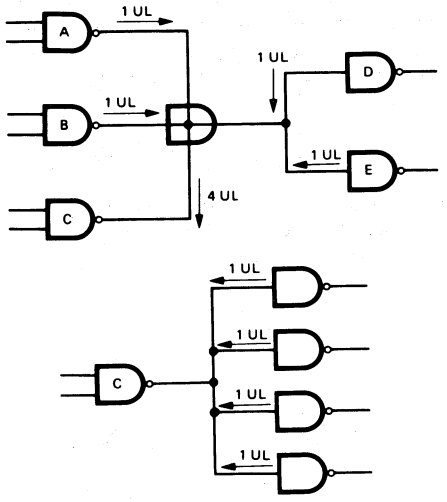


Fig. 5. Either connection presents four unit loads to gate C when that gate is on.

Each output is actually capable of sinking the input currents from eight—not five—unit loads when it is in the low state. But then in the high state, each might have to supply 8 UL of leakage current, or a total of 80 μA.

Assume the worst-case production tolerance for a 9.1K resistor plus a change in value in the same direction at worst-case temperature; the pullup resistor might actually represent a 14.2K resistance. Thus, an 80 μA current could produce a 1.13V drop across the resistor. If V_{CC} is also worst-case at 11V and I_{CEX} at maximum, the high output voltage (V_{OH}, see Figure 1) might drop below the 10.0V guarantee.

Hence, the spec that says the 324 gate can drive 5 UL is a conservative one for guaranteed performance. Obviously, in applications where some noise immunity can be traded off, or where temperatures are mild, a loading of 8 UL could be used with safety.

Still, the designer can have his cake and eat it too. He can get a fanout of at least 7 UL without dropping V_{OH} to below 10.0V. The trick is to use a 10K supplementary pullup resistor connected from the data line to V_{CC} in parallel with the pullup resistor on the chip. The additional current flow reduces the "0" state fanout from 8 to 7 UL.

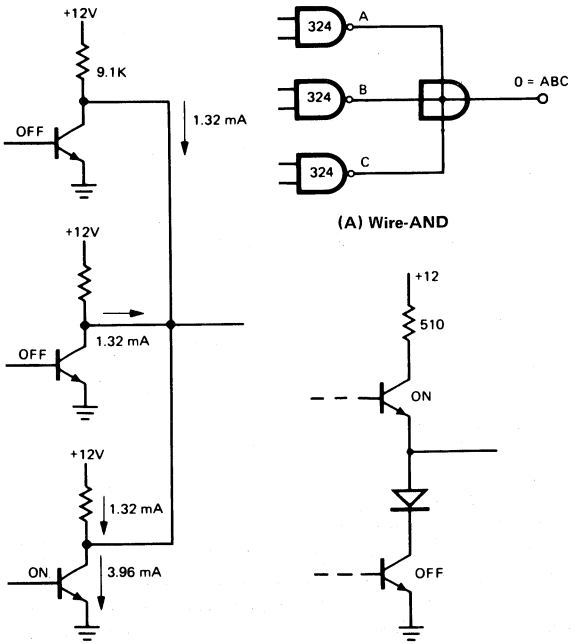
However, the parallel resistance also decreases the pullup resistance in the "1" state. The equivalent resistance of 14.2 and 10 kilohm resistors in parallel is only 5.85K. Across this, a worst-case 70 μA leakage only causes a 410 mV drop and leaves V_{OH} at a comfortable minimum of 10.59 volts for a 12V device actually operating at 11V V_{CC}. Likewise, the 15V versions of the circuits stay well within limits.

Actually, an external resistor may not be needed at all. If two passive pullup outputs are to operate with their pullup resistors in parallel, a similar voltage drop limitation is obtained. Thus, seven unit loads are easily driven by two passive pullup devices with every conservative design, at V_{OL}.

The equation given in the section on open collector devices may be used by designers who wish to calculate the external resistor values for particular operating conditions, but 10 kilohms in parallel is usually satisfactory. The 15V branch of the HiNIL family gives a little less leeway in the "0" state for tradeoffs of fanout against noise immunity, but much greater flexibility in the "1" state noise immunity. Generally, maximum "1" state noise is more desirable than maximum "0" state noise immunity.

Collector OR'ing

One of HiNIL's advantages over 5-volt TTL is that collector OR'ing does not reduce HiNIL's noise immunity. Collector OR'ing or "wire OR'ing", is more precisely a method of AND'ing outputs. But a solder dot is used instead of an actual gate (Figure 6). The more times a designer uses the technique in a system, the more gates he usually saves.



(A) Wire-AND

(B) Passive Pullup

(C) Active Pullup

Fig. 6.

15

The major rule is that any turned-on collector OR'd device be able to sink all the load currents from all the off devices sharing the solder dot or output line, as well as all the loads presented by the driven inputs on the line.

Considering the AND'ed outputs first, assume gate C in Figure 6 is on and A and B are off (the connection is often used to transfer data to a bus line, so this condition is logically desirable).

If the collectors were not OR'd, current would not flow through the pullup resistors of the turned-off outputs. However, the connection gives the 9.1K pullup resistors in gates A and B an alternate path to ground—not through their own output transistors, but through the solder joint and the output transistor of gate C. Therefore, when C is on it must sink three current loads rather than one.

This explains why collector OR'ing can generally be done only with open collector or passive pullup devices such as the HiNIL 323 or 324 NAND gates. They can both use large resistors that will limit the current flow. The resistor of a passive pullup HiNIL output device, such as the 324, is on the chip and has the nominal 9.1K value shown in Figure 7. The 344 is the only active output device which is OR'able.

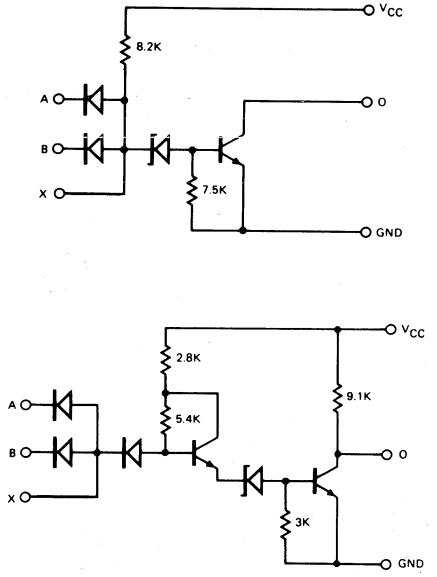


Fig. 7. HiNIL open collector and passive pullup NAND gates.

The resistor of an active pullup output is only 510 ohms. When the gate is sinking current, the flow through the resistor is limited because the upper transistor of the "totem pole" is off. But when the gate is sourcing current, the upper transistor is on. If several active pullup outputs were connected, excessively high currents would flow through the several pullup resistors through the one sinking transistor. These currents could destroy the one output.

Open-Collector OR'ing

The HiNIL family also includes a number of devices with open-collector outputs, including gates, lamp drivers, and so forth. Since these have uncommitted collectors, they are much more versatile in certain applications than the passive pullup or the active pullup types.

Figure 7 shows the schematic of the 323 gate. Note that a pullup resistance must be added externally between the collector pin and some positive voltage supply. However, the resistance doesn't have to be a resistor and the voltage doesn't have to be the HiNIL V_{CC} of 12V or 15V. Depending on their ratings, these outputs work with various kinds of loads and can also operate at various logic levels such as DTL, TTL and MOS. For a gate, the maximum pullup resistor value allowed by the specifications guarantees is:

$$R_{MAX} = \frac{V_{CC} - V_{OH}}{(n \times 25\,\mu A) + (f \times 10\,\mu A)}$$

when n is the number of OR'd open collector outputs and f the number of unit loads driven. The example in Figure 8 meets the spec with a maximum resistor size of 12.5K.

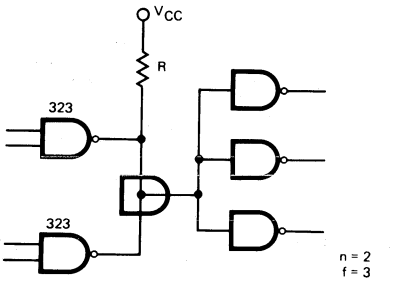


Fig. 8. Calculation of maximum pullup resistor value.

The minimum value is calculated with the following equation, using the upper value of V_{CC} and the sink current given for the device:

$$R_{MIN} = \frac{V_{CC} - V_{OL}}{I_{sink(MAX)} - f\,(I_{INL})}$$

Equations (1) and (2) apply to both 12V and 15V devices. But continuing the example in Figure 8, we get a minimum resistor value of:

$$R_{MIN} = \frac{13.0V - 1.5V}{12.6\text{ mA} - 3\,(2.1\text{ mA})}$$

$$= 1825 \text{ ohms}$$

Within the more than 4:1 range of resistor values, the designer chooses the one best suited to his system's operating conditions. In general, the smaller the pullup resistor, the better the

$$R_{MAX} = \frac{11V - 10V}{2 \times 25\,\mu A + 3 \times 10\,\mu A}$$

$$= \frac{1}{80\,\mu A}$$

$$= 12.5K$$

"1" state noise immunity and the faster the circuit operation. The "1" noise immunity is enhanced by the smaller voltage drop across the resistor, as covered before.

The rise time of the output is governed by the RC time constant consisting mainly of the pullup resistor and line and load capacitance to be charged through. The only disadvantage of using a minimum value of R is that average power supply drain goes up slightly. In most systems, this is of little importance.

Second-Level Gating

Another technique that can be used quite successfully with High Noise Immunity Logic is that of second-level gating. This is nothing more than the process of using diodes and pullup resistors as gates without active devices to restore logic levels. While it is true that using diodes in this manner will deteriorate the logic levels, it is also true that this deterioration is only disastrous when working with 5 volt logic. The deterioration amounts to about 0.7 volts, the forward drop across the diode, and would exceed the 400 mV guaranteed noise immunity of DTL or TTL. But when working with HiNIL with its guaranteed worst case noise immunity of 3.5 volts, the deterioration is not enough to cause problems in most systems. The decision is up to the systems designer. If he feels that he can reduce his worst case noise immunity of 2.8 volts (still seven times greater than DTL or TTL), then second-level gating opens up all kinds of possibilities for him. The basic configuration is shown in Figure 9

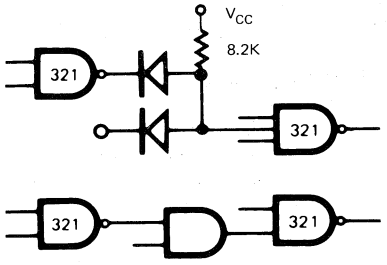


Fig. 9. The combination of two NAND gates and one AND gate can be made with two diodes, a resistor, and a pair of NAND gates using second level gating.

Here is a two-input AND gate made up of two diodes and a pullup resistor followed by a normal two-input NAND gate such as a 321. When the input to the AND gate is 1.5 volts or less (the guaranteed V_{OL} for the family), the output of the AND gate will be 1.5V +0.7V or 2.2 volts (or less). This is well below the threshold of the next gate and so the output is considered to be a zero. If the output of the driving gate is greater than 10.5 volts, the diode will be reversed biased and the output of the AND gate will be very close to +12 volts, certainly well above the threshold of the next gate. Thus, the diode-resistor combination functions very well as an AND gate. An example of this technique is shown in Figure 10.

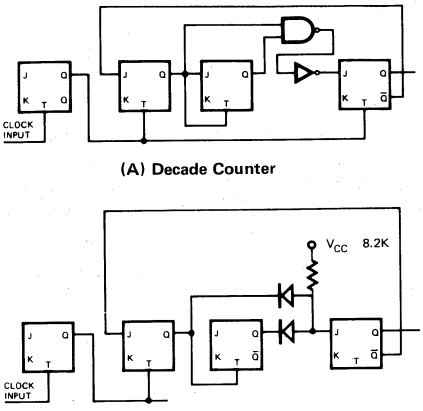


Fig. 10. Using second level gating can effectively reduce the number of I.C. gates in a system.

While it illustrates the construction of a decade counter, a device readily available as a single package in HiNIL, the application so well illustrates the technique of second-level gating that it bears examination. Figure 10a shows the construction of the decade counter using conventional techniques, i.e., four JK flip-flops and a pair of NAND gates. Examination of the diagram will reveal that one of the NAND gates is used merely as an inverter to change the first NAND to an AND. Whenever you see a NAND gate followed by another NAND gate to invert the first, you have a perfect spot for second-level gating. The same circuit using second-level gating is shown in Figure 10b. The saving is obvious. Two diodes and a resistor have replaced two NAND gates. This is a relatively simple application but its use throughout a system can yield amazing results in reduced package count. And there is no reason why it should be restricted to this relatively simple application.

Driver Pullups

Care must be used when working with powerful passive pullup or open-collector devices, particularly the 302 and 303 quad power NAND gates. Both are capable of sinking about 65 mA. The resistor sizes can be calculated with the above equations. Without making compromises in system noise immunity, a designer can achieve a fanout of about 20 with either the 302 open collector or 303 passive pullup drivers by using the above equations. The 5 UL nominal loading spec for these gates applies to a maximum resistor value as provided by the resistor on the 303 chip.

After the minimum and maximum resistor values for the desired operating conditions are calculated, the designer can judge whether on-chip passive pullup resistors are adequate or whether supplemental pullup should be used. If the devices are being OR'd, it is usually desirable to calculate the optimum fanout achievable with a parallel resistance combination of either on-chip resistors or on-chip plus external resistors. It is unlikely that the internal resistance values will be too low, but they may be too high for maximum fanout.

The 380, 381, 382 and 383 decoder/drivers all have open collector outputs designed to handle the loads encountered in their applications.

The 380, when driving lamps, may not require any pullup resistor. Each of its outputs can sink up to 30 mA. There are many lamps whose operating resistances are sufficient to limit the output sink current to 30 mA. Allowing for surges and tolerances, lamps rated at up to 24 mA maximum steady state current can generally be used without any other current limiting. In our own work, we have found 14V, 10 mA lamps give excellent brightness and economy when operated with the 380.

HiNIL Interfaces

There are very few system interfaces that cannot be handled simply with HiNIL devices of one type or another. The logic interface devices in the 360 series were made specifically to handle interfaces with TTL, DTL and RTL logic families straightforwardly, as shown on their data sheets, so there is no need to detail their operation here, although they are summarized in Figure 11.

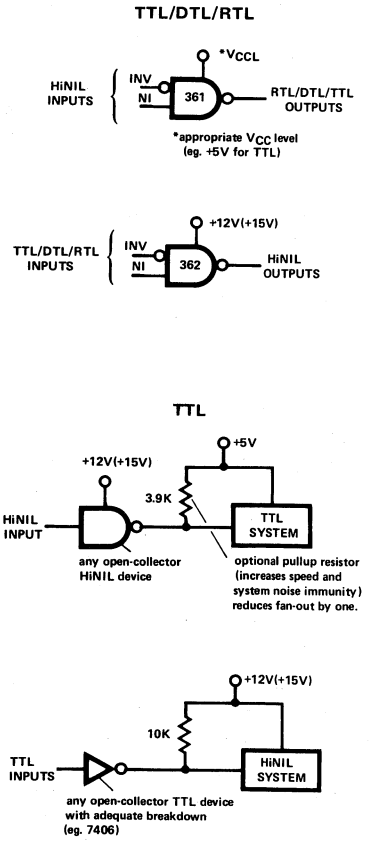


Fig. 11. HiNIL-to-TTL/DTL/RTL Interface Summary.

But it should also be noted that open-collector devices, including the simple gates, generally have ample output sink and drive currents to operate as output interfaces. The gates can easily operate a small lamp or relay, for instance, and they can share the same power supply. For larger loads the 301, 302 and 303 power gates can be used, and the new 390 series handles up to 250mA.

So the designer rarely need to worry about designing special circuitry for his system output interfaces with discrete components or hybrid ICs.

For output interfaces to other types of logic—for instance from a HiNIL control circuit in a noisy machine tool or motor application to TTL, DTL or MOS—one simply connects an open collector output through a pullup resistor to the desired high logic level for input to the other family. That is, to the TTL or DTL V_{CC} supply or to the MOS pullup supply (for low-threshhold MOS requiring input pullup to 12V, of course, the HiNIL and MOS can share the same 12V supply). The pullup resistors are calculated as before.

To get signals from another type of device into HiNIL logic is usually easy, too. In many cases, the other side of the input interface is a switch, relay, or operational amplifier comparator, operating at the HiNIL voltage levels. Since switching transients generally do not affect the logic performance of HiNIL, interfacing is merely a matter of making the connection in most cases.

Occasionally, low frequency, very heavy transients may have to be removed from the input line. This can be done with any number of inexpensive filtering or isolation type devices. The high-frequency transients are of little concern. Unlike high speed, 5-volt logic, HiNIL takes a pronounced, fairly long-term change in the input voltage level to switch because of the wide spread between its threshold voltages. So it ignores high frequency transients as a rule.

When the need arises to interface low voltage logic with HiNIL the easiest way is to plug a 5 Volt-to-HiNIL interface circuit into the assembly. Alternatively, one can use a homemade or off-the-shelf transistor switch. Any of literally thousands of cookbook designs intended to get from logic to small lamps or relays are easily adapted as interfaces.

Finally, it should be mentioned that HiNIL has interface applications where noise immunity is not a great concern. Suppose, for example, that a system contains a number of analog signal sources, a MOS commutator, and operational amplifiers or other analog instrumentation circuitry. How convenient it is to build the digital channel selection circuitry with a few HiNIL packages, such as a counter and a decoder, without having to provide special power supplies for the logic and a complex interface network.

Interfacing to Microprocessors and MOS

An MOS microprocessor system can be troubled by disastrous bugs unless it is protected against noise transients generated by switches, electromechanical peripherals and other nearby noise sources, such as lamps, and machinery. But filters and shielding, the traditional cures, are often difficult to add to a microprocessor because of size and cost constraints.

These problems can be avoided by substituting HiNIL interface devices (see table) for conventional I/O logic. HiNIL has a guaranteed DC noise immunity about 10 times that of TTL, for example (3.5 vs. 0.4V). Also, HiNIL blocks AC transients large enough to cause TTL malfunctions. Two additional advantages are superior output drive and, in low power systems, protection of CMOS memory and random logic inputs.

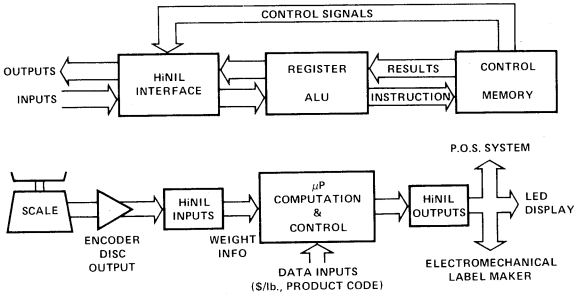


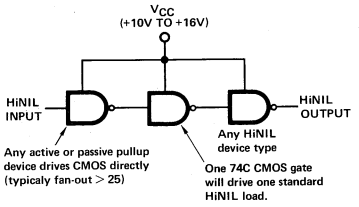
Fig. 12. Use of HiNIL interfaces in POS systems with electronic scale. Top diagram shows basic microprocessor configuration.

One manufacturer of microprocessor-controlled electronic scales decided to use the configuration in Figure 12 because he was concerned about the consequences of incorrect weights and prices. The probability of errors resulting from noise transients was high because the scale would be used in a supermarket POS system, where the environment includes refrigerators, fluorescent lamps, meat grinders and electromechanical label makers.

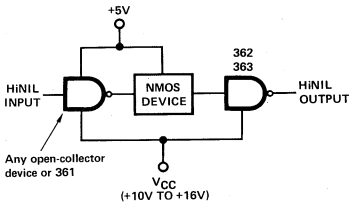
In the system, the microprocessor receives weight codes from an encoder disc in the scale and operates a cash register interface, LED display, and relays of a receipt printer or label maker. The system designers put HiNIL interface logic on the microprocessor board to handle the I/O functions, suppress noise transients picked up along the transmission lines, and drive the peripheral devices. HiNIL output interfaces can drive long lines, relays, displays and lamps without additional components since they sink up to 65 mA and source up to 12 mA. (The new 390 buffer series sinks up to 250 mA.)

The rules for using HiNIL with MOS or with CMOS operating at lower voltages are simple. The pullup resistor of an open collector HiNIL device is connected to the desired high logic level voltage (see Figure 13). HiNIL is also compatible with most analog devices.

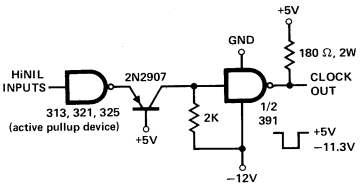
Complementary MOS



N-channel MOS



MOS Clock Driver



PMOS

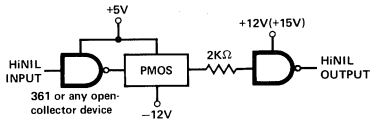


Fig. 13. Typical HiNIL/MOS and HiNIL/CMOS interfaces.

Examples of HiNIL Interface Devices

301 Dual 5-Input Power Gate 302 Quad Power NAND Gate (OC)	65mA relay or lamp driver
323 Quad NAND Gate (OC) 332 Hex Inverter (OC) 334 Strobed Hex Inverter (OC)	Input noise protection plus open-collector pullup to other logic levels
350 8-bit Multiplexer 351 Dual 4-Bit Multiplexer	Drive longer lines than TTL with 10X noise immunity (I_{OH} = 12mA)
361 Dual Input Interface 362 Dual Output Interface 363 Quad Output Interface	361 directly connects HiNIL to DTL/RTL/TTL, 362 and 363 connect DTL/RTL/TTL to HiNIL
367 Quad Schmitt Trigger 368 Quad Schmitt Trigger (OC)	Suppress 100V/1μs spikes, protect CMOS, decode switches, etc.
380 BCD to Decade Decoder 381 BCD to Decade Decoder (OC) 382 BCD to Decade Decoder 383 BCD to 7-Segment Decoder	Provide decode/drive for lamps, LEDS, gas discharge displays, etc.
390 Interface Buffer Series	250mA HiNIL driver series

15

Application Note 2
Design Techniques With Schmitt Trigger 367 Quad
By Robert MacIntyre

The Teledyne 367 is loosely classified as a Schmitt Trigger, and in fact, does everything a Schmitt does and much much more. A conventional Schmitt Trigger is an emitter-coupled binary which behaves much like a gate, but is really a two-stage amplifier with positive feedback.

Figure 1 shows the block diagram of a Schmitt. This diagram and most of the comments following apply to the 367 as well. The differences will be discussed later. The transfer characteristics of Figure 1 are described by the equation

$$\frac{E_{OUT}}{E_{IN}} = \frac{K}{1-KB}$$

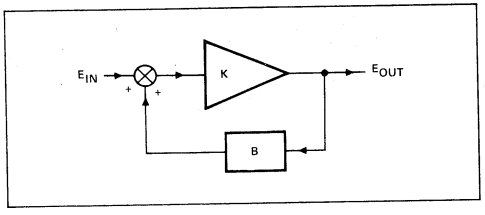
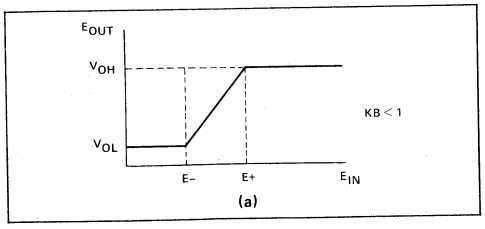


Fig. 1

In general, either K or B is linear only over a portion of the input voltage range, and the possible transfer curves are represented by the three versions shown in Figure 2. If the linear portion of the loop gain, KB, is less than one, the transfer curve is that of Figure 2a, with the output linear between the E– and E+ input levels (if B = 0, we have an ordinary non-inverting gate characteristic). As B increases so that KB approaches 1, the slope becomes steeper and steeper, and points E– and E+ move closer together. When KB = 1, the curve looks like Figure 2b, with the slope vertical and E– = E+. The extra gain of the positive feedback produces a "snap" effect, resulting in a squaring action which is very desirable in many applications. Unfortunately this characteristic also makes the device unstable at the threshold level.

When KB is increased beyond unity, the characteristic of 2c results, with a negative slope connecting the E– and E+ points. This is the most common Schmitt circuit.



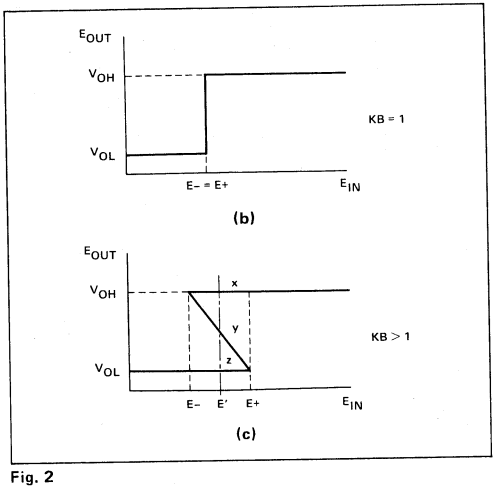


Fig. 2

The transfer curve of Figure 2c is said to have hysteresis. If the input voltage is at point E', between E– and E+, the output could theoretically be at point x, y or z. x and z are stable states – y is not. Hence the output will be at V_{OH} or V_{OL}, depending on its previous history. If the input has been below E– more recently than it has been at E+ then E_{OUT} will be V_{OL}. If the most recent excursion was above E+, the output will be at V_{OH}. Figure 3 will clarify this point.

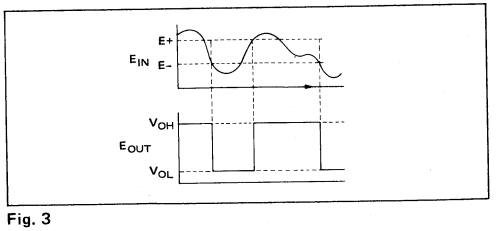


Fig. 3

The 367 has the input/output characteristics of Figure 2c and was designed to maximize the "dead zone" between E– and E+. It is composed of four trigger circuits connected as shown in Figure 4. Each of the four circuits has an input pin, a delay pin and an output pin. In addition, the pull-up input and the inhibit input are common to all four circuits.

The function of the inhibit pin is apparent from the logic diagrams. As long as the inhibit is high, all four outputs are held high. With the inhibit low, the output is the inverse of the data input. The delay input is provided so that a grounded capacitor can be connected to slow down the input. This pin can also be used as a direct input if desirable.

15

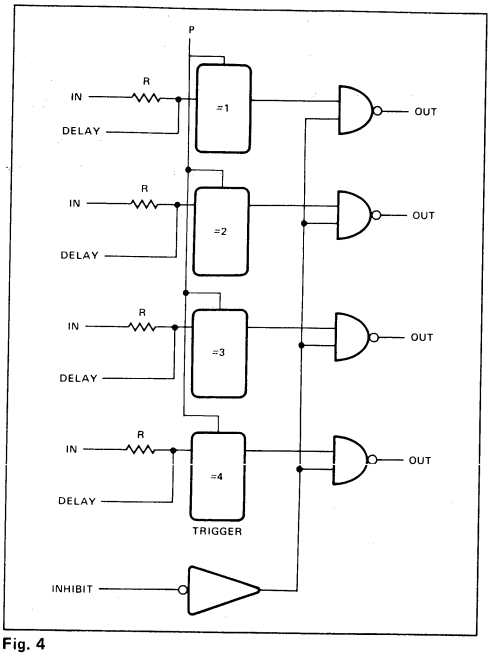


Fig. 4

In conventional Schmitt Trigger designs such as the 7413, an open input will appear to be a logic one. This is the major difference with the 367. If the input is opened, the device does not react – it stays in whichever state it was in before the input opened up. Putting this another way, external current must be supplied for the device to recognize a high and current must be extracted from the input for the device to recognize a low. If more conventional operation is desired, merely connecting the special pull-up pin to V_{CC} will cause the device to treat an open input like a high signal. These characteristics are described by the truth tables. Tables 1a and 1b.

TRUTH TABLES

Pin P Open

INPUTS		OUTPUT
A	INH	O
0	0	1
OPEN (was 0)	0	1
1	0	0
OPEN (was 1)	0	0
0	1	1
1	1	1
OPEN (was 0)	1	1
OPEN (was 1)	1	1

(a)

Pin P Connected to V_{CC}

INPUTS		OUTPUT
A	INH	O
0	0	1
1	0	0
0	1	1
1	1	1

(b)

TABLE 1

The second major feature of the 367 is its large hysteresis or dead zone – typically 4.5 volts. The DC noise immunity of a standard single-threshold device is the difference between the threshold and the high and low output levels. For TTL the guaranteed noise immunity is only 400 mV, but for HiNIL it is about nine times larger or 3.5V (hence the name High Noise Immunity Logic). There is, however, more to the noise immunity story. During the logic transition period, the output voltage of the driving device moves through the threshold V_T of the driven device. As the voltage approaches the threshold, the noise immunity decreases until finally, at the threshold itself, the noise immunity is zero. As can be seen from the diagram in Figure 5a, noise spikes occurring on the line during the transition can cause "extra" excursions through the threshold that show up as false output signals.

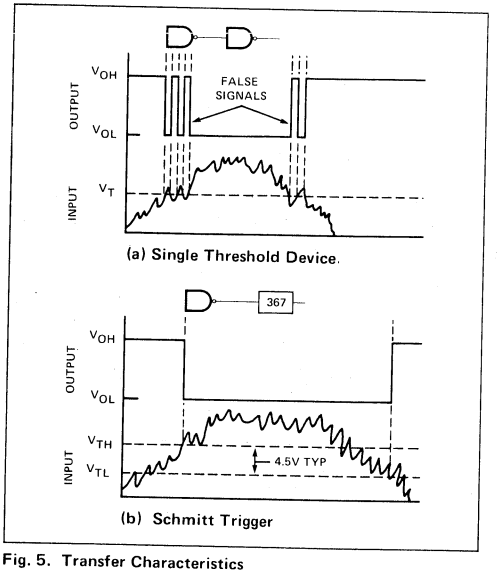


Fig. 5. Transfer Characteristics

Generally speaking, the 3.5V of noise immunity provided by HiNIL is more than enough to ensure trouble-free operation, even in very noisy environments. But there is one point in the typical system that is subjected to more than the normal amount of noise, and the use of the 367 at this point provides the user with a great deal of insurance in the way of additional noise immunity. That point is the system

input and the problem occurs because the input is frequently a long line that acts as a perfect antenna.

The 367 Quad Schmitt Trigger solves this problem with its system of dual thresholds. The Schmitt action is such that the device will not interpret an increasing input voltage as ONE until it RISES through the upper threshold, V_{TH}. As soon as the device switches, the critical voltage level changes to the lower threshold, V_{TL}. Now the input voltage has to FALL through V_{TL} before the 367 considers the input to be ZERO. Since the two thresholds are typically 4.5V apart (2.5V guaranteed), a noise spike EVEN DURING LOGIC TRANSITIONS would have to be greater than 4.5V in amplitude to cause a logic error. Thus, the 367 combats noise by removing the problem of spikes as logic devices go through the threshold.

Actually, the hysteresis provided by the schmitt action increases the noise immunity in a second, more subtle way. As can be seen in Figure 6, the thresholds are moved further from the output voltages, V_{OL} and V_{OH}, used for the noise immunity calculations. The normal HiNIL gate input has typically 4.6 volts of noise immunity in the ZERO state and 5.5 volts in the ONE state. Using the 367 extends the ZERO state noise immunity to 7.6 volts and the ONE state immunity to 7.3 volts on DC basis.

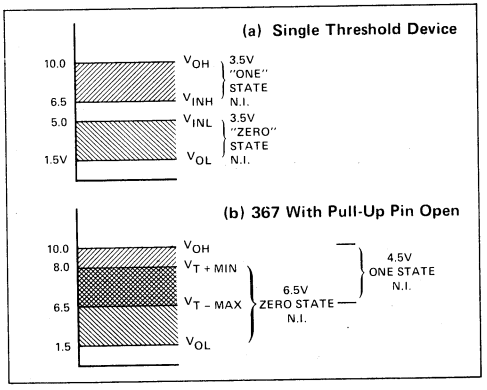


Fig. 6

The inhibit input can actually increase system noise immunity in a third way if it is used to enable the 367 only at times of low overall system noise. A prime example of a low-noise time is when the 120VAC line is crossing zero.

The unique truth table that results if the pull-up is left open (see Table 1a) is the fourth way the 367 combats system noise. Suppose we had a 12 volt logic system which received some inputs from mechanical switches such as contactors, relays, limit switches or even manual toggle switches. If such switches did not bounce, we would have no problem connecting them directly to the input of gates or other logic elements. But they do bounce, so we have to devise some means of ignoring the bounce. The 367 was designed to take advantage of the fact that a double-throw contact does not bounce from throw to throw; the bounce merely results in momentary opens. Therefore, if the switch is connected to the 367 as shown in Figure 7, the bounce and resultant noise will be locked out of the system. This may become the most common usage for the device.

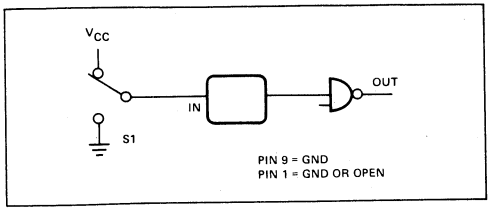


Fig. 7

The 367 has still another design feature which extends the usefulness of the unit — the slowdown capacitor connection point (delay pin). Ordinarily, merely slowing down the input of a gate with a capacitor is not the best way of achieving immunity to transients. This is because the slowed input is *more* susceptible to noise because the capacitor holds the input near the threshold voltage (where the immunity is low) for long periods of time. The large hysteresis of the 367 removes this problem so that slowdown capacitors can be used to make the device ignore short pulses. See Figure 8. This connection may also be used as a pulse delay circuit.

The topological design of the 367 gives the resistor between the input and delay pins special characteristics. The input can safely be driven 5 volts below ground or above V_{CC} for an unlimited length of time. Short spikes will be shrugged off even at very high amplitudes (100V) if they are short enough (1 μsec). The resistor limits the current to accomplish this.

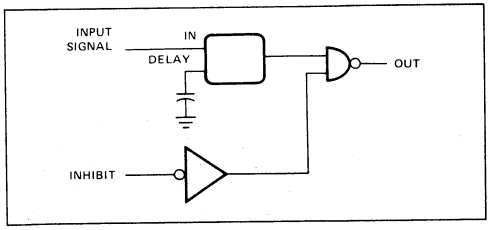


Fig. 8

The availability of the slowdown point and other features of the design open up and/or simplify other applications using the 367. Figures 9 through 14 show some of these applications.

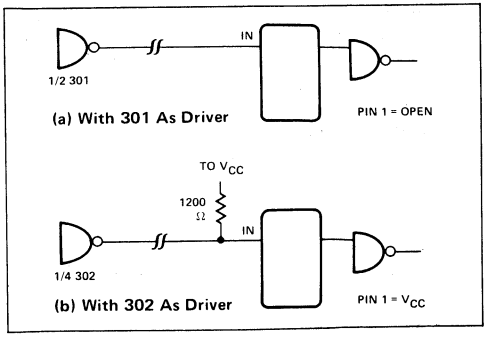
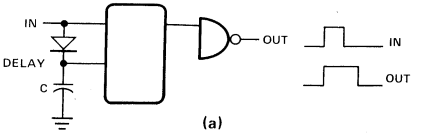
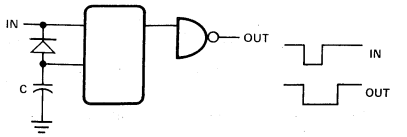


Fig. 9. Line Receivers



(a)



(b)

Fig. 10. Pulse Stretchers

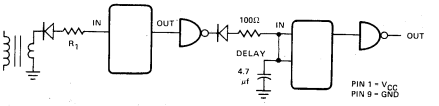


Fig. 11. AC Detector

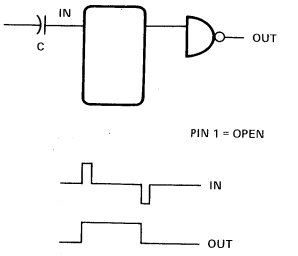


Fig. 12. AC Coupled Latch

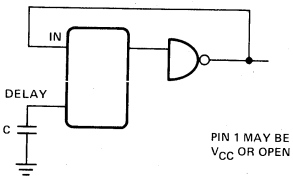


Fig. 13. Free-Running Oscillator

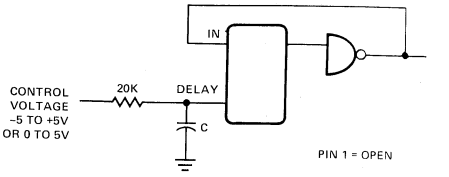


Fig. 14. Voltage Controlled Oscillator

The application shown in Figure 9 will probably be seen nearly as often as the switch interface usage discussed previously. It is an ideal method of interconnection between two-widely-separated portions of a system. For noisier environments, this hookup can be used with slow-down capacitors, as mentioned earlier. In extremely noisy applications, the inhibit input may be used to gate out virtually all unwanted signals.

The circuits of Figure 10 are straightforward. The diode is connected to speed up charge or discharge of the capacitor, depending on the polarity of the input pulse. This connection may be used with or without the internal pull-ups connected to V_{CC}. In this and some other applications, it may be desirable to use external resistors – either in place of the pull-ups or instead of the series limiting resistor between input and delay pins.

Figures 11 and 12 will probably not see much use, but are included to demonstrate the 367's flexibility and versatility. In the AC detector, the output is high if a large enough 60 HZ signal is present at the input. R_1 is selected to set the AC level which will be detected. Direct or capacitor coupling may replace the transformer input if the DC ground is connected to AC common.

The oscillator circuits of Figures 13 and 14 will be very useful. The free-running version in Figure 13 may be gated on and off with the inhibit input. A 1K pot could be connected between output and input to provide a frequency trim. The oscillation frequency is approximately

$$f_{osc} \frac{250 \times 10^6}{C} \text{ at } V_{CC} = 12V \text{ and } T = 25°C$$

(f is in H_Z and C is in farads)

The unique features of the 367 make it an extremely versatile logic element that will become the universal input to every HiNIL logic system.

NOTE:
HiNIL 368 Quad Schmitt Trigger now available. Features open collector outputs (directly interfaces to TTL).

Application Note 3
Designing Programmable Controllers With HiNIL
By David Guzeman

One of the most common problems faced by the designer of industrial electronics equipment is that of the programmable controller. This system is used in one form or another for everything from controlling complex manufacturing processes to running long-term laboratory tests. Generally they are built as functions of time, and usually include some provisions for feedback at several points in the cycle. These functions are sometimes performed by minicomputers. The minicomputer is a vastly more complex (and versatile) tool, but it suffers from high initial expense, the need for special I/O circuits, and extensive training in the programming and operation of the machine.

Programmable controllers, on the other hand, are much smaller, inexpensive, and require no training. Many times these are hard-wired machines built for specific jobs. Sometimes they possess the ability to be re-programmed in terms of time or load functions. This article will describe a design approach that encompasses both hard-wired and re-programmable machines.

Use has been made throughout of Teledyne's High Noise Immunity Logic (HiNIL). This logic family has the unique property of operating from a single supply voltage of +12 V (+15 V optional) and offering the user a guaranteed 3.5 V worst case noise-immunity across the temperature range. Its use is ideal here, since many of the gate inputs will be brought out to front-panel connections that act as excellent antennas for picking up noise. HiNIL effectively eliminates this problem. Similarly the use of HiNIL removes the need for filtering capacitors, "slow-down" networks, and allows the use of an inexpensive power supply (all HiNIL specs including the 3.5 V guaranteed worst-case noise immunity are guaranteed for V_{CC} ± 1.0 V). Finally, the controller presented here will make extensive use of a technique called second-level gating that replaces IC's with discrete diodes. It does this by sacrificing 0.7 V of noise immunity, not much of a loss to HiNIL but far in excess of TTL's 0.4 V noise immunity.

The controller presented here utilizes the properties of the HiNIL 380 BCD to Decade Decoder. This device is designed to accept BCD code on its inputs and to select one-of-ten active-low outputs. Each of the outputs are open-collector transistors which makes it possible to collector-AND the outputs by tying them to V_{CC} through a common resistor.

TIMING FUNCTION

	Valve A	Valve B	Valve C	Pump
0:00	OFF	OFF	OFF	OFF
0:15	ON	OFF	ON	OFF
0:30	ON	OFF	ON	OFF
0:45	ON	OFF	ON	OFF
1:00	OFF	OFF	ON	OFF
1:15	OFF	OFF	ON	ON
.				
.				
.				
3:15	OFF	OFF	ON	OFF
3:30	OFF	ON	OFF	OFF
.				
.				
.				
9:30	ON	ON	ON	ON
9:45	ON	ON	ON	ON
0:00	OFF	OFF	OFF	OFF

REPEAT

Fig. 1. Typical controller cycle that can be implemented with the controller.

The 380 is designed to be used with the 371 decade counter. In Figure 2 is a simple controller that delivers a one minute output pulse to a load seven minutes after the beginning of a ten minute cycle. The discrete 9.1 kΩ resistor acts as a pull-up for the open-collector transistor that is the output for count number 7. Since all of the outputs are open-collector transistors, they could be ANDed together by simply tying several of the outputs to the same pull-up resistor. This has been done in Figure 3, where it is used to generate output pulse trains of odd sequences.

There is no reason why more than one load cannot be controlled by the same 380. This requires only that the various outputs be isolated from each other by the addition of discrete diodes. Theoretically this will decrease the noise immunity of the system by 0.7 V.

The decrease in noise immunity can be seen from the basic equation for zero state noise-immunity. $N.I._{(o)} = V_{INL} - V_{OL}$. For HiNIL these values are V_{INL} = 5.0 V and V_{OL} = 1.5 V, hence $N.I._{(o)}$ = 3.5 V. Adding a diode to the output as shown in Figure 4, adds 0.7 V to the V_{OL} of the 380, and the equation becomes

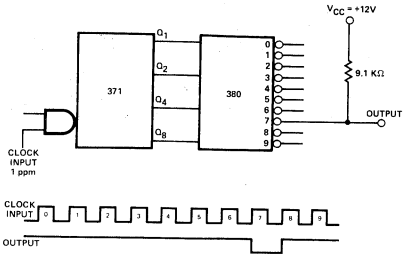


Fig. 2. Simple Controller causes output to go low for one minute every ten.

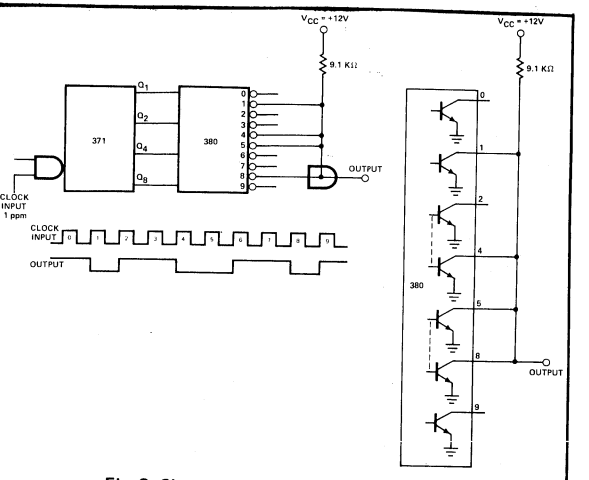


Fig. 3. Since any of the output transistors can pull the output line low, this circuit delivers low output pulses on clock pulses 1, 4, 5 and 8.

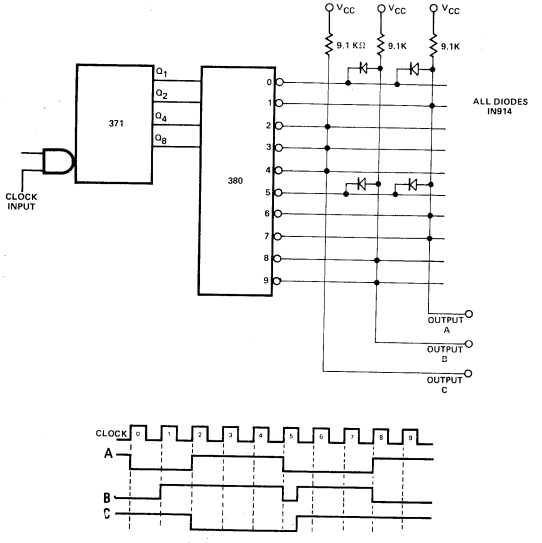


Fig. 4. More than one load can be controlled by a decoder if diodes are used to isolate the output lines.

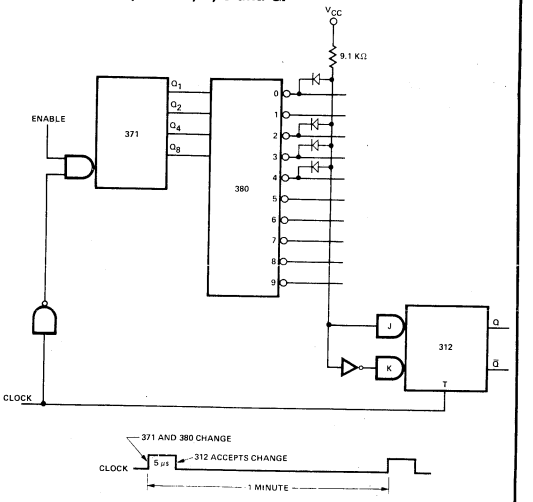


Fig. 5. Adding a JK flip-flop to the system eliminates false pulses.

$$N.I._{(0)} = V_{INL} - (V_{OL} + 0.7\ V) =$$
$$5.0\ V - (1.5\ V + 0.7\ V) = 2.8\ V$$

Actually, the value of V_{OL} = 1.5 V was picked for the family because many of the devices had active outputs. The HiNIL active output configuration gives a typical V_{OL} = 1.2 V under full fan-out conditions. But the 380 has open-collector outputs and a typical V_{OL} of 0.4 V with a fan-out of 20! This means that using discrete diodes with open collector devices maintains the system noise immunity at 3.5 V worst case.

A problem, easily eliminated, is associated with the circuits of Figures 3 and 4. This is because it is possible for two or more outputs of the 380 to go low immediately after its inputs change states. This is due to race conditions within the 380 and will have died out within a few nanoseconds. If the 380 is to be followed by latching type logic, it is possible for these glitches to result in false output signals.

In any event, the cure, illustrated in Figure 5, is so easy it should be included for safety's sake. The particular flip-flop chosen, the 312 dual JK, happens to trigger on the falling edge of the clock. This provides an automatic two-phase operation since the 371 is delivered an inverted clock so that it triggers on the rising edge of the clock. That means the 371 and 380 change states immediately after the clock goes high, and after a few nonoseconds all false outputs will have died out, leaving only valid information on the inputs to the JK flip-flop. Finally when the clock goes low, the JK reacts according to its truth table and 'glitchless' output will result. A flip-flop is used for each output.

Of course, none of this is particularly useful unless we can get out to the outside world and drive a load. The method illustrated in Figure 6 has the advantages of being entirely solid-state, offering total isolation from the ac line, and finally is a poor-man's version of a zero-crossing switch. The ring oscillator, identified in Figure 6 as the triac clock, delivers a high frequency pulse train to the 301 buffers that are being used to drive the pulse transformers. If the other input to the buffer is high, the pulse transformer delivers a train of pulses to the triac which energizes the load. Since the trigger pulses are arriving at a much higher rep rate than the 50-60 Hz line frequency, there will always be a trigger pulse arriving very soon after the line voltage has crossed through zero. This ensures that the triac switching is done with a minimum amount of RFI.

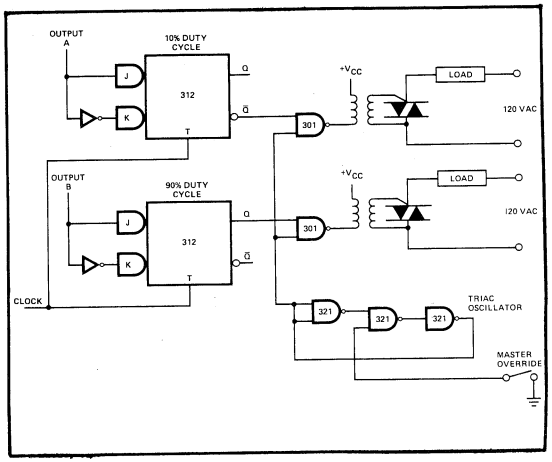


Fig. 6. Driving heavy ac loads through triacs and pulse transformers isolates the logic from line voltages.

In the event that the other input to the 301 is low, the output is automatically clamped high, and there will be no pulse train to the transformer and the load will be off.

One of the advantages of using a flip-flop at the output of the 380 now becomes evident. In Figure 6, we have shown output A as being on for a 10% duty cycle. That means that there will be a diode on only one of the 10 outputs of the 380. Each time the 380 energizes that particular output, the Q output of the JK flip-flop will go high and the load will be energized. If, on the other hand, we had wanted a 90% duty cycle as on output B, there would have been nine diodes instead of one. This can be reduced simply by using the $\overline{Q}$ output of the JK flip-flop instead of the Q. Now the diodes are tied to only those outputs that will turn the load off. Then the 380 energizes that output, the JK is reset to $\overline{Q} = 0$ and the load is shut off. In this way we have reduced the number of diodes from nine to only one.

Introducing provisions for feedback into the system can be very useful, and certainly makes the system much more versatile. When considering feedback you should keep in mind that there is considerable difference between feedback that turns the load on and feedback that turns the load off.

The most common form of feedback occurs when safety switches are added to be sure a load is off when one or more conditions are true. In the event that all of the loads should be turned off simultaneously (as when a heat-sensitive device like a thermostat gives a danger signal) the simplest implementation is to shut the triac oscillator off. This can be done by pulling any of the inputs low, as is being done by the master override switch in Figure 6.

Another desirable place to add feedback paths is at the input of the 301 buffer that is used to drive the pulse transformer. Previously this has been shown as a two-input gate, but in fact it is a five-input device with provisions made for expanding the number of inputs even further by the addition of discrete diodes. Feedback at this point is especially useful because it offers a way to conveniently override the timing sequencer and turn individual loads off.

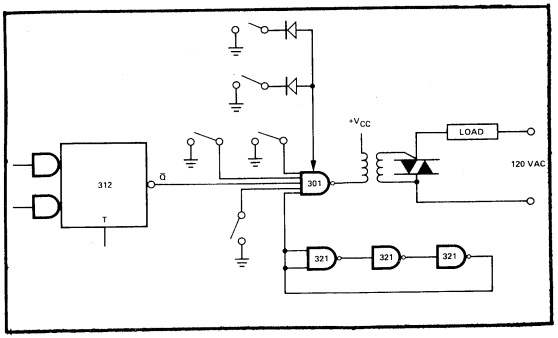


Fig. 7. Closing any one of the five limit switches will override the sequencer and shut the load off.

The 380 timing sequencer could be used to turn a pump on at time 5:00 to fill a reservoir, and to turn it off again at 5:30. A limit switch could then be used to detect the presence of a high liquid level in the reservoir, so that the 380 turns the pump on and the switch turns it off when the reservoir is full. The "off" command by the 380 at 5:30 then becomes a safety instruction to turn the pump off in the event the switch fails.

This simple method is fine for turning a load off, but can't be used to switch a load on. That requires a completely different method, but again one that is easy to implement with HiNIL. It will be remembered that any of the outputs of the 380, when low, will turn the load on. Thus, pulling the output line low will accomplish the same thing. To do this we use a technique of tying discrete diodes to the output line as illustrated in Figure 8.

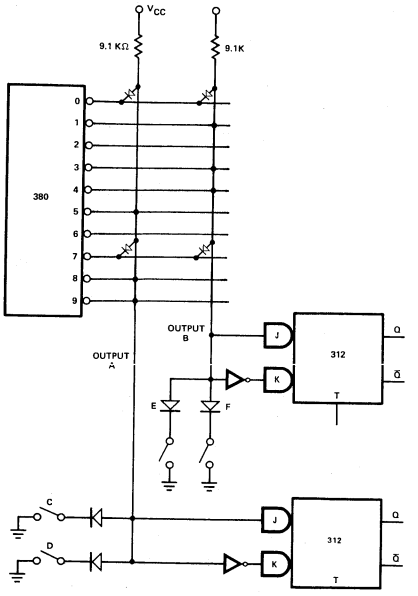


Fig. 8. Feedback paths have been added to the 380 outputs. Closing either switch C or D will energize load A. Likewise, closing either switch E or F will energize load B.

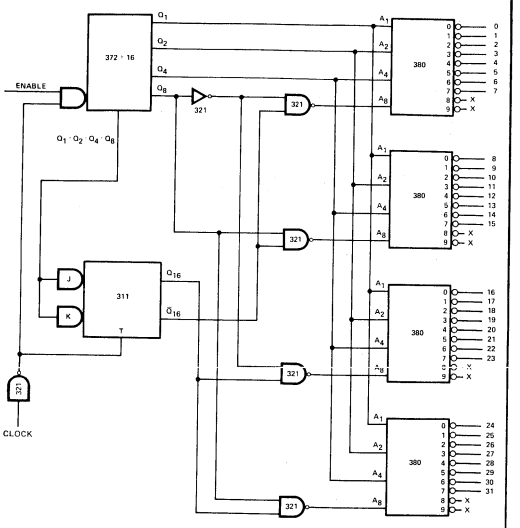


Fig. 9. Cascading 380's to give more than ten outputs. This particular design expands the number to 32.

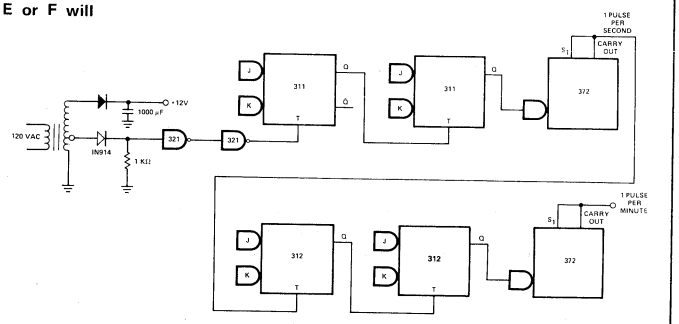


Fig. 10. Pulse generator receives timing pulses from system power supply and delivers 1 ppm. Tap may be inserted after first 372 to provide 1 pps.

This method will cause a delay in the output, since the load will not be energized until the next clock pulse. In the event the delay cannot be tolerated, an alternative method involves tying the switches to the direct reset inputs on the JK flip-flops. This will reset the flip-flop to Q = 1 regardless of the state of either the JK or the clock inputs.

Obviously if we could only divide our time period into ten parts, as in the previous circuits, this system would not be very useful. Fortunately it is relatively easy to cascade 380's to break the cycle into smaller increments. Since the techniques for expansion are relatively straight-forward, we will not belabor the point here. One such circuit for expansion to 32 outputs has been illustrated in Figure 9 to indicate the general procedure.

The use of HiNIL allows a simple solution to the problem of generating accurate one minute clock pulses. This has been illustrated in Figure 10. Its simplicity is highly dependent upon the ability of the 372 hexa-decimal counter to divide by 15 (after suitable hard-wire connections have been made).

This then is a total system for controlling ac loads as a function of time and switch closures. It is easily programmed as to total length of cycle and duty cycle for the individual loads. One convenient method for programming the duty cycle involves bringing the 380 outputs to the front panel via banana jacks and then altering the duty cycle by dual banana plugs containing 1N914 diodes.

Application Note 4
HiNIL 375 Universal Shift Register
By David Guzeman

The HiNIL 375 is a universal four-bit shift register capable of either serial or parallel inputs and serial or parallel outputs. The device is fully synchronous and features active outputs, as well as several interesting twists in the logic that make the device easier to use and more versatile in its applications.

The logic diagram of the 375 is shown in Fig. 1. Each of the four master/slave flip-flops are D-type. Additional gating for the first, FF0, provides J and $\overline{K}$ inputs. By using the complement of the K input rather than the true, a logical advantage is realized in that the complement need not be generated externally. This is illustrated in Fig. 2.

For much the same reason the output of the last flip-flop, FF3, has both Q_3 and $\overline{Q}_3$ brought out. Thus, for data entry from the 375 into a standard JK input, the Q_3 output is tied to J and the $\overline{Q}_3$ output is tied to K. When muliple 375's are being cascaded the Q_3 output of the first 375 is tied directly to both J and $\overline{K}$ inputs of the second device.

The $\overline{PE}$ input switches the flip-flop type D inputs between the parallel input pins and the flip-flop outputs. Thus with $\overline{PE}$ low, the data on P_0, P_1, P_2, and P_3 is transferred into the flip-flops on the next low-to-high clock transition. With $\overline{PE}$ high the parallel inputs are disabled and control of flip-flops FF1, FF2 and FF3 is transferred to Q_0, Q_1 and Q_2 respectively. The input to FF0 is transferred to the $\overline{JK}$ input pins.

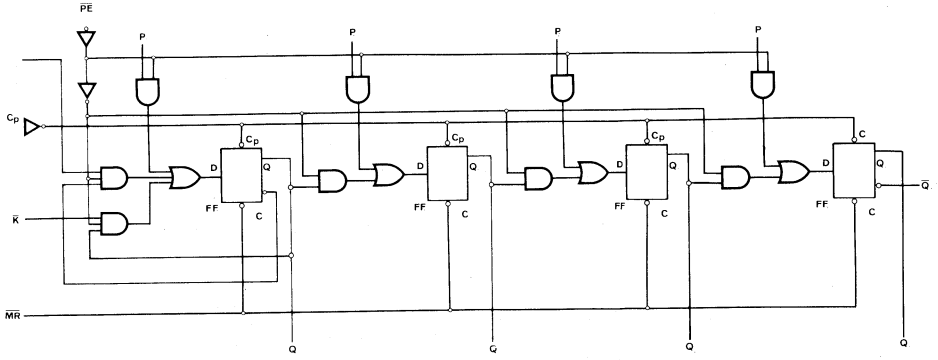


Fig. 1. Logic diagram of the 375 shift register.

Thus with $\overline{PE}$ high, the device becomes a four-bit shift register shifting data one position to the right for every low-to-high clock transition. In addition a master-reset input, $\overline{MR}$, sets all of the flip-flops to zero when it is low, independent of the clock or any of the other inputs.

J	K	Q_{n+1}
L	L	L
L	H	Q_n
H	L	Q_n
H	H	H

Fig. 3. Truth Table for JK input.

The combination of inputs and outputs on the 375 makes it an extremely versatile device. By wiring the parallel inputs to the outputs a shift-left, shift-right register can be constructed. This is shown in Fig. 4 for a 4-bit unit and in Fig. 5 for an 8-bit unit.

In both cases the method is to use the $\overline{PE}$ input as a control to determine whether the shift pattern is left or right. If the $\overline{PE}$ input is high all of the parallel inputs are disabled and the 375's function as standard shift-right circuits. If the $\overline{PE}$ is low, the $\overline{JK}$ inputs are disabled and P_0, P_1, P_2 and P_3 are enabled. Since these are externally connected to Q_1, Q_2 and Q_3 respectively, the device then functions in a shift-left mode.

The 375 makes an excellent vehicle for parallel-to-serial conversions, and vice versa. Fig. 6 is the circuit for a seven-bit parallel-to-serial converter. The eighth input is used to load a marker bit into the register to bring about an automatic loading cycle as each seven-bit word is shifted out of the register. The 322 serves to hold the $\overline{PE}$ input high, thus disabling the parallel inputs, as long as there is a "zero" in the first 6 flip-flops of the eight-bit register. This is usually the case since a "zero" is automatically loaded into FF0 on every load cycle due to the grounded condition of P_0. With no "zeros" present in the shift register the 322 enables $\overline{PE}$ and on the next low-to-high transition of the clock the seven-bit data word along with the "zero" from P_0 is transferred into the flip-flops via the parallel inputs. The "zero" in FF0 immediately disables PE and the next low-to-high clock transition will serve to shift the data one position to the right.

This will continue until the "zero" originally entered through P_0 reaches FF2 of the second 375. At this point the entire seven-bit data word has now been transferred serially out of Q_3 of the second 375. The

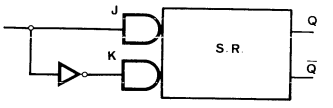


Fig. 2a. Conventional JK inputs require the complement of the data input be generated through the use of an inverter when data is to be input from a single-ended source.

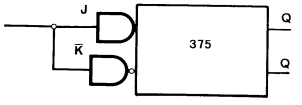


Fig. 2b. By using JK, the 375 eliminates the need for an inverter.

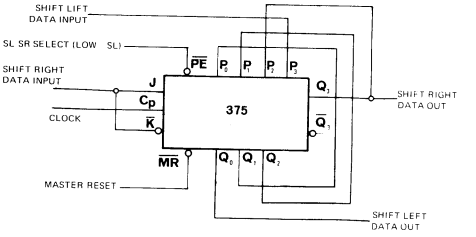


Fig. 4. Four-bit shift-left shift-right shift register.

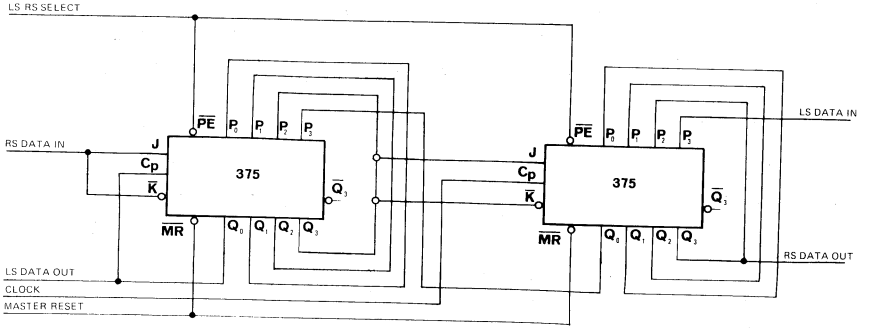


Fig. 5. Eight-bit left/right shift register.

flip-flops to the left of the marker "zero"-bit now residing in FF2 are all logic "ones" since the $\overline{JK}$ inputs are held high and are introducing a new "one" on every clock pulse. Thus when the marker bit reaches FF2 of the second 375 the output of the 322 goes low which once again enables $\overline{PE}$. The next clock pulse will load a new seven-bit data word into the registers. This cycle will continue indefinitely with the 375's putting out an unbroken string of seven-bit serial words. The concept can be expanded to an eight-bit word by adding one 312 flip-flop to the shift-register chain as shown in Fig. 7.

A similar scheme can be used to construct a serial to parallel converter. Since in this instance the data on the parallel output lines will be changing on every clock pulse, it is necessary to inform the rest of the system when the data is correct. The seven-bit serial-to-parallel converter in Fig. 8 accomplishes this by the $\overline{Q}_3$ output on the second 375. Whenever $\overline{Q}_3$ goes high, it is a signal that the data on the output lines is now correct and should be transferred into the system.

The $\overline{Q}_3$ high state has a second purpose. When $\overline{Q}_3$ is high, Q_3 must be low and since Q_3 is tied back to $\overline{PE}$ it serves to enable the parallel inputs. On the next low-to-high clock transition the information on the parallel inputs is transferred into the flip-flops. FF0 of the first 375 receives the first bit of the seven-bit serial data word. FF1 is set to "zero" and the remaining flip-flops are all set to "one". As FF3 of the second 375 goes to "one", the "data ready" signal on $\overline{Q}_3$ disappears and the parallel inputs are disabled. Subsequent clock pulses will shift data into the register. Since all of the flip-flops to the right of the "zero" marker bit originally entered through P_1 of the first 375, are all "ones" there will be no "data ready" signal (and hence no parallel enable) until the marker bit reaches FF3. At that time the seven-bit data word is correctly positioned on the output lines and the PE input is enabled so the next clock pulse will reset the flip-flops to "one" and start the cycle over.

This scheme has been expanded in Fig. 9 to cover eight bits. At the same time an additional pair of 375s are used to store the data that appears fleetingly on the output lines.

The second set of 375s are used as four-bit clocked registers and as such their $\overline{PE}$ inputs are grounded so the parallel inputs are constantly enabled. Their clock, however, is inhibited by a gate controlled by the data change line. When the data is correct this gate allows one clock pulse to pass and the 375s accept and store the eight-bit word. That word remains in the holding register until the next eight-bit

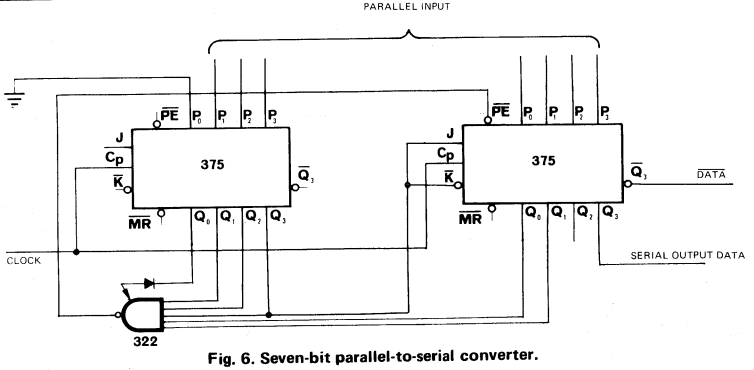


Fig. 6. Seven-bit parallel-to-serial converter.

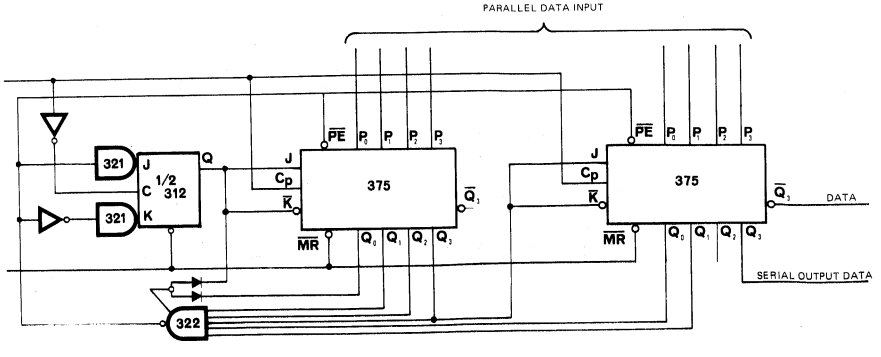


Fig. 7. Eight-bit parallel-to-serial converter.

word is in place, at which time the parallel inputs of the holding register are again enabled and the data in the register is updated.

Although the 375 is connected internally for shift-right operation, that same capability can be added externally. If this is done, the shift-right operation will be done regardless of the state of $\overline{PE}$. In Fig. 10 a circuit has been constructed using this technique that will select serial information from one of two sources.

Another use of the $\overline{PE}$ input is as a shift enable. When the $\overline{PE}$ input is high the parallel inputs are disabled and the device responds to serial inputs through the $\overline{JK}$ pins. By putting a "zero" on the $\overline{PE}$ pin, the $\overline{JK}$ inputs are disabled and the parallel inputs are enabled. In Fig. 11 the parallel inputs have been tied to the outputs of the corresponding flip-flops, P_0 to Q_0, P_1 to Q_1, etc. The effect is to load the flip-flops with the information already in them. Thus dropping $\overline{PE}$ low stops the serial inputs and the shifting action

"In this fashion the 375 can be taken around the state diagram with the individual paths being chosen on the basis of whether the input is a 'zero' or a 'one' on each clock pulse."

without affecting the information stored in the register. When the circuit is connected in this fashion $\overline{PE}$ is being used as a shift enable. This technique may be preferred over the more common approach of inhibiting the clock with a gate since the approach shown in Fig. 11 does not make use of gate circuits. It does, however, sacrifice the use of the parallel inputs.

One very useful application of the 375 is as a counter. There are many variations of these circuits; several will be explored in detail to illustrate the approach. The techniques all use the general state diagram that appears in Fig. 12. By selecting loops of various lengths different count modes can be constructed.

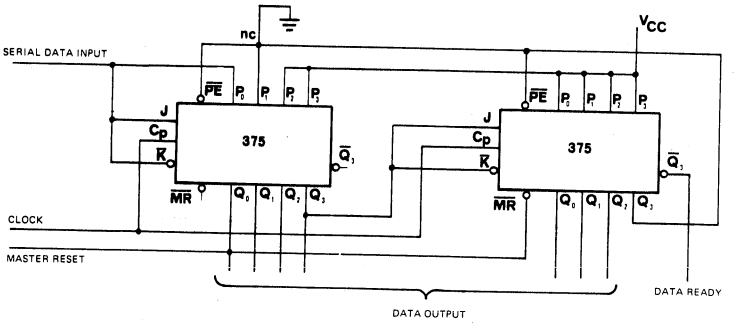


Fig. 8. Seven-bit serial-to-parallel converter.

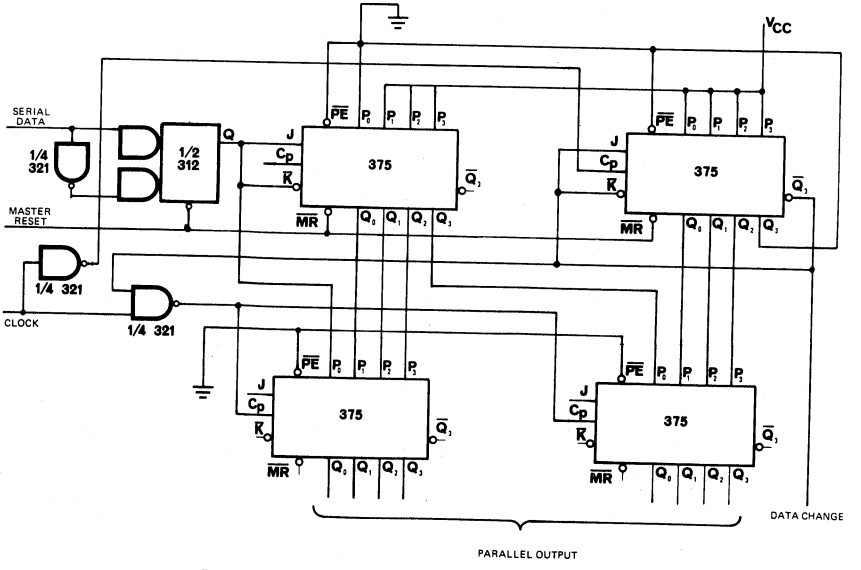


Fig. 9. Eight-bit serial-to-parallel converter with holding register.

"In order to use the 375 as a counter it is only necessary to find a closed loop with the desired number of states."

When examining the state diagram, keep in mind that the numbers contained in the circles are the decimal equivalents of the contents of the register, when read from RIGHT TO LEFT. Thus, the first "one" that is entered serially into the 375 is read as ① , shifting it into the second flip-flop makes it ② , into the third makes it ④ , etc. Each circle, or state, on the state diagram has two entry paths and two exit paths. Assume the register is loaded with all "zeros". The next clock pulse will shift either another "zero" or a "one" in through the $\overline{JK}$ inputs. If a "zero" is shifted in, the circuit remains in the ⓪ state on the state diagram. If a "one" is shifted in, the circuit moves to the ① state.

Assume that a "one" had been shifted in and the circuit is now in the ① state. The next clock pulse brings with it another choice. If a "zero" is shifted in, the register will contain 0100 and will be in the ② state. If, on the other hand, a "one" is shifted in, the register will contain 1100 and be in the ③ state.

In this fashion the 375 can be taken around the state diagram of Fig. 12 with the individual paths being chosen on the basis of whether the input is a "zero" or a "one" on each clock pulse.

In order to use the 375 as a counter it is only necessary to find a closed loop with the desired number of states. To make a mod-10 counter, for example, requires only that there be 10 states in the continuous loop on the state diagram as there are in Fig. 15. Once the desired path has been determined, feedback circuits will be added to force the 375 into this path.

To find the required feedback, let us first label the four flip-flops in the 375 as A, B, C and D (A being

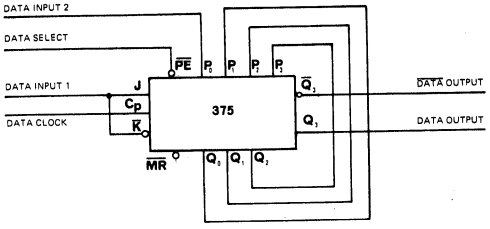


Fig. 10. PE is used to select which of two sources of serial information will be entered into shift register.

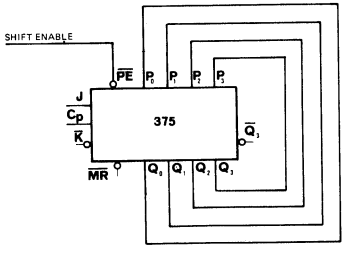


Fig. 11. Using the PE input as a shift enable.

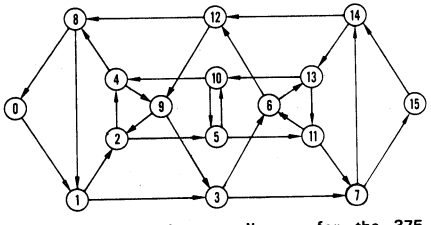


Fig. 12. Generalized state diagram for the 375. (PE high)

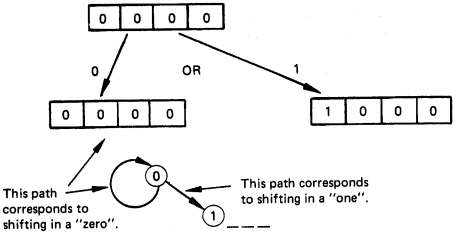


Fig. 13. When the register contains all "zeros" the next clock pulse will either shift in a "one" or a "zero". That determines the exit path from the ⓪ point on the state diagram.

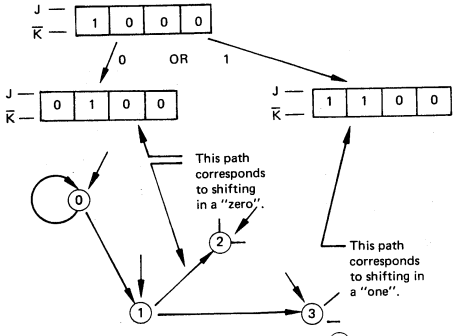


Fig. 14. After the circuit is in the ① state, the next clock pulse will move it to either the ② state or the ③ state.

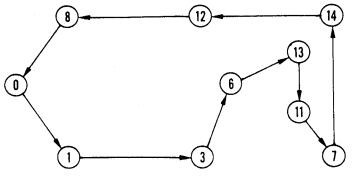


Fig. 15. Basic state diagram for a mod-10 counter using the 375.

the one connected to the $\overline{JK}$ inputs). It is then possible to fill in a Karnaugh map for the J and $\overline{K}$ inputs that will force the 375 along this path. Actually, not all of the squares need be filled in. Since ② is not a state in the mod-10 loop it need not be considered in the feedback circuits. In Fig. 16 all of the squares pertaining to states not in the mod-10 loop have been shaded. Likewise there are several squares that will have no effect on whether the flip-flop receives a "zero" or a "one". Suppose the register contains all "zeros", 0000, and according to the state diagram the next clock pulse should shift a "one" into the first flip-flop, 1000. An examination of the truth table in Fig. 3 reveals there are two ways to shift in a "one". The first is to set in a "one" by putting 11 on the $\overline{JK}$ inputs. The other is to cause the flip-flop to toggle by placing 10 on the $\overline{JK}$ inputs. (Since the previous state was a "zero", toggling will result in a "one".) Thus, either a 11 or a 10 will cause the flip-flop to load a "one". Obviously then, the state of the J input is all that matters, since $\overline{K}$ could be either "zero" or "one" with the same result. Thus, an X ("don't care") has been placed in the 0000 square of the $\overline{K}$ Karnaugh map.

When all the squares have been filled in using this method, the circuit can be implemented. It can be seen that, ignoring shaded boxes and "don't care" states, the J map can be implemented by simply tying the $\overline{D}$ (or $\overline{Q_3}$) output back to the J input. The K input is a little more involved and requires the use of a gate. The actual circuit is shown in Fig. 17.

One drawback of the approach just used is that if the shift-register should somehow find itself in one of those shaded squares, it might not get back onto a mod-10 count, but may just count around another loop of different length. To guard against this occurrence it is good practice to work out all of the other loops and add feedback circuits so that each secondary loop feeds back to the prime one. This insures that after a few clock pulses the 375 will be back on the mod-10 loop. Actually the feedback circuits used in Fig. 17 take care of all but one loop. The complete state diagram in Fig. 18 shows that, even if the register is loaded with ⑩ it will move through ④ and ⑨ to ③ where it rejoins the primary loop. Once on the primary loop it will not get off unless it is forced by external circuits.

A	B	C	D
0	0	0	0
1	0	0	0
1	1	0	0
0	1	1	0
1	0	1	1
1	1	0	1
1	1	1	0
0	1	1	1
0	0	1	1
0	0	0	1

J =

C \ A	00	01	11	10
00	1		X	X
01	0		X	
11	0	0		X
10		1	X	

K =

C \ A	00	01	11	10
00	X		1	1
01	X		1	
11	X	X		1
10		X	0	

Fig. 16. Karnaugh maps used for implementing the mod-10 counter of Fig. 15.

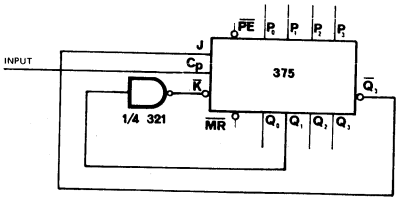


Fig. 17. Complete mod-10 counter.

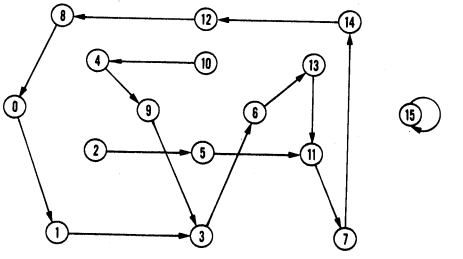


Fig. 18. State diagram of mod-10 counter.

"Another useful approach to designing counters is to produce a single loop on the state diagram that can then be shortened to produce the desired counting mod."

The approach used in Fig. 21 is to use the four outputs with a four-input NAND gate to reset the flip-flops to 0000. Since 0000 is one of the states in the primary loop, the 1111 condition results in an immediate shift to the primary loop.

It is possible to make a variable mod counter with the 375 in various ways, all involving modifications of the feedback circuits. By connecting the flip-flop outputs to the $\overline{JK}$ inputs through a four input NAND gate with the inputs tied to switches as in Fig. 22, the 375 will count by 2, 3, 4, 5, 6, 7 or 8 depending on the position of the switches. All loops are closed and there are no ambiguous outputs.

Another useful approach to designing counters is to produce a single loop on the state diagram that can then be shortened to produce the desired counting mod. To be useful, the loop should be a long one so that a large number of counting mods can be implemented. One such loop can be generated by toggling the first flip-flop whenever the last flip-flop is "zero". This is easy to implement by the circuit in Fig. 23.

The only loop not covered by the feedback circuit of Fig. 17 is the one revolving around the (15) state. Actually, this is called a persistant state since once the register contains 1111 it will remain in this condition. The feedback circuit shown will not break the device out of the persistant "one's" state. In Figs. 19 and 21 are two methods for removing the persistant "ones".

Assume that we wish to use the circuit of Fig. 23 to count by 10. An examination of Figs. 24 and 25 reveal that the loop can be shortened to 10 states if a jump occurs from (1) to (3), eliminating (2), (5), (10), (4) and (9). Furthermore, this jump should be easy to implement because

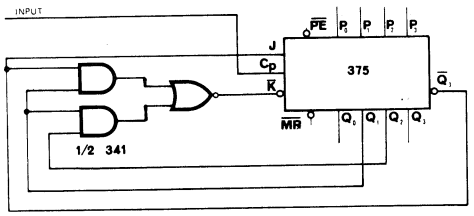


Fig. 19. Mod-10 counter with one loop and no persistant states.

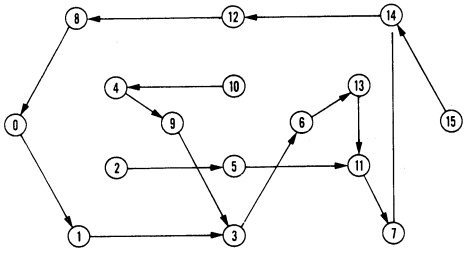


Fig. 20. State-diagram of counter in Fig. 19.

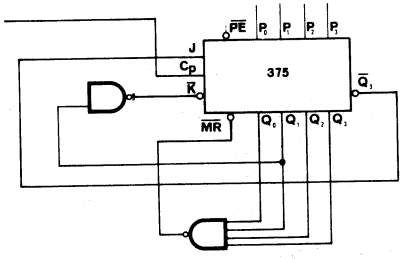


Fig. 21. Mod-10 counter using MR to eliminate the persistant "ones" state.

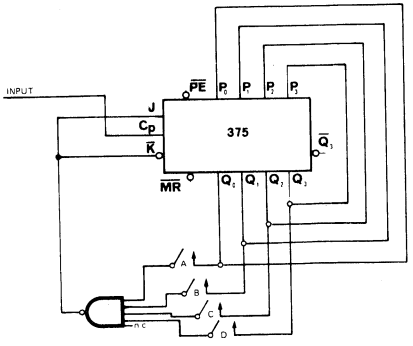


Fig. 22a. Mod as a function of switch closures.

it involves a change in only one flip-flop. Instead of toggling the first flip-flop when the register contains 1000 to produce 0100, if the toggle is inhibited at this point, the next state will be 1100 and the desired count modulus will be achieved.

The first approach to implementing the inhibit function is to force $\overline{K}$ high whenever Q_1, Q_2 and Q_3 are all "zero". Thus when 1000 is reached, the next step is 1100. While this certainly works, it is possible to simplify the circuit by carefully examining the flow table in Fig. 25.

As a first logic reduction, it should be noted that Q_2 equals "zero" is not necessary to force the inhibit. There are four states where Q_1 and Q_3 are "zero" – 0000, 1000, 1010 and 0010 – but two of them, 1010 and 0010, are never seen by the circuit because those two states are jumped over when the loop is shortened for the divide by 10 circuit. That leaves only 0000 and 1000. It turns out that 0000 takes care of itself because Q_3 = "zero", which makes $\overline{Q}_3$ = "one", and by the truth table of Fig. 3, FF0 will be loaded with a "one" regardless of the state of $\overline{K}$. Thus 0000 will lead to 1000 by virtue of Q_3 = "zero". Thus the only state where the toggle will be inhibited is 1000, and Q_2 equal to "zero" is not a necessary condition for this.

The circuit can be further simplified by an even closer examination of the flow table. This requires some insight but the approach is to examine the Q_1 states to see if X0XX can be used to inhibit instead of X0X0. Every line of the flow table where Q_1 = "zero" must be examined separately as has been done in Fig. 26. Many states are eliminated because they are among those that are jumped over. Others are eliminated because as we have already seen, there is no toggle whenever Q_3 = "one". Only two states need be considered, 0000 and 1000, and as we have already seen 0000 will lead to 1000 by virtue of Q_0 = "zero" and Q_3 = "zero". Thus Q_1 can be used for the toggle inhibit with total disregard for the other flip-flops. By forcing $\overline{K}$ to "one" whenever Q_1 = "zero", FF0 will be loaded with a "one".

SWITCH A	B	C	D	MOD	SEQUENCE							
C	O	O	O	2	5	10						
C	C	O	O	3	6	13	11					
C	C	C	O	4	7	14	13	11				
C	C	C	C	5	7	15	14	13	11			
O	C	C	C	6	7	15	14	12	9	3		
O	O	C	C	7	7	15	14	12	8	1	3	
O	O	O	C	8	7	15	14	12	8	0	1	3 OR
C = CLOSED					6	13	10	4	9	2	5	11
O = OPEN												

Fig. 22b. Variable mod counter.

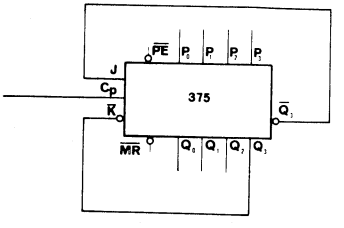


Fig. 23. Simple feedback loop forces 375 into a mod-15 counter.

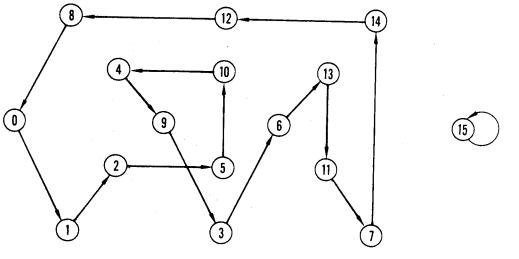


Fig. 24. State diagram for circuit in Fig. 23 has 15 states with no secondary loops and only one persistant state ("ones").

"Another technique for implementing counters is to use the parallel inputs to load the flip-flops and hence modify the counting loop."

The feedback circuits should then consist of the ones already present in Fig. 23 and an additional circuit to shorten the loop. Since each of these circuits should control $\overline{K}$ independently of the other, they should be OR'd together at the $\overline{K}$ input. The complete circuit is developed in Fig. 27.

It will be seen that this analytical technique produces the same circuit arrived at intuitively in Fig. 17.

Another technique for implementing counters is to use the parallel inputs to load the flip-flops and hence modify the counting loop. This approach has been used in Fig. 28 to eliminate the persistant "ones" state. If the shift register contains 1111, the output of the 322 will be low and 0111 will be loaded. This puts the shift register back onto the primary loop and the persistant state has been eliminated.

This same technique can be used to produce a Modulo-10 counter with no persistant states. It uses the same circuit as Fig. 23 but shortens the loop by loading 0001 whenever FF1 and FF2 are both "one". The circuit is in Fig. 29. The two input NAND gate enables $\overline{PE}$ whenever this condition occurs and the manner in which the P inputs are wired causes the desired number to be loaded. The other states where FF1 and FF2 are "one" are jumped over and need not be considered. Since 1111 will also cause the jump to occur, the persistant "ones" state has been eliminated.

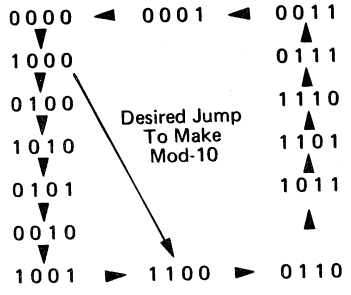


Fig. 25. Flow table for circuit of Fig. 23.

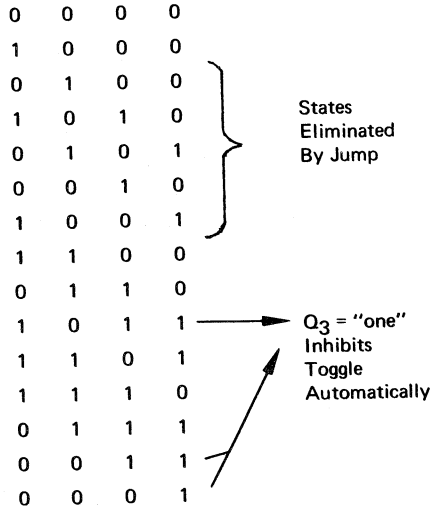


Fig. 26. Using only Q_2 for jump circuit involves examining the flow table for every Q_2 = "zero" condition.

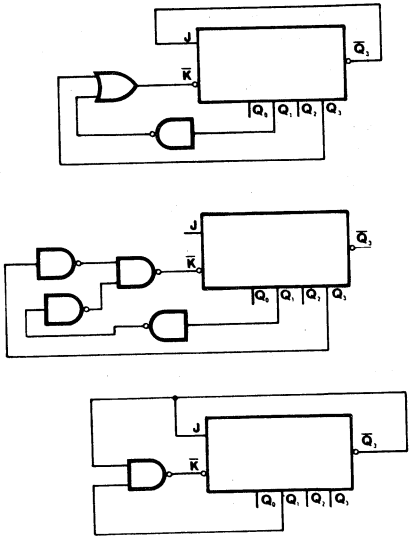


Fig. 27. Implementation of the 10 counter. In (a) Q_1 has been OR'd at K with the normal feedback circuit from Q_3. In (b) the OR has been replaced with its NAND equivalents and these have been simplified in (c).

This technique can be used to implement counters of odd counting mods very easily. The single disadvantage of this technique is the loss of the parallel inputs for pre-loading the flip-flops.

This should serve to illustrate some, albeit not all, of the possible uses for the 375 universal register. The intent has been to simply suggest possible uses without resorting to slavish attention to details. Naturally, in any brief paper such as this, only a few applications can be considered, and in any event the reader will wish to modify these to fit the requirements of his application.

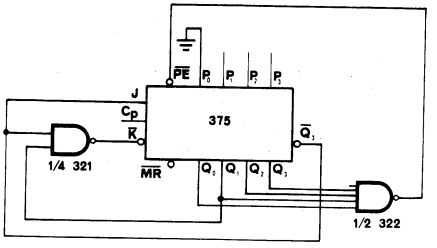
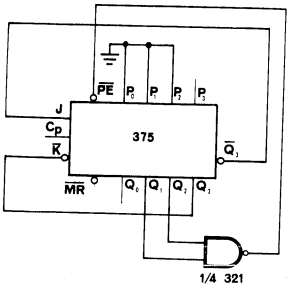


Fig. 28. Modulo 10 counter with one loop and no persistant states.



0	0	0	0
1	0	0	0
0	1	0	0
1	0	1	0
0	1	0	1
0	0	1	0
1	0	0	1
1	1	0	0
0	1	1	0
1	0	1	1
1	1	0	1
1	1	1	0
0	1	1	1
0	0	1	1
0	0	0	1

Fig. 29. Jump caused by gate loading 0001 in parallel inputs.

Application Note 5
High Noise Immunity Logic — Powerful, Versatile and Growing

By David Guzeman

Because this logic family operates at higher voltage levels than CMOS, it can sink and source large currents with greater noise immunity.

With all the attention recently given to the noise immunity in digital systems brought about by CMOS, the fact that there are also bipolar logic families that offer high noise immunities, is sometimes forgotten. In many applications, the bipolar families offer advantages over both TTL and CMOS; in others, a marriage of HNIL and CMOS makes an excellent combination. These families once consisted only of gates and a few flip-flops, but they now include over 30 separate devices, including many MSI circuits such as shift registers, decade counters, BCD to 7-segment decoder/drivers, and 4-bit comparators.

The bipolar families operate at supply voltages 12 v to 15 v higher than conventional logic families. This higher voltage provides 3 v to 6 v of noise immunity. With a 12 v supply, these devices can source and sink large amounts of current. Standard flip-flops and MSI elements can sink 15 ma and source 5 ma; buffers and other special purpose elements can do even more. For instance, a BCD to 7-segment decoder can drive standard LED displays directly; this is not possible with CMOS.

Line driver/receiver

The ability to pump 5 ma of high-state drive current down a line to charge line capacitance quickly makes each HNIL IC a single ended line driver. To complement this, each HNIL element features a high input threshold, 5 v to 6.5 v, so that each IC is an excellent single-ended line receiver. Thus, systems that would otherwise require separate line drivers and receivers, have them included within the logic elements. In typical HNIL systems, shift registers directly drive transmission lines that feed buffer registers at remote stations, saving up to several dollars per line.

HNIL is specified to give 3.5 v of worst case noise immunity over the temperature range of −30° to 85°C and with a ±1 v tolerance on the power supply. This loose tolerance means that inexpensive power supplies

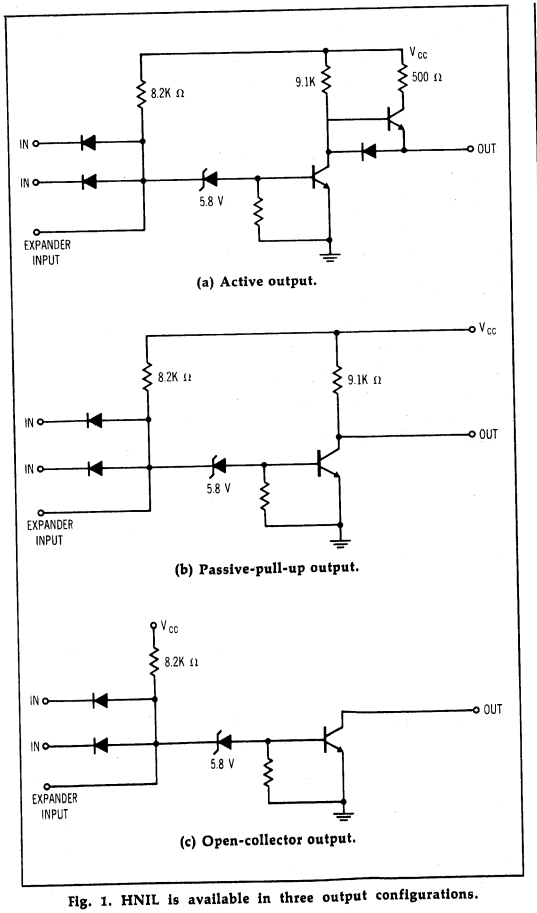


Fig. 1. HNIL is available in three output configurations.

15

can be used with little regulation. In many smaller systems, the power supply is one of the most expensive elements; cutting its cost in half has a dramatic effect on the overall price of the system.

All current bipolar high noise immunity logic families are modified forms of DTL and as such, they have several output configurations — active, passive and open collector (Fig. 1). The active output type features high drive current capability. The passive and open-collector types allow several gates to be wired in parallel to collector-AND the outputs. The passive pull-up types have the pull-up resistor on-chip and do not require any external components for ANDing. The open collector types allow a greater number of gates to be ANDed, but an external resistor must be used. The AND gates are virtually free and allow extensive package size reductions. Special expander input pins are provided on most HNIL elements. When combined with discrete 1N4148 diodes, these increase the number of inputs to the device. For instance, a 5-input gate can be turned into a 7-input gate (Fig. 2). For those devices that don't have expander inputs, a similar technique, called second level gating, accomplishes the same thing by creating a diode AND gate in front of the IC logic elements (Fig. 3). In this case, the diode drop causes a loss of about 0.7 v in noise immunity; this still leaves 2.8 v, more than enough for most applications.

HNIL applications

High noise immunity is important in industrial systems and HNIL has found its way into such diverse applications as gunny sack stitchers, copy machines, automatic weighing equipment, and welding controls. The Paris Metro uses it to control trains, and Delco uses it in the 747's inertial guidance system.

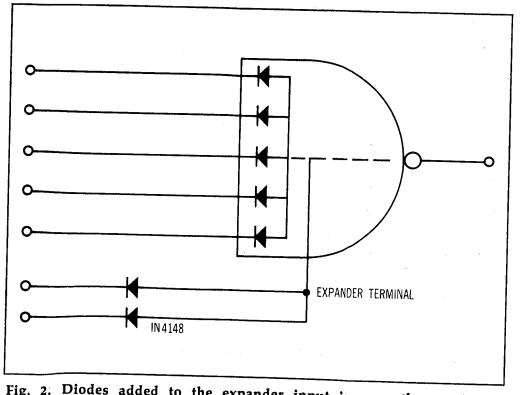


Fig. 2. Diodes added to the expander input increase the number of input lines.

The most appropriate applications for HNIL can best be shown by block diagrams. A typical electronic data processing (EDP) system is shown in Fig. 4a. The diagram is characterized by a large central logic block and a very small number of inputs and outputs. If the choice of logic families for this application were to be based strictly on speed and the cost per element, HNIL would probably not be chosen. The typical industrial control application in Fig. 4b is characterized by a large number of inputs and outputs and a shallow logic block. In this system, there may be only a few gates between the input and output. In selecting a logic family for this application, the user must consider the cost of the input and output circuits, since these may be as much as the logic elements themselves. This application would be suitable for HNIL.

Just add a zener diode

A typical HNIL gate circuit is shown in Fig. 1a. All the elements are designed to operate at supply voltages of either 12 v ±1 v or 15 v ±1 v. The output swings between ground and the supply voltage, providing the basis for high noise immunity. All that is needed in addition is a high input threshold, and that is obtained by including a 5.8 v zener diode. The voltage drop across the input diode is offset by the V_{BE} drop across the input transistor, so that the zener voltage becomes the actual threshold of the circuit.

The active output version of HNIL uses the output diode to bias the upper transistor, causing the upper transistor to lag the lower one, always insuring that one or the other is off. This avoids output current spiking, the cause of self-generated noise common with TTL. Thus, decoupling capacitors on the V_{CC} pins of HNIL are not needed. The oversized geometry of the

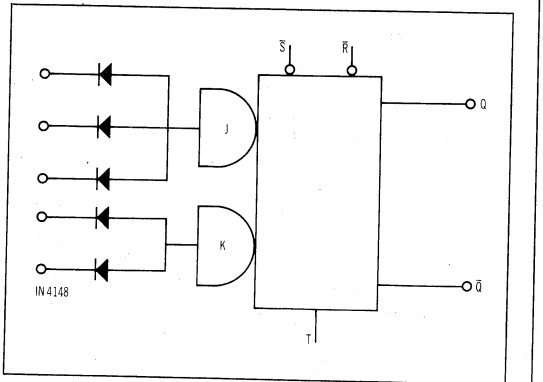
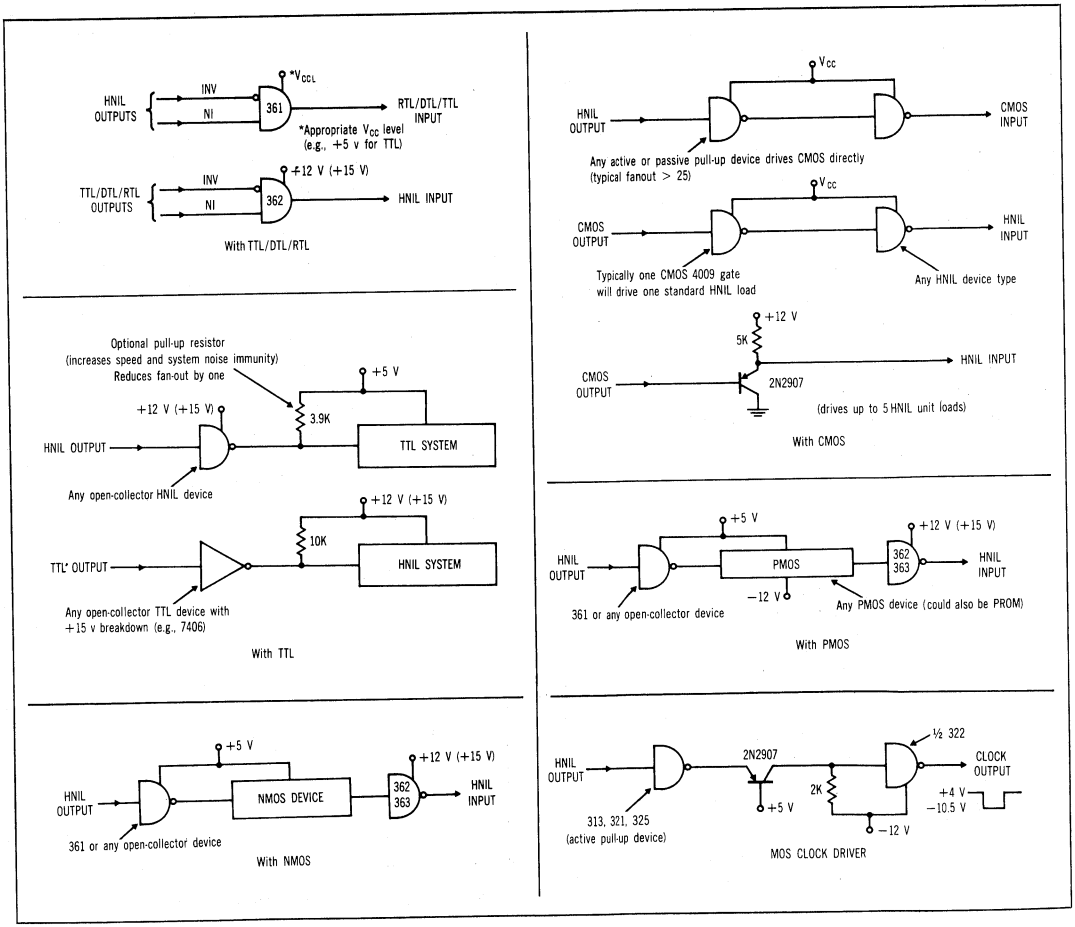


Fig. 3. Discrete diodes can be added to give "second level" AND gates and increase input capacity. Here they are applied to a J-K flip-flop.

upper transistor provides plenty of drive current capability to drive lines and charge load capacitance.

The passive pull-up output (1b) is a variation of the active circuit just considered. Here, the upper transistor and diode have been replaced with a simple 9.1k pull-up resistor to bias the output transistor and set the output high voltage. While this resistor limits the current to prevent current spiking, it also limits the amount of current available for charging line capacitance. These devices, therefore, should not be used for driving lines. The real advantage the passive pull-up offers over the active is the ability to collector-AND the outputs. If several active outputs were hard-wired together, whenever one of the pull-ups was low and one of the others was high, a high current path from the supply to ground would exist. The combination of a low impedance upper transistor in the ONE state output and a low impedance lower transistor in the ZERO state output would produce a near short to ground. Because the pull-up resistor limits the current flow to the lower transistor to about 2 ma, this condition is avoided and the outputs of several passive pull-up devices can be wired together without high-current flows. The number of passive pull-up devices that can be ANDed together in this fashion is equal to the fanout of the devices.

Open collector output devices (1c) are similar to the passive types in use, but the number that can be ANDed is much larger and is set by the size of the external resistors that must be used with this type of



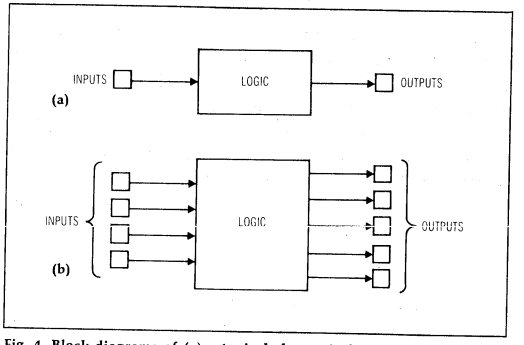


Fig. 4. Block diagrams of (a) a typical electronic data processing system, and (b) a typical industrial control system.

output. Collector-ANDing can best be understood if the connecting wire is considered to be an output of a third "phantom" element and a truth table for this element is constructed (Fig. 6). If two gates are connected in this manner with outputs A and B, either output A or B or both will pull the voltage on the wire close to ground. But the voltage on the wire will be high only if both outputs A and B are high (truth table of an AND gate). This "phantom" AND gate exists physically only in the wire that connects the outputs, but it is as usable as any IC gate available.

There is much more to noise immunity, however, than just a comparison of output voltage swings against input thresholds. The key term is power noise immunity — how much energy must a noise source have before it can cause a logic error? Consider a noise source coupled capacitively to the logic (Fig. 7). The output impedance of the logic output serves to leak

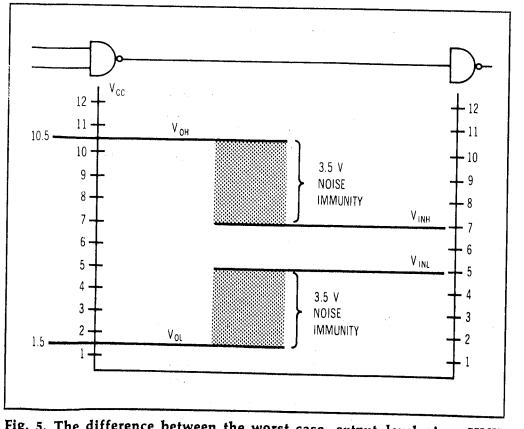
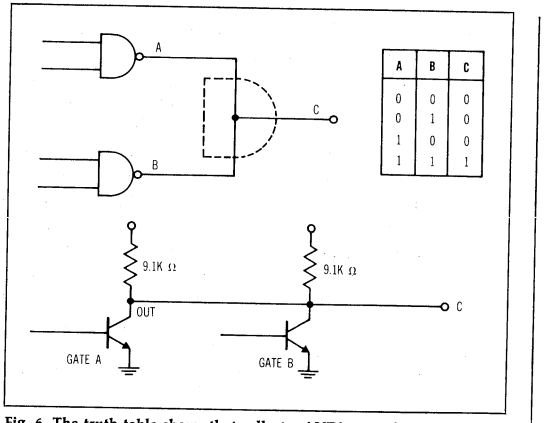


Fig. 5. The difference between the worst case output level gives HNIL 3.5 v noise immunity.



A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

Fig. 6. The truth table shows that collector ANDing results in a phantom AND gate.

noise charge off the capacitor. The lower the output impedance, the harder it is for the noise source to couple enough energy through the capacitor to cause an error. It isn't enough to have good voltage noise immunity, the logic family should also have low output impedances to provide good power noise immunity. The results of tests run on several logic families are given in Fig. 8. In each case, a square wave generator at f = 100 kHz was coupled into a pair of logic elements through a 470 pf capacitor. The amplitude of the generator was slowly increased until a logic error was caused — this amplitude was recorded.

Both HNIL and CMOS perform considerably better than TTL when it comes to power noise immunity. The HNIL passive and active pull-ups differ significantly The passive pull-up output has greater ZERO state immunity because of its lower output voltage, but it

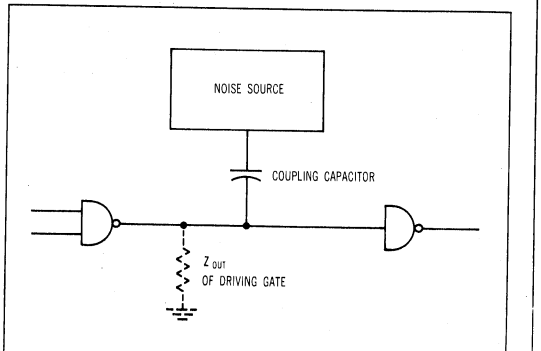


Fig. 7. The lower the output impedance of the driving gate, the faster the noise charge will leak off the coupling capcitor.

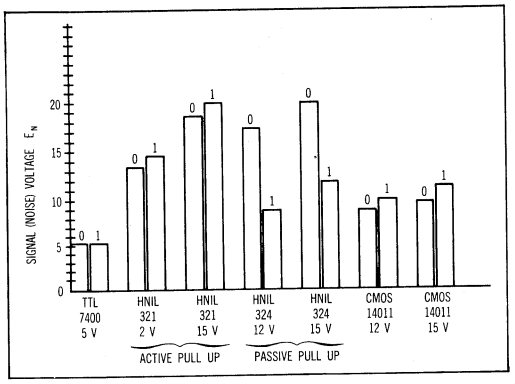


Fig. 8. The amount of signal required to cause a logic error in the ZERO or ONE state shows the relative noise susceptability of HNIL, TTL and CMOS.

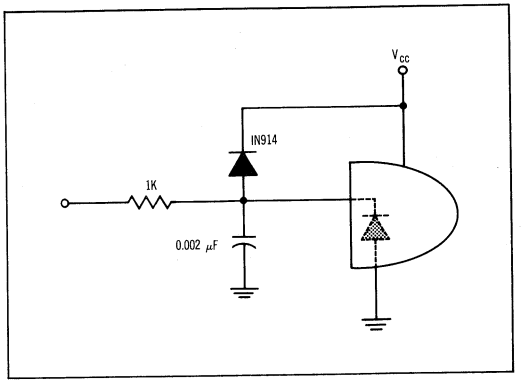


Fig. 9. This circuit is recommended when input protection is needed. The internal substrate diode forms part of the protection circuit.

has much less ONE state immunity due to the high ONE state output impedance. This is somewhat misleading since since passive pull-ups are only used in collector ANDing applications where the pull-up resistor is paralleled to one or more others. The effective output impedance in actual use is reduced by a factor of at least two, causing a corresponding increase in the ONE state immunity. The active pull-up devices have considerably higher immunity than both TTL and CMOS.

Operating practices for HNIL do not differ significantly from those for TTL, but the power supply can get by with much less regulation. And power supply bypass capacitors are not needed on the individual p-c boards because there are no output high current spikes. Other than that, the devices behave exactly like any other current-sinking logic. They have typical input breakdown voltages of 30 v to 35 v, but still need protection from potentially damaging high voltage spikes. Users who would never consider hooking an unprotected TTL input to a long line will do so with HNIL. Even though HNIL's relative high input breakdown levels are considerably better than TTL, the devices should still be protected. A suitable input protection circuit is shown in Fig. 9.

HNIL devices require more power than their TTL counterparts. An HNIL quad gate typically dissipates 85 mw, while its TTL equivalent only dissipates about 60 mw. Both figures are far in excess of the dissipation offered by CMOS, which would be measured in microwatts or even nanowatts so, if low power is a major requirement, HNIL is not the best choice.

Sometimes low power systems that provide high drive current are required. A marriage between a CMOS logic block with HNIL outputs may be the answer (see box, p67). CMOS components are very susceptible to latchup and can even fail if excessive input voltages are supplied; HNIL can provide input protection to CMOS. And, since both logic families operate from the same voltage, interfacing is straightforward.

Keyboard contact bounce causing false inputs is a common application problem, as discovered by one HNIL user. He tried to cure this with a pair of gates cross-coupled to act as a latch but found that noise pickup caused the latch to operate at the wrong times. He then tried the 367 quad Schmitt trigger. This unit has a truth table defined so that open circuits, such as occur during contact bounce, are not recognized as logic ONE's. The only signal that is recognized as a logic ZERO is a solid (current sinking) zero. This eliminated the contact bounce part of the problem. The 367 also reduced his noise pickup in several ways. The Schmitt triggers provided 2.5 v of hysteresis, which added to the noise immunity, and offered 2.5 v of immunity during switching. He then used the enable input to strobe the system to look for input information only at low noise time (when the ac line was crossing zero). He also used the independent slow-down pins to delay propagation and to act as an input filter.

Reprinted From ELECTRONIC PRODUCTS Magazine — December 17, 1973 Issue
645 Stewart Ave., Garden City, N. Y. 11530 • © 1973 United Technical Publications, Div. of Cox Broadcasting Corp. PRINTED IN U.S.A.

Application Note 6
The HiNIL 347 Dual Retriggerable One Shot Theory and Applications

Summary of Operation

The 347 is a retriggerable one shot with both inverting and non-inverting inputs and complementary outputs. The retrigger capability may be defeated by connecting the Q output to the inverting input. Connected in this way, the 347 may be used as a free-running multivibrator. Once initiated, the timing cycle may be terminated by grounding the $\overline{\text{RESET}}$ input.

The output pulse width, T, is given by $T \cong 0.31RC$. Recovery time is non-existent in a retriggerable device, but there is a minimum time required between input pulses (300 ns) and a minimum input pulse width, P, given by $P = 200C + 200$ ns. Longer input pulses are shortened within the device by internal feedback to be equal to the minimum. This time plus the RC network time constant determine the equation for T shown above.

GENERAL DISCUSSION

A simplified logic diagram is shown in Figure 1. For normal operation, $\overline{\text{RESET}}$ is high (or open) and the timing components are connected to R/C. The resistor connects from R/C to V_{CC}, the capacitor to ground. An internal resistor of 10 kΩ nominal is provided on the chip, but the tolerance is too loose for critical applications. It is only included for convenience. For ordinary applications involving triggering on the leading edge of a positive-going pulse or trailing edge of a negative-going pulse (Mode 1), input A is used and B is low (grounded). See Figure 2. If the applications require triggering on the trailing edge of a positive-going pulse or the leading edge of a negative going pulse (Mode 2), input B is used with A high (open) as in Figure 3.

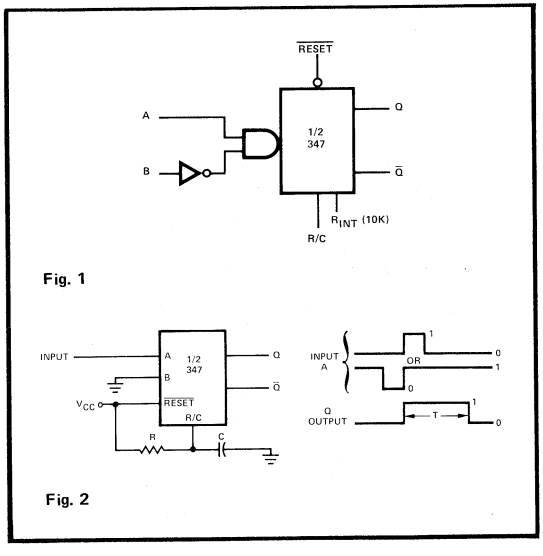


Fig. 1

Fig. 2

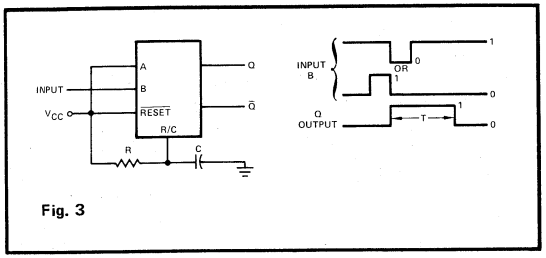


Fig. 3

The 347 is retriggerable in either of these operating modes. That is, the Q output will remain high for another full timing cycle if a second input is applied prior to completion of the first normal timing cycle. The normal timing cycle is $T \cong 0.31RC$ for $C > .02\,\mu F$. For $C \leqslant .005\,\mu F$, a better approximation is $.35RC + 90$ ns. For $.005 < C < .02$, $T \approx .3\,RC + 2\,\mu s$. As an example, suppose $R = 10\,k\Omega$ and $C = .01\,\mu F$, so that $0.3RC + 2 = 32\,\mu s$. Now assume the 347 is triggered and allowed to time out; the output pulse width, T, will be 32 μs. If, instead of allowing the unit to time out, a second pulse is applied after 20 μs; the output pulse becomes $32 + 20 = 52\,\mu s$. This is shown in Figure 4.

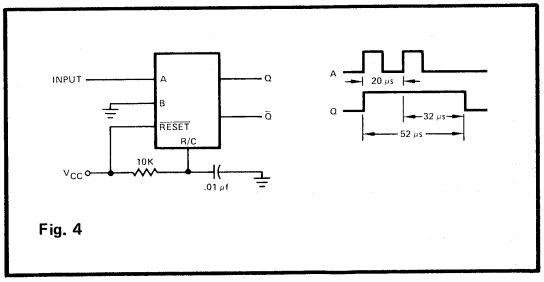


Fig. 4

It is sometimes desirable to terminate the output pulse before the end of the normal timing cycle. This is done by forcing the $\overline{\text{RESET}}$ input low. See Figure 5. If, in the example above, the second input were a low applied to the $\overline{\text{RESET}}$ input, the output pulse would only be approximately 20 μs long.

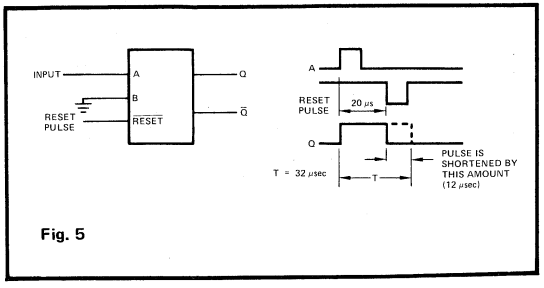


Fig. 5

15

The 347 may also be used in a third mode with the Q output connected to the B input, as shown in Figure 6. One of three results may then occur, depending on the conditions on the A input. If A is high or open, the device will become a free-running multivibrator, generating narrow pulses (W ≅ 250 ns) at a frequency of approximately

$$\frac{1}{T + W}$$

Input A may be used as a control input to turn the multivibrator ON and OFF. When A is high, the device will free-run; when A is low, it will not free-run. If A is held normally low but allowed to go high for a period of time less than T, the 347 will act as a normal, non-retriggerable one shot. A second input applied before completion of the normal timing cycle, T, will be ignored. However, if the second input overlaps the end of the normal output pulse, the unit will recycle. This is illustrated in Figure 7.

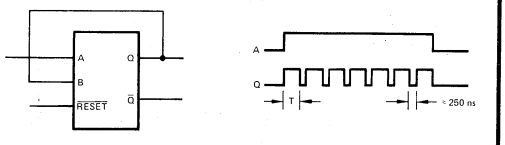


Fig. 6

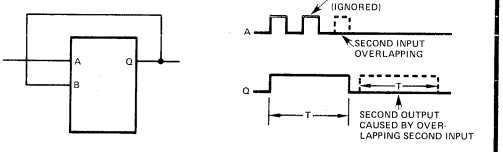


Fig. 7

DETAILED DESCRIPTION

Although the circuit of Figure 1 is accurate enough for a basic knowledge of 347 usage, the complete logic diagram of Figure 8 is required to understand the detailed operation of the circuit, particularly the differences in the three functional modes. In mode 1, with A as the input terminal, B is grounded and I is high. In the steady state, when A is low (prior to firing), gate 4 output (E) will be high along with gate 3 output (H). With these two inputs high, gate 5 output (F) will be low, latching E high. Gate 3 is now enabled, ready for a high on A to trigger the device. See Figure 9. The input to the Schmitt trigger is H, so the output, J, is also high, setting Q low and $\overline{Q}$ high in anticipation of the trigger pulse. The capacitor is charged to the zener voltage. When A goes high, H starts low, discharging C. During the downward transition of H, the Schmitt trigger fires at Point 2 and Q goes high. When H reaches Point 3, the threshold of gate 5, F goes high and E latches low, shutting off gate 3 and H starts toward V_{CC} again, with C charging through R at time constant RC. When C becomes charged to the upper threshold of the Schmitt, (Point 1 on Figure 9) Q goes low again. The timing cycle is complete.

The threshold of gate 5 is set so that C will be nearly discharged before starting to charge again, assuring a full, stable output pulse. This threshold and that of the Schmitt trigger are both determined partially by one V_{BE}, so that they will track with V_{CC} and temperature. Latch 4/5 (E) is reset when A goes low again, readying the 347 for another trigger. If the second trigger occurs before C is charged all the way to the upper Schmitt threshold, C will again be discharged and Q will remain high for another complete cycle. The device has thus been retriggered. See Figure 10. If the $\overline{RESET}$ is pulled low before the completion of the timing cycle, gate 7 will short the timing resistor, R, with approximately 400 Ω, speeding up the charge time and therefore shortening the cycle. This input also disables gate 1 so that gate 3 will not turn on and shunt the 400 Ω across V_{CC} to ground.

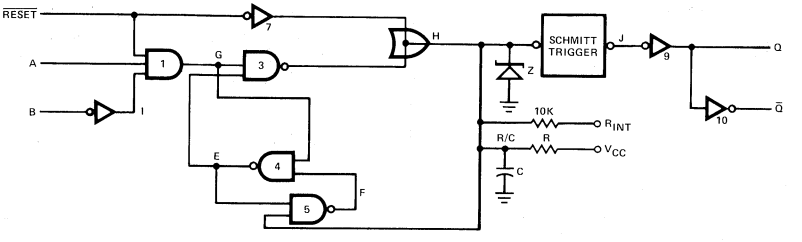


Fig. 8

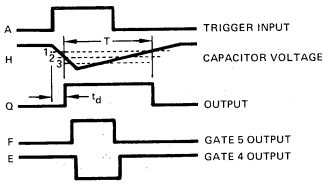


Fig. 9

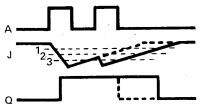


Fig. 10

Modes 2 and 3 utilize inverter gate 2. Gates 3, 4 and 5 plus the Schmitt trigger interact just as in mode 1 except that gate 2 inhibits gate 1 as long as B is high. In mode 2, A is held high. If B is pulled low, I goes high, allowing one cycle, but E stays low, inhibiting gate 3. (Figure 11.) Now when B goes high,G goes low, resetting E, and gate 3 is enabled so that when B again goes low another output pulse is initiated. Retriggering is again possible. Input B need be high only long enough to reset the latch before the unit may again be fired. For trailing edge triggering, the time between positive pulses must be long enough to meet the minimum input width requirements of mode 1 operation. This is just the opposite from input A for mode 1 usage, which is to be expected from Figure 1.

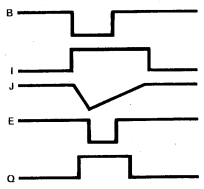


Fig. 11

Mode 3 is the same as mode 2 except that B = Q. In other words, the unit can trigger when the output is low. But as soon as it triggers, the output goes high, inhibiting further triggering until the end of the cycle. At the end of the cycle the output will go low, recycling the device. Input A may be used in either mode 2 or 3 to inhibit the operation, just as B may be used in mode 1. The only difference is the sense of the inhibit input. So if A is brought low after only the required minimum time, the 347 will cycle only once unless A is allowed to be high again precisely at the end of the cycle. Even then, the recycling will result in a distinct second pulse with Q low for a short time in between pulses, instead of a single extended output pulse. Retriggering is defeated.

APPLICATIONS INFORMATION

The minimum input trigger required, P, is primarily a function of the timing capacitor, C, and the worst case value is 200C + 200 ns. There is some dependence on R, but it is minor. In our example, the minimum time is 200 ns + 200 ($.02 \times 10^{-6}$) = 2.2 μs. In modes 1 and 3, input A must be high for this time; in mode 2, input B must be low for this time. In mode 3, the second, overlapping input must overlap by the minimum amount. Refer again to Figure 7. The device will trigger with narrower inputs, but the output pulse width will be shortened. Such shortening is a function of the input pulse width, as shown in Figures 12 and 13. The output pulse width is generally unpredictable for times shorter than 50C. For smaller capacitors and larger resistors, the effect is more pronounced. There is also a delay between the input and the output which is again a function of C, being equal to as much as 30C + 300 ns. Typically, the delay runs about 18C + 200 ns.

P_{OUT} (NORMALIZED) VS. P_{IN} AS A FUNCTION OF C

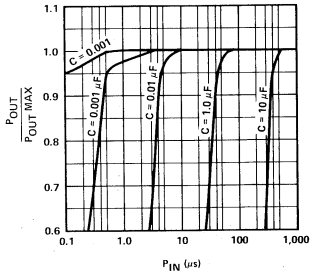


Fig. 12

P_{OUT} (NORMALIZED) VS. P_{IN} AS A FUNCTION OF R

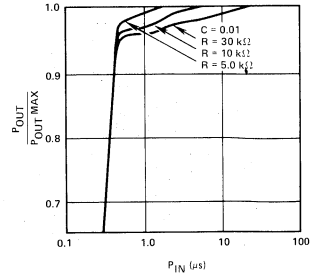
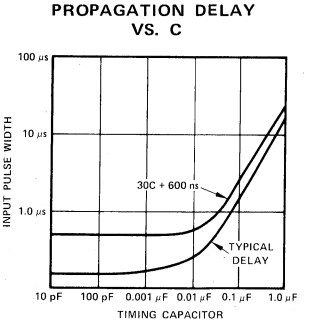
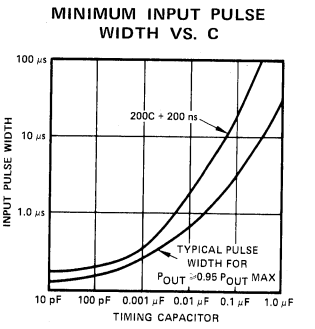


Fig. 13

15



(a)



(b)

Fig. 14

Figure 14 shows both the delay and minimum input pulse width as a function of C. Typical values are shown as well as the worst-case equations. Figures 15 and 16 show nominal output pulse widths as a function of R and C.

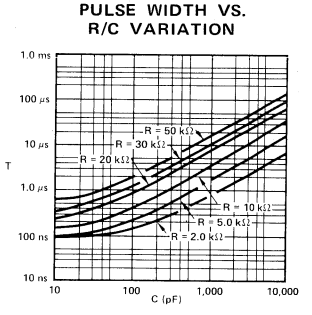


Fig. 15

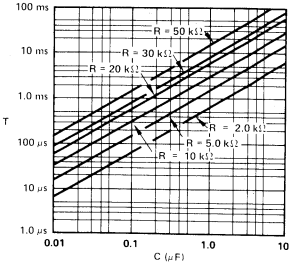


Fig. 16

The time required between inputs (high on A, low on B) is independent of the timing components, and is only the time necessary to reset all the input stages. This time is of the order of 100-300 ns. This fact may be used to advantage if the input trigger pulse available is less than the minimum given above, but an extra delay equal to the available pulse width is acceptable. Simply switch to trailing-edge triggering by using the other input. For example, if the minimum time, P, is 5 μs and the input available is a 0.5 μs positive-going pulse but a 0.5 μs extra delay can be tolerated, pin A is left open and the input is applied to B. The effective input pulse width now becomes the time between pulses and the output is merely delayed by the real pulse width.

The timing resistor may have values from 3 kΩ to 30 kΩ for full temperature operation. If the temperature range is restricted to 0°C to 55°C, the maximum is increased to 50 kΩ. For applications in which $\overline{\text{RESET}}$ will be used, a minimum of 5 kΩ is recommended. The range of the timing capacitor for full temperature operation is 0 to 10 μF. The limited temperature range allows values up to 20 μF. For larger values of C, the circuit of Figure 17 is suggested. The timing equation is modified to be $T \cong 0.15RC$. The minimum input pulse width, $P \cong 5C$, and the delay $\cong 0.5C$.

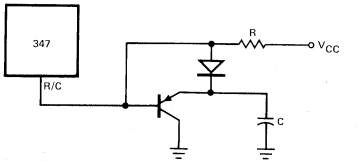


Fig. 17

Figures 18 and 19 show typical behavior of the output pulse width of the 347 as a function of V_{CC} and ambient temperature, respectively. The dotted line in Figure 18 indicates the variation over the entire 11-16 V V_{CC} range, with 12 V taken as nominal.

The 347 is designed specifically for use in noisy environments. All normal trigger and reset inputs have standard HiNIL thresholds of around 6 volts. In addition, the integrating timing arrangement makes the device insensitive to noise on the power supply. Some typical applications are shown below.

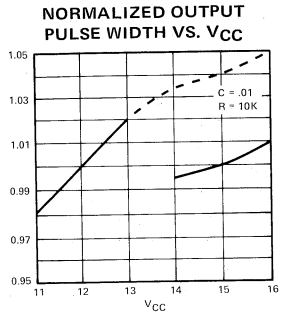


Fig. 18

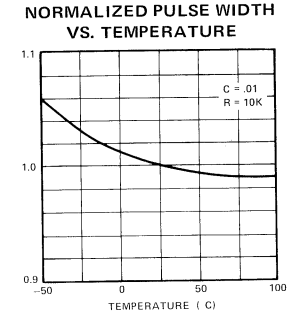


Fig. 19

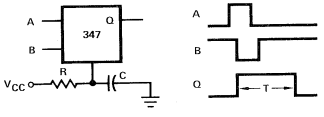


Fig. 20 COINCIDENCE DETECTOR

The circuit of Figure 20 is a coincidence detector. If A is high at the same time B is low, an output pulse will occur. If both signals to be detected are positive-going, one must be inverted before applying it to input B.

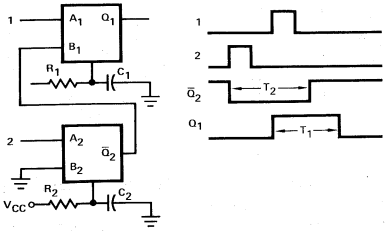


Fig. 21 ENVELOPE COINCIDENCE DETECTOR

Both halves of the 347 are used in the envelope coincidence detector of Figure 21. Output Q1 occurs if input 1 is present within time, T_2 after the beginning of input 2.

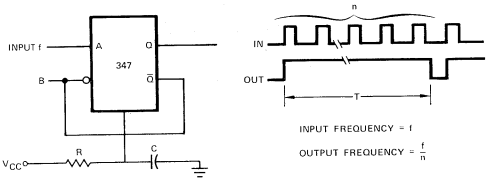


Fig. 22 FREQUENCY DIVIDER

To use the 347 as a frequency divider (Figure 22), the time constant is set by the formula

$$RC \cong \frac{n + \frac{1}{2}}{.31\ f}$$

where f is the input frequency and f/n is the desired output frequency.

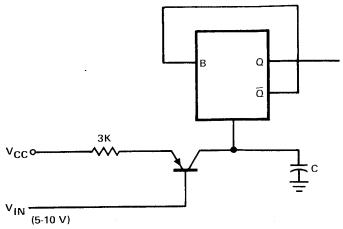


Fig. 23 VOLTAGE TO FREQUENCY CONVERTER

In the voltage to frequency converter of Figure 23, the 3K resistor and the PNP transistor convert the input voltage to a current. As the input varies, the charging rate of C varies proportionally.

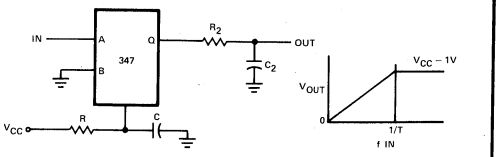


Fig. 24 FREQUENCY TO VOLTAGE CONVERTER

Figure 24 is the complement of Figure 23; a frequency to voltage converter. The output duty cycle is proportional to input frequency up to $f = \frac{1}{T}$.

R_2C_2 integrates the output. The Q output may be used to get a 1/f function.

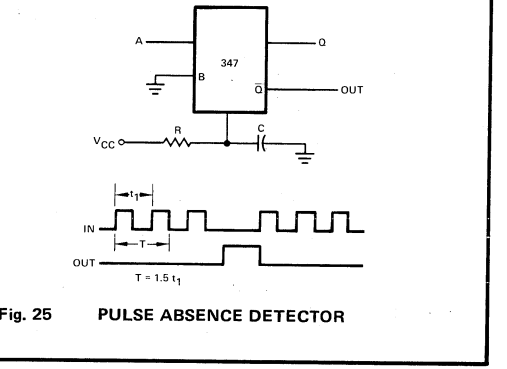


Fig. 25 PULSE ABSENCE DETECTOR

The circuit shown in Figure 25 is a simple pulse absence detector. If a retrigger pulse does not occur within the cycle time T after the previous input pulse, the device will time out and generate a positive output at T.

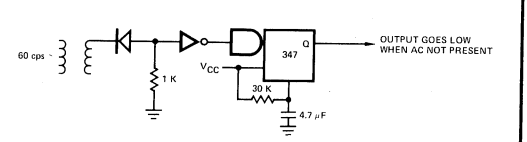


Fig. 26 AC LINE DETECTOR

Figure 26 shows a method of monitoring an AC input source and generates a level to monitor the presence of the AC signals. The retrigger capability of the 347 is utilized when the output period is slightly longer than the 60 cps (or 120 or 240 cps) of the AC source. As long as the 60 cps clock is present, it retriggers the one shot and extends the high state one more period. If the AC source goes away, no retrigger pulse will occur and the one shot will "time out" (go low) indicating loss of AC. This output could be used to initiate a counter whose output displays how long AC was not present.

Application Note 7
Using Bipolar Logic To Improve Performance in CMOS and Microprocessor Systems

In increasing numbers of applications, CMOS and microprocessors (μP) are proving to be the engineer's choice in a wide variety of system designs. The advantages which these technologies offer over other logic devices include — in the case of CMOS — low power dissipation, improved noise margin and wide voltage supply range; with μPs, there are component cost reductions and improved system versatility, compared with hard-wired logic.

There are, unfortunately, certain limitations to both technologies where alternate logic elements can be used to optimize overall system performance. In such instances bipolar logic families such as HiNIL or low power Schottky are interfaced with CMOS or μPs to overcome a specific design restraint or perform a unique function.

The advantages of this design approach include:

LP Schottky with CMOS or μP

a. Improved speed performance.

b. Lowest speed/power product.

HiNIL with CMOS or μP

a. Maximized system noise margin.

b. CMOS input protection.

c. Output drive capability (displays/relays).

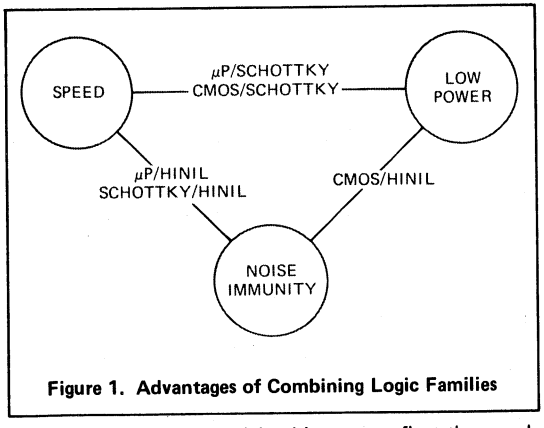


Figure 1. Advantages of Combining Logic Families

The applications discussed in this paper reflect the speed, power and noise immunity advantages offered from various combinations of the above technologies in optimizing system performance. (See Figure 1.) Many of the examples illustrate users' inputs regarding specific problems and solutions.

Noise Problems Cost Money

Consider a manufacturer of electronic game machines who developed a slot machine featuring reduced system power requirements, utilizing CMOS logic to implement the random control logic. After "in lab" testing, the system was released to a hotel, where several machines were placed on various floors for field testing and reliability study. One machine repeatedly contained about 70% less money than machines placed on other floors. It was determined later that noise transients peculiar to that floor enabled a system payoff whenever power was cycled to the machine. In other words, the maid who would unplug the machine to vacuum the hall caused a payout each time the plug was replaced. Noise problems can cost money, and this is a most tangible example.

The system power supply of 12 volts made the solution of this problem a simple matter. Implementing HiNIL bipolar logic on all system inputs overcame the noise (error) susceptibility and further provided input protection from static charge to the CMOS circuits. Later design modification involved replacing discrete transistors with HiNIL gates to drive displays and drum relays.

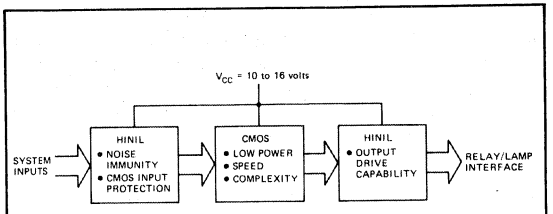


Figure 2. HiNIL/CMOS Design Approach

The resulting design approach is outlined in the block diagram shown in Figure 2. It overcomes the input noise susceptibility of the CMOS devices, allows direct logic control of relays and displays, and in addition operates from 10-16 volts.

CMOS Input Protection

Two other input-related CMOS limitations can be solved with this approach:

a. High voltage (or static) transient protection.

b. Input protection from dc input levels prior to power-up of CMOS circuitry.

The delicate nature of the CMOS oxide region limits the input voltage levels which can occur at the CMOS input. Even with the diode protection networks common to present day devices (see Figure 3), additional input protection in potentially transient environments is generally required.

High voltage static charges (in excess of a few thousand volts) can cause device destruction due to oxide rupture. Static charges in excess of 10,000 volts are commonly generated by routine material and/or personnel movement in a low-humidity or controlled environment.

A second problem is potentially more serious. Input signals greater than V_{CC} or less than V_{DD} (ground) cause forward conduction of the input protection diodes. Current levels in excess of 5 mA are possible and can cause four-layer-diode action (more commonly SCR latch-up) in the CMOS device.

This causes excessive I_{CC} currents, device latch-up and logic malfunction and frequently results in catastrophic failure.

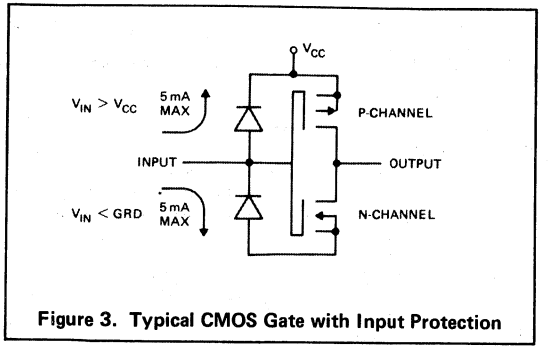


Figure 3. Typical CMOS Gate with Input Protection

The inclusion of a HiNIL Schmitt Trigger at the system input provides protection from both transient and dc destruction of the CMOS device. Figure 4 illustrates its use with suitable delay capacitor to accept transients up to 100 volts for 1 μsec with no resulting error or destruction. In Figure 5 it protects the CMOS from input levels between −5 and V_{CC} + 5 volts. (Refer to HiNIL Schmitt Trigger application notes for complete discussion of circuit operation and application.)

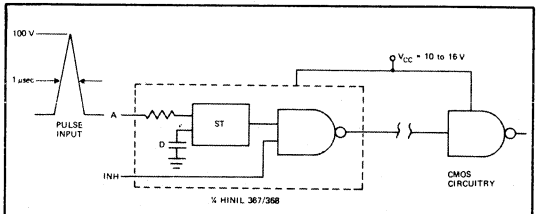


Figure 4. CMOS Input Protection Using HiNIL Schmitt Trigger

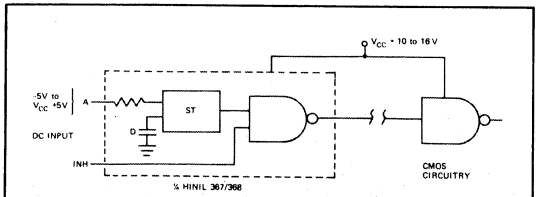


Figure 5. CMOS Input Protection

The second input-related limitation is much more subtle and may involve field maintenance problems long after the system is debugged and in production. Many types of field equipment previously designed with electro-mechanical (relay) or standard bipolar devices feature "on-power" field maintenance – in other words, plugging PC cards in and out with system power on to locate a malfunction logic board. The logic board to be replaced has no V_{CC} connection until plugged in.

If system power remains on, logic (dc) levels will continue to appear at the connector inputs. When the new card is connected, a positive potential, or logic "1" can appear at the CMOS input for a short period until V_{CC} power is realized.

This results in gate destruction, as shown in Figure 6, caused by excessive current flowing through the input diode and low impedance path of the power supply.

Current levels in excess of 5 mA can also cause catastrophic SCR latch-up as mentioned earlier.

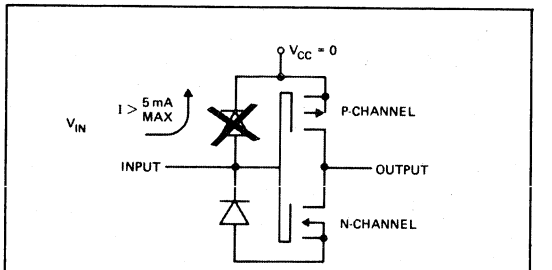


Figure 6. Typical CMOS Gate with Input Protection

Buffering the inputs with any HiNIL devices present a "rugged" bipolar input not susceptible to this failure mechanism.

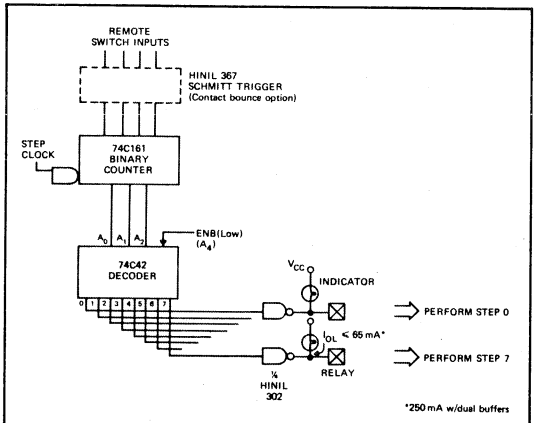


Figure 7. Sequence Controller

Driving Relays and Displays in CMOS Systems

The compatibility of HiNIL circuits with displays, relays and long lines makes them the ideal complement to CMOS for eliminating special interface circuitry. An illustration of this is shown in the sequence control example of Figure 7. (This can be expanded in increments of 8 steps to perform added numbers of step sequences.)

For reasons outlined in previous examples, HiNIL input buffering is provided for essential inputs (e.g., control and clock). The counting and decoding functions are implemented with standard CMOS elements. Each STEP CLOCK transition increments the counter by one count, enabling the corresponding step output from the BCD-to-decimal decoder.

The output interface to step indicator lamps and relays uses HiNIL open collector devices capable of sinking up to 65 mA. (New dual buffers, soon to be made available, will sink up to 250 mA.)

An option for this design is the inclusion of a remote monitor, consisting of a sensor and 8 input multiplexer, to detect a "function complete" signal which is fed back to the COUNTER ENABLE input of the step increment counter. Failure to detect from the sensor that function 2, for example, were actuated would disable the counter, preventing it from incrementing to the next step.

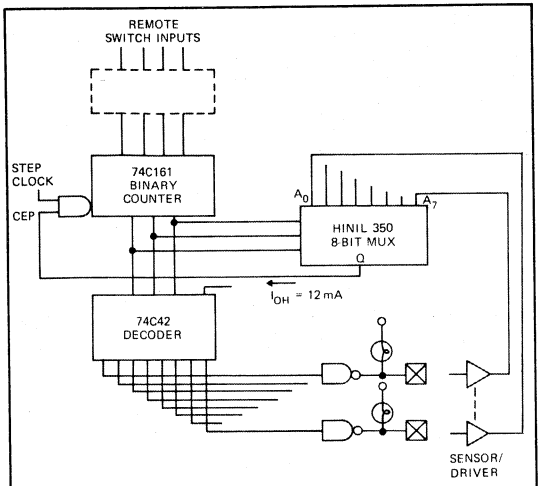


Figure 8. Sequence Controller with Remote Step-complete Feedback Sensor

The sensor/multiplexer can be remote, since the multiplexer is specified for I_{OH} = 12 mA, sufficient to drive several hundred feet of line. The entire system requires no special buffers or interface elements and features low power in the counter/decoder with operation over 10 to 16 volts.

HiNIL and CMOS in Industrial Process Control

Many industrial process controllers and numerical control (NC) machines require small scratchpad/file memories for temporary storage of limited bits of information. Noisy environments warrant special consideration – particularly data inputs where erroneous inputs can have costly results. In this application, I/O functions between the machine control device and scratchpad memory (implemented with 74C89 RAM's) are accomplished with HiNIL circuitry. Address and timing control (not shown) utilize standard CMOS logic.

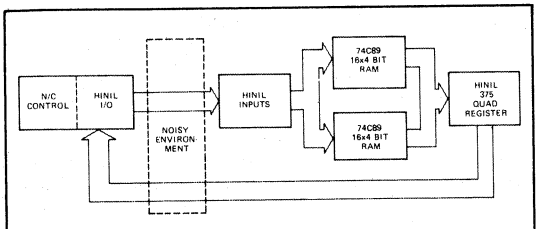


Figure 9. Scratchpad/File Interface

The 74C89 64-bit RAM features three-stage outputs for common bus application to the output register. This configuration is easily cascadable to drive the output lines to the NC I/O subsystem.

Improving Microprocessor Performance

The microprocessor offers the systems designer much flexibility in control systems. A basic processor is shown in the simplified block diagram of Figure 10. The microprocessor provides the register, ALU and control subsystem on a single chip. Peripheral components required are memory devices and interface elements to enable the processor system to "handshake" with other systems.

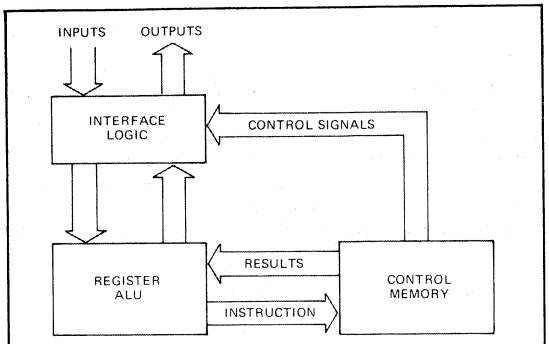


Figure 10. Basic Processor Block Diagram

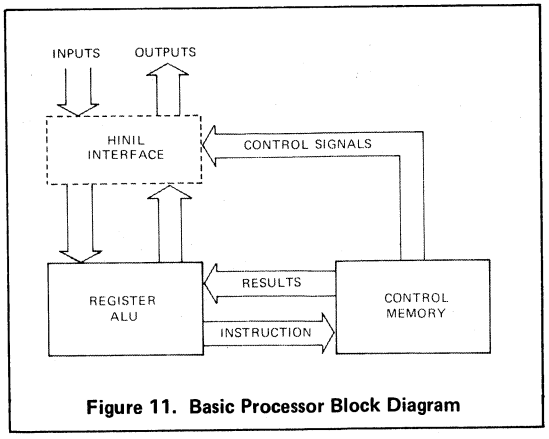


Figure 11. Basic Processor Block Diagram

In many applications, particularly in noisy environments, input/output interface elements are required to maximize noise immunity and provide capability to drive various relays, displays or long lines. The I/O interface function shown in Figure 11 is accomplished using bipolar HiNIL elements to provide output drive capability and input noise protection.

Consider an electronic scale design utilizing a μP and several peripheral RAM's and ROM's. A typical supermarket environment might include fluorescent or incandescent lighting, cash registers with receipt printers, mechanical label markers, meat grinders, etc. Accuracy (i.e., noise immunity) is a prime consideration, because of the ramifications of errors in weight or price/weight calculations (overcharging or loss of profit).

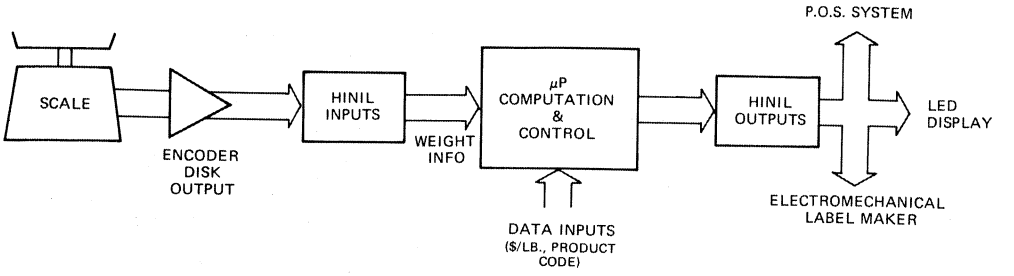


Figure 12. Electronic Scale Block Diagram

The basic design shown in Figure 12 shows how HiNIL can be implemented with the μP subsystem to buffer the digital input code from the weight encoder disk and how HiNIL outputs control and drive the P.O.S. register interface, LED display and the relay associated with the receipt printer or electromechanical label maker. Similar applications involve intelligent process controllers, electronic games and P.O.S. registers.

CMOS with Schottky for Extra Speed

The frequency characteristics of a CMOS device are a function of the supply voltage applied. In practical applications, the maximum frequency of a CMOS counter, for example, is 5 to 10 MHz at V_{CC} of 10-15 volts. As shown in the curve of Figure 13, increased speed is accompanied by sharply increased power dissipation, because of the low impedance to ground during switching (greater than LPTTL or LP Schottky). In many applications speed in excess of 5 to 10 MHZ with supply voltage of 5 volts are required, and alternate means of achieving this, while still maintaining low dissipation, are required.

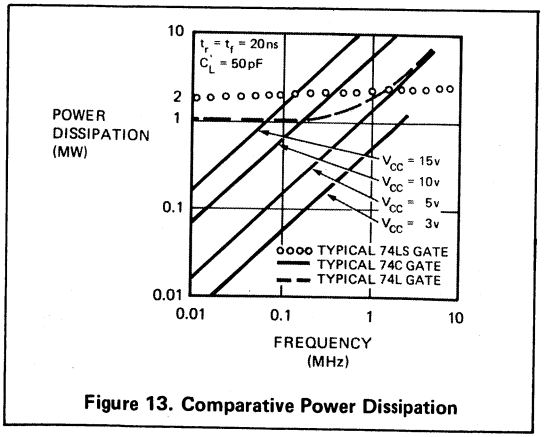


Figure 13. Comparative Power Dissipation

The emerging LP Schottky technology offers speed performance to 35 MHz, TTL function and pin-out and 1/5 the power dissipation of 7400 TTL. It can be used with CMOS to enhance frequency performance from 500 KHz to 35 MHz. The resultant system design features optimized speed/power performance and provides the logic engineer with a valuable design tool for systems requiring low power with high-speed accuracy.

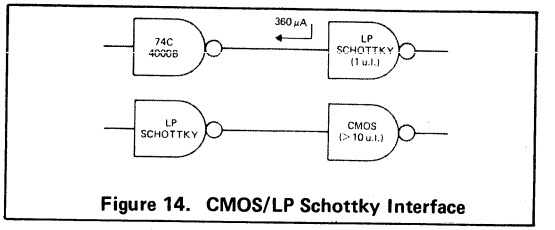


Figure 14. CMOS/LP Schottky Interface

The CMOS/LP Schottky interface is shown in Figure 14. Standard 74C or 4000B (buffered) devices interface directly, providing 360 μA current sinking capability compatible with LP Schottky's I_{INL} spec of 360 μA. A single LP Schottky gate will directly drive a minimum of 10 CMOS loads.

The CMOS/LP Schottky design approach holds the key to reducing power requirements on many existing TTL systems. Electrical (speed and noise) performance and function equivalence is maintained with power reductions of 80-90% over the TTL design.

Lower cost/function and increased availability of complex functions, along with the cheap power supply advantages, will certainly make this combination a serious contender in future designs. By similar analogy, LP Schottky functions can replace standard TTL elements in designs utilizing μPs to improve speed and power performance. Potential applications include electronic games, calculators, electronic cash registers, etc.

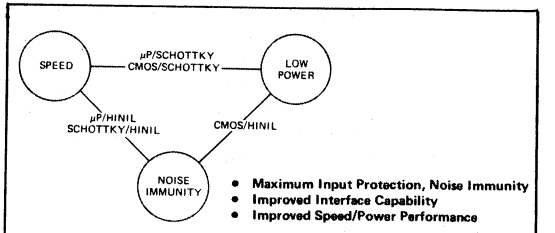
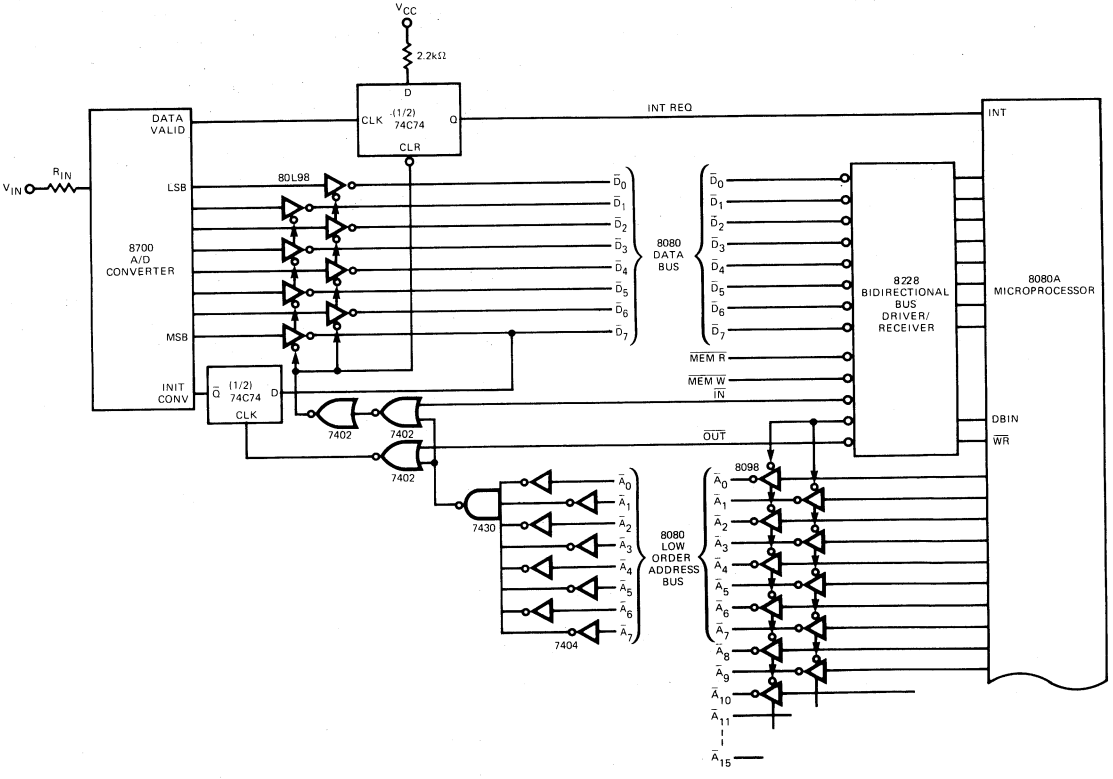


Figure 15. Optimized System Performance

As the spectrum of CMOS and microprocessor applications broadens, an awareness of the limitations imposed by these technologies is essential to optimize system performance. The advantages of combining bipolar logic families with CMOS and μPs — input protection, noise immunity, relay/display compatibility and improved speed/power performance — make this approach an excellent design tool for dealing with those limitations.

Application Note 8
Interfacing the TSC8700 A/D Converter with the 8080 μP System
By Dave Guzeman



15

INTERFACING THE 8700 A/D CONVERTER WITH THE 8080 μP SYSTEM

The growth of microcomputers has included an expansion into process monitoring and control systems, as well as other applications requiring interaction with "real world" physical variables. At the same time, advances in semiconductor technology have allowed complex data conversion functions (A/D, D/A, V/F, etc.) to be performed by small and inexpensive IC's. By integrating these monolithic converter circuits into his microcomputer system, the designer thus can retain the same low cost and small size advantages which make the microprocessor so attractive.

In particular, the popular Intel 8080A microprocessor and Teledyne Semiconductor's 8700 series analog-to-digital converters are well suited to such a combination. This paper describes the basic techniques for interfacing the two, as well as ways to handle some more sophisticated situations.

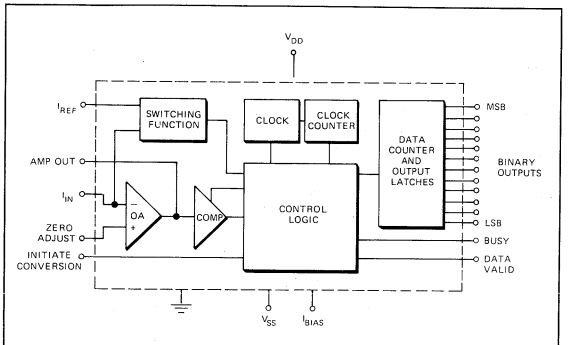


Figure 1. 8700 Series Internal Elements

THE 8700 A/D CONVERTER

Teledyne Semiconductor's 8700 series is a family of monolithic CMOS analog-to-digital converter IC's. All versions — the 8700 8-bit, 8701 10-bit and 8702 12-bit — are integrating converters which can accept an unlimited input voltage range (changed to a current input by external scaling resistor) and provide a latched parallel binary digital output. All are available in 24-pin ceramic DIP, and the 8-bit version is also offered in a low-cost 24-pin plastic package. As may be seen from the block diagram (Fig. 1), each device contains all of the essential elements for a complete A/D converter; only minimal support components are needed.

In addition to the 8, 10 or 12 buffered data output lines, three handshaking signals are provided to ease the interface to the host system. All outputs are CMOS and LPTTL compatible. The DATA VALID output signal is normally high, indicating that the data in the output latches is valid, for the entire cycle except for approximately 5μs before the end of the conversion, when the data is being updated. Notice that the latches maintain the data from the previous conversion even while the next conversion is being performed. A second output, BUSY, is high whenever a conversion is being performed. Finally, an input to the device, INITIATE CONVERSION, allows the function to be operated under system control. A positive-going pulse of at least 500ns duration causes the conversion to begin. If this input is tied high, the conversion will occur in a free-running mode at approximately 800 conversions per second for the 8700 (200 conv/sec for the 8701 and 50 conv/sec for the 8702).

Since the 8700 series devices operate from +5V and -5V supplies, they are particularly easy to interface with the 8080A microprocessor system. Fig. 2 shows a possible hook-up for the 8700's analog inputs and power supply; also

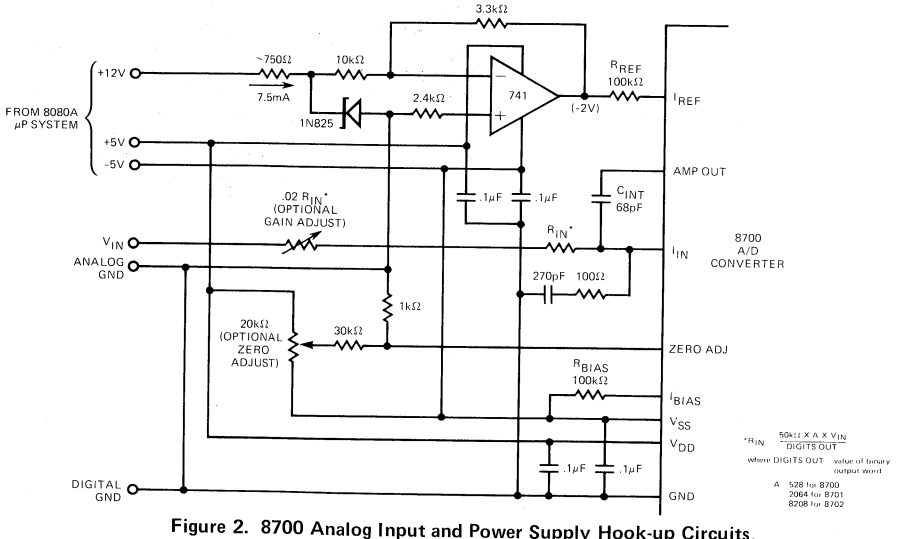


Figure 2. 8700 Analog Input and Power Supply Hook-up Circuits, Including V_{REF} Derived from 8080A System

incorporated is a circuit to supply the necessary negative reference, using a temperature-compensated zener diode and an inverting op amp. Note that the ±5V supplies needed for the 8700, as well as the additional +12V used in the reference circuit, are all available from the 8080A system.

In order to simplify the hardware and software for illustrative purposes, this paper concentrates on interfacing the 8-bit 8700 converter and the 8-bit 8080A microprocessor system. The same principles apply to inter-connecting the 8080A with the higher-resolution 8701 and 8702 A/D converters.

THE 8080A MICROPROCESSOR

The 8080A, an 8-bit microprocessor, communicates within the microcomputer system over two buses, a 16-bit address bus and an 8-bit data bus. During each machine cycle the current contents of the program counter are sent out over the address bus; the memory receives the address and returns the contents of the selected memory location to the 8080A via the data bus. During an instruction fetch cycle, the returning data is interpreted as an instruction.

Communications between the microcomputer and the outside world are via Input/Output (I/O) ports addressed by the address bus. I/O instructions utilize 8-bit addresses; the port address is duplicated on both the low order address lines and the high order address lines of the address bus.

In addition to the address and data buses, the 8080A communicates with the memory and I/O ports via a set of control signals. In particular two control lines, $\overline{IN}$ and $\overline{OUT}$, are used to enable the I/O ports. A logic 0 on the $\overline{IN}$ line will enable the Input port that corresponds to the address on the address bus at that time. The $\overline{OUT}$ line functions in a similar fashion.

THE BASIC 8700 I/O PORT

A basic approach to interfacing the 8080A and the 8700 8-bit A/D converter is shown in Fig. 3. The conversion is started on command of the 8080A, using the INITIATE CONVERSION input of the 8700. When the conversion is complete, the DATA VALID output of the A/D requests an interrupt; the interrupt service routine transfers the current data from the working registers to the stack memory, and the A/D input port is read. A control signal then is sent to the INITIATE CONVERSION input to restart the conversion, and the main program activity is resumed.

It is assumed that the data bus will be shared by many devices, both in the ports and in memory, and that inverting drivers/receivers (such as 8228) will be included in the 8080A system to service this bus. Therefore, 80L98 buffers have been provided at the 8700 to drive an inverted input over the data bus, as well as to provide a three-state function, electrically removing the A/D from the bus when its input port has not been selected. (For applications where inverted signal and high bus-driving capability are not needed, Teledyne is offering a version of the 8700 with three-state outputs.)

Each port of the system is assigned an address by virtue of the way the address bus is decoded to select the port. In the basic input port of Fig. 3, the output of the 7430 gate is low only when all of its inputs are high. This corresponds to address FF_H.

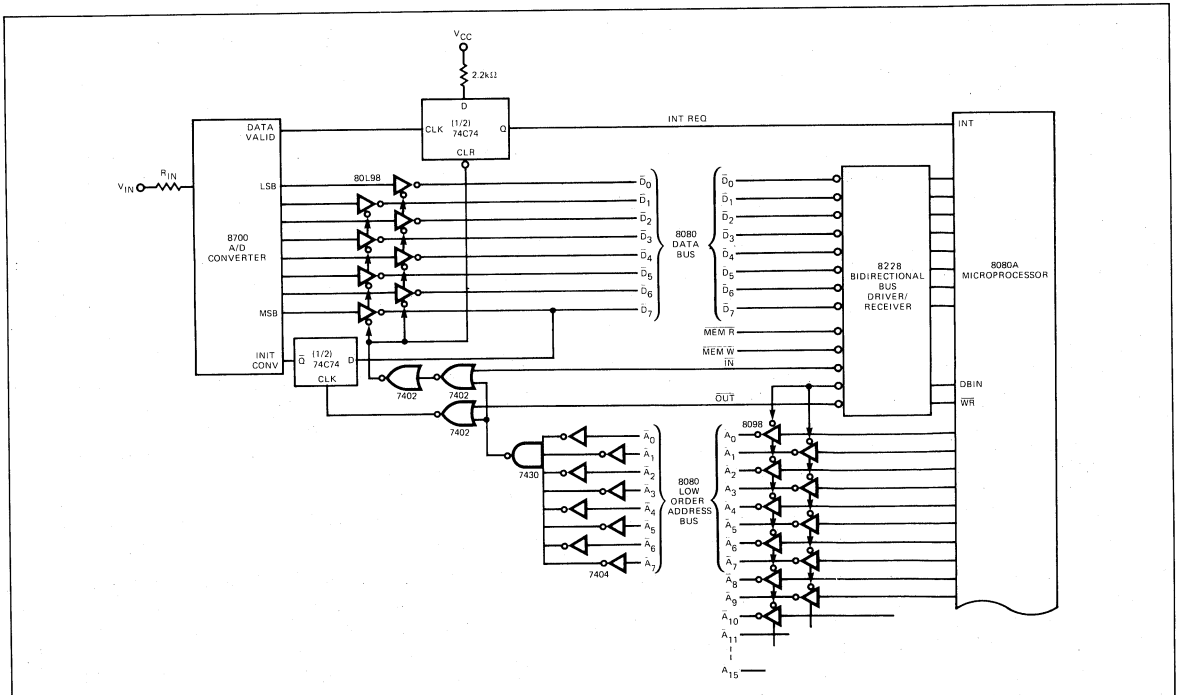


Figure 3. Basic 8700/8080A Interface

```
;INITIATION
        MVI     A,80H   ;THE CONVERSION
        OUT     0FFH    ;IS INITIATED
        MVI     A,0     ;BY SENDING A
        OUT     0FFH    ;BRIEF PULSE
                        ;TO PORT FF
;INTERRUPT
        PUSH    B       ;THE PROCESSOR
        PUSH    D       ;REGISTERS AND
        PUSH    H       ;STATUS ARE SAVED
        PUSH    PSW     ;IN THE STACK, AND THE
        IN      0FFH    ;DATA IS READ AND
        MOV     B,A     ;STORED IN REG B.
        MVI     A,80H   ;THE CONVERSION IS
        OUT     0FFH    ;INITIATED AND
        MVI     A,0     ;THE DATA IS
        OUT     0FFH    ;PROCESSED.
        .
        .
        .
        .
        POP     PSW     ;WHEN COMPLETE,
        POP     H       ;THE REGISTERS
        POP     D       ;ARE RESTORED, THE
        POP     B       ;INTERRUPTS ENABLED
        RET             ;AND PROGRAM
                        ;CONTROL RETURNED
                        ;TO THE MAIN PROGRAM.
```

Figure 3A

To initiate a conversion in the A/D, an output port, also address FF_H, is used. By defining both the input and output ports as address FF_H, the same address decoder, the 7430, may be used for both functions. In this case the output of the 7430 and the $\overline{OUT}$ signal are gated by 7402 to clock half of a 74C74 flip-flop. The D input of the flip-flop is tied to the D_7 line of the data bus. The flip-flop is, in effect, a one-bit output port. Sending the data word 80_H to port FF_H with an output ($\overline{OUT}$) instruction will cause the flip-flop to be set, thus supplying an INITIATE CONVERSION signal to the 8700. A second output instruction, sending 00_H to the same port, will reset the flip-flop and remove the INITIATE CONVERSION signal. Since an output instruction requires ten 0.5μsec clock cycles to execute, the INITIATE conversion pulse will be approximately 5μsec long. After beginning the conversion process by the double output instructions, the 8080A is free to perform other processing operations.

When the 8700 completes its conversion cycle and latches the result onto its internal output latches. the DATA VALID output goes high. This triggers the other half of the 74C74 flip-flop, clocking a logic one from the D input (tied high) onto the INTERRUPT REQUEST line. The result is that the microprocessor is interrupted when the conversion is complete. The interrupt service routine (See Fig. 3A) saves the CPU's working register contents by pushing them onto the stack and then reads the output of the 8700.

To read the 8700 input port, it is necessary to supply the address of port FF_H on the address bus while simultaneously sending out a logic zero on the $\overline{IN}$ control line. The combination of the 7430 and 7402 gates supplies a logic zero to the enabling input of the 80L98 three-state buffers on the outputs of the 8700 and to the clear input of the 74C74 flip-flop on the INTERRUPT line; this puts the 8700 data on the data bus and removes the interrupt request.

After reading the converter data and saving it in one of the registers, the system again pulses the INITIATE CONVERSION input to start the next conversion, restores the stack with a series of POP instructions, and resets the internal interrupt-enable flip-flop. Thus the 8080A only reads the 8700 when the new information becomes available; the rest of the time is spent in processing activities.

HANDLING MULTIPLE A/D CONVERTERS

When multiple analog inputs are involved, conventional system designs have tended to use an analog multiplexer feeding a single high-speed A/D converter. With the increasing availability of low-cost converter IC's, the approach of using a separate A/D for each analog line becomes more attractive. Fig. 4 illustrates a system of eight 8700 converters all supplying data in parallel to an 8080A system.

The system illustrated in Fig. 4 contains many of the same elements as the basic input port of Fig. 3. As before, the data outputs of the 8700s are buffered with 80L98 three-state buffers to drive the bus and to allow them to be disconnected. The decoding circuitry is slightly more complex. The five high-order address lines form the inputs to a 7430 gate which is used to enable a 7442 BCD to decimal decoder. The 7442 performs the final decoding by selecting the appropriate 8700 whenever an INPUT instruction is executed to one of the output ports $F8_H$ to FF_H. Also, the 8700s have their INITIATE CONVERSION inputs tied high so the devices operate in the free-running mode.

The interrupt scheme in this system is far more versatile than that previously illustrated. The user may assign priorities to each of the input ports, so that if one port has already interrupted the system and is being serviced, only a higher priority port can interrupt it. Lower priority interrupts will be delayed until the first port has been serviced.

Each of the eight interrupt input ports is constructed of a 74L74 flip-flop with its D inputs wired high. Each flip-flop is clocked independently by lines from the appropriate 8700 DATA VALID output, transferring the logic one on the D input to the Q output. The $\overline{Q}$ output of each flip-flop is gated onto the $\overline{INT\ REQ}$ line producing an interrupt whenever one of the 8700's completes its cycle. The Q outputs of the flip-flops are buffered by the 8098 and tied to the data bus; this buffer is enabled by a 7430 and 7400 gates to respond to the INPUT instruction at address $7F_H$. The 8080A thus can determine which flip-flop has caused the interrupt and which of the 8700s has completed its conversion cycle.

The interrupt service routine (See Fig. 4A) saves the contents of the working registers with a series of PUSH instructions, and then proceeds to determine which port caused the interrupt. This is done with an input ($\overline{IN}$) instruction to address $7F_H$, which loads the status of the DATA VALID outputs from the 8098 into the accumulator. Here the word can be tested, bit by bit, until a logic one is found. This is then converted to the address of the correct 8700 input port and that port read with an input instruction. At the conclusion of the service routine, the flip-flop is reset by sending a zero to the appropriate bit position of the output port $7F_H$ which shares the same decoding circuitry as the input status port. Finally the stack is restored, and the internal interrupt enable flip-flop is reset.

There is nothing to prevent one of the 8700s from completing its conversion cycle and sending out a DATA VALID signal at the very time that another 8700 port has caused an interrupt and is in the process of being read. If this occurs, the flip-flop tied to the second port will be set and an additional interrupt signal generated. This will have no effect, however, since the

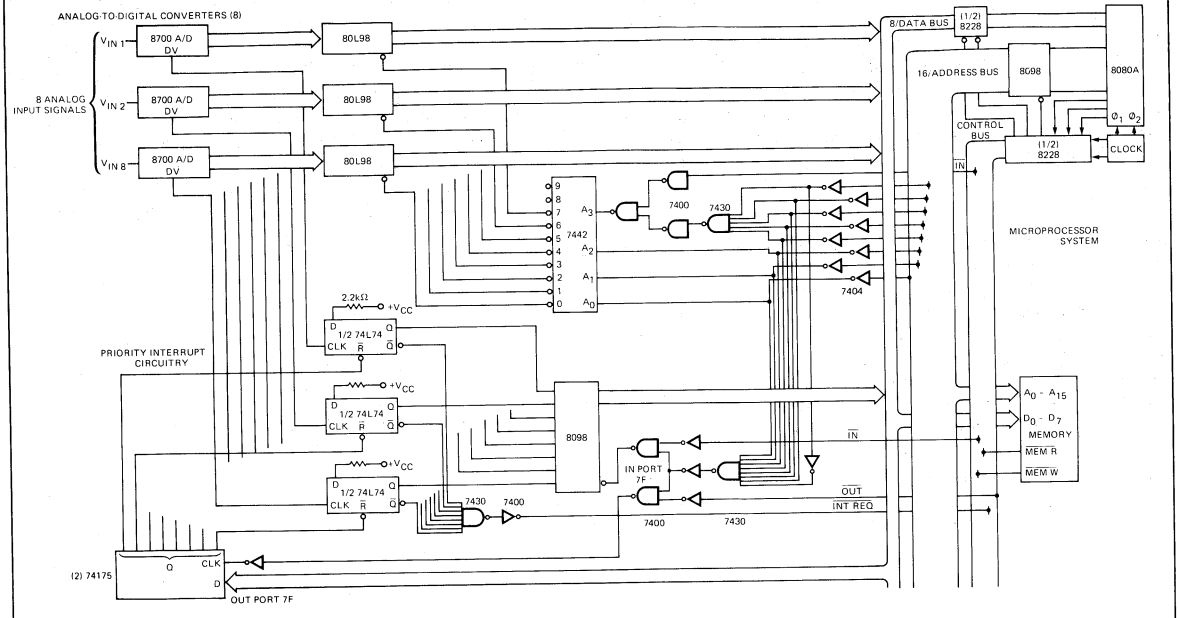


Figure 4. Eight Port A/D Converter System with Maskable Priority Interrupt

```
;THIS IS A PROGRAM FOR RESPONDING
;TO AND SERVICING EIGHT INTERRUPTING
;INPUT PORTS ON A PRIORITY BASIS.
POLLED: PUSH    B       ;SAVE PROCESSOR
        PUSH    D       ;REGISTERS AND
        PUSH    H       ;STATUS.
        PUSH    PSW
        IN      7FH     ;READ INPUT PORT
        MVI     D,0     ;TO FIND WHICH
        STC             ;CAUSED INTERRUPT.
        CMC             ;SET D TO ZERO
                        ;AND CARRY TO ZERO.

LOOP1:  RAL             ;DETERMINE WHICH
        INR     D       ;PORT CAUSED INTERRUPT
        JNC     LOOP1   ;BY ROTATING ACCUMULATOR
                        ;LEFT AND TESTING
                        ;FOR PRESENCE OF
                        ;CARRY.  INCREMENT
                        ;D EACH TIME.
        LXI     H,STABL ;LOAD H AND L WITH
        LXI     B,3     ;STARTING ADDRESS
                        ;OF JUMP TABLE AND
                        ;B AND C WITH 3.

LOOP2:  DAD     B       ;ADD B AND C TO
        DCR     D       ;H AND L, DECREMENT D
        JNZ     LOOP2   ;AND TEST FOR
        PCHL            ;ZERO.  EXIT LOOP
                        ;BY TRANSFERRING
                        ;TO APPROPRIATE
                        ;JUMP COMMAND
                        ;IN JUMP TABLE.

STABL:  JMP     ONE     ;JUMP TABLE
        JMP     TWO     ;CONSISTING OF
        JMP     THREE   ;3-BYTE JUMP
        JMP     FOUR    ;INSTRUCTIONS.
        JMP     FIVE
        JMP     SIX
        JMP     SEVEN
        JMP     EIGHT

RSTR:   POP     PSW     ;RESTORE REGISTERS
        POP     H       ;AND EXIT.
        POP     D
        POP     B
        RET
ONE:    IN      0F8H    ;THIS IS THE
        MOV     B,A     ;SERVICE ROUTINE
        MVI     0FEH    ;FOR PORT #1.
        OUT     7FH     ;IT LOADS THE
        EI              ;PRIORITY MASK
                        ;WITH 1111 1110,
                        ;ENABLES INTERRUPTS
                        ;AND PROCESSES
                        ;DATA.  AT CONCLUSION,
                        ;THE PROGRAM JUMPS
        JMP     RSTR    ;TO RSTR.

TWO:    IN      0F9H    ;THIS IS THE
        MOV     B,A     ;ROUTINE FOR
        MVI     0FCH    ;PORT #2.  THE
        OUT     7FH     ;PRIORITY MASK
        EI              ;IS 1111 1100 WHICH
                        ;KEEPS PORT #1
                        ;FROM INTERRUPTING.
        JMP     RSTR
;THE BALANCE OF THE SERVICE ROUTINES
;ARE OMITTED FOR BREVITY.
```

Figure 4A

8080A's internal-interrupt enable flip-flop is automatically disabled when the first interrupt is received, locking out any further interrupts. (This flip-flop must be reset with an EI instruction, Enable Interrupts.) The first interrupt service routine ends with the resetting of the status flip-flop and the enabling of the internal interrupt enable flip-flop. This removes the source of the first interrupt, but the second status flip-flop now causes a new interrupt which must be serviced in turn. The 8080A will respond to each of the input ports as they complete their cycles, even if several occur in a short period.

So far we have assumed that each of the 8700 ports is of equal importance. When we wish to assign priorities to the ports, it is only necessary to make a slight change in the program — no hardware changes are needed. This is done by holding the reset inputs of selected data valid flip-flops low, which effectively serves to inhibit those ports from causing interrupts. The output port 7F accomplishes this by having its latches loaded with a binary word called a priority mask. Each interrupt service routine begins by loading a different priority mask into the output port and resetting the internal enable interrupt flip-flop. For example, if the priority mask for port number 3 is 11111100, port number 1 and 2 cannot interrupt the processing of port number 3 data; ports number 4 through number 8, however, can cause further interrupts.

If it is necessary to guarantee that no data is ever lost, a slight modification places the conversion cycle under the control of the CPU. This is done by tying the reset inputs of the status flip-flops to the INITIATE CONVERSION inputs of the corresponding 8700's. The process of resetting the status flip-flop after the port has been read will cause the cycle to restart. This has the effect of holding the data on the output latches of the 8700's until it has been read.

INCREASING THE THROUGHPUT

If a great deal of data manipulation is to be done by the 8080A or a large number of 8700 input ports are to be connected to the bus, it is possible to feed data to the system faster than it can be processed. If the analog inputs on some of the ports are changing slowly, additional logic can be added to increase the effective capacity of the system. This involves adding a latching output port with the same address as the 8700 input port corresponding to it. (See Fig. 5) After the input port is read initially, an output instruction to the same address causes the data to be duplicated in the 74175 latches. The open collector feature of the 9386 allows them to be collector-ORed; logic ones at all of their outputs signify that the data in the 8700 latches matches that in the output port. This condition means there has been no change in the analog input voltage and there is no need to reprocess the data. If one of the bits of the 8700 does not match the corresponding bit in the 74175, a zero will be produced on the outputs of the 9386. This will deliver a clock pulse to the 7474 status flip-flop which will in turn interrupt the 8080A. From this point the operation is similar to the system already discussed.

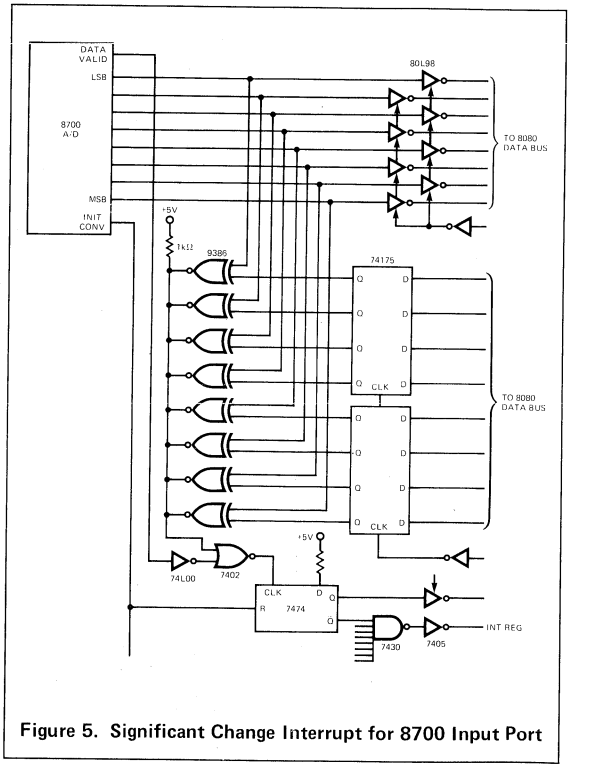


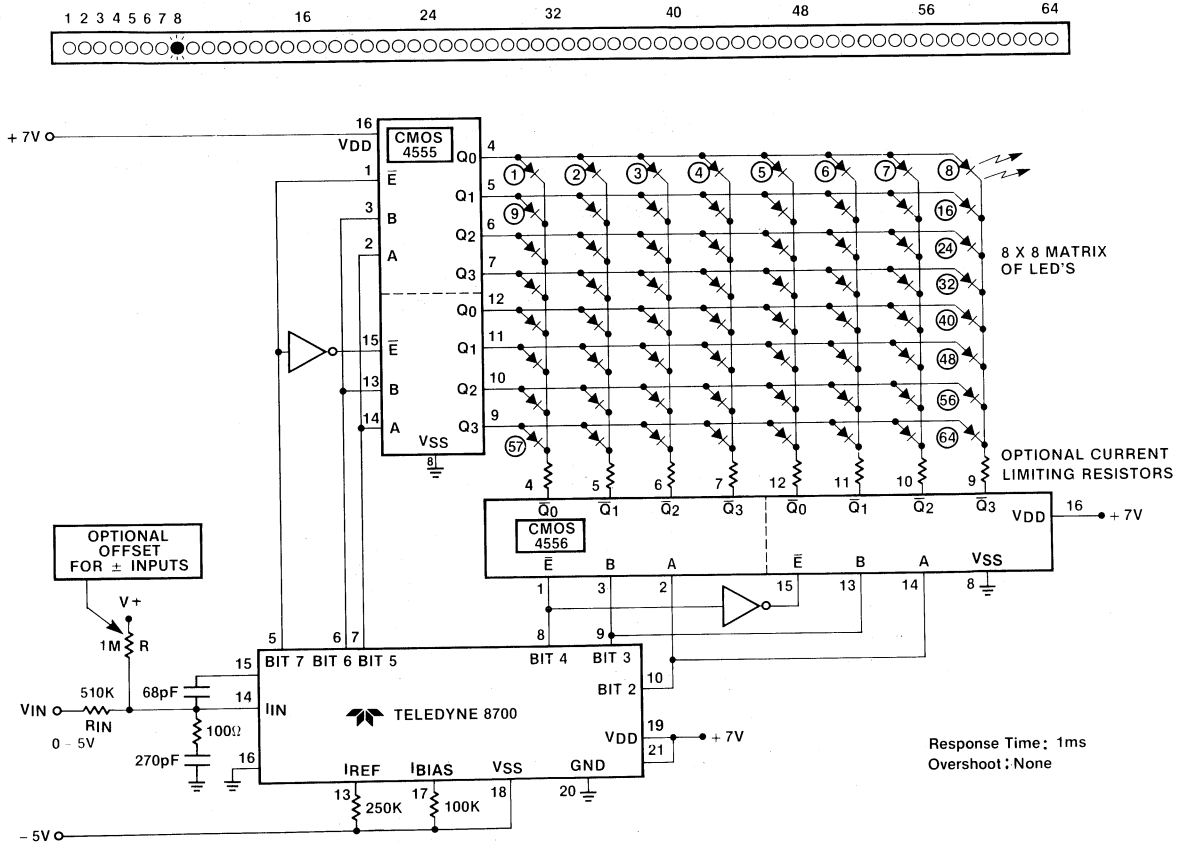
Figure 5. Significant Change Interrupt for 8700 Input Port

TELEDYNE SEMICONDUCTOR

Application Note 9
Applications of the TSC8700 Series CMOS A/D Converters

By Michael O. Paiva & John Blake

LED PANEL METER

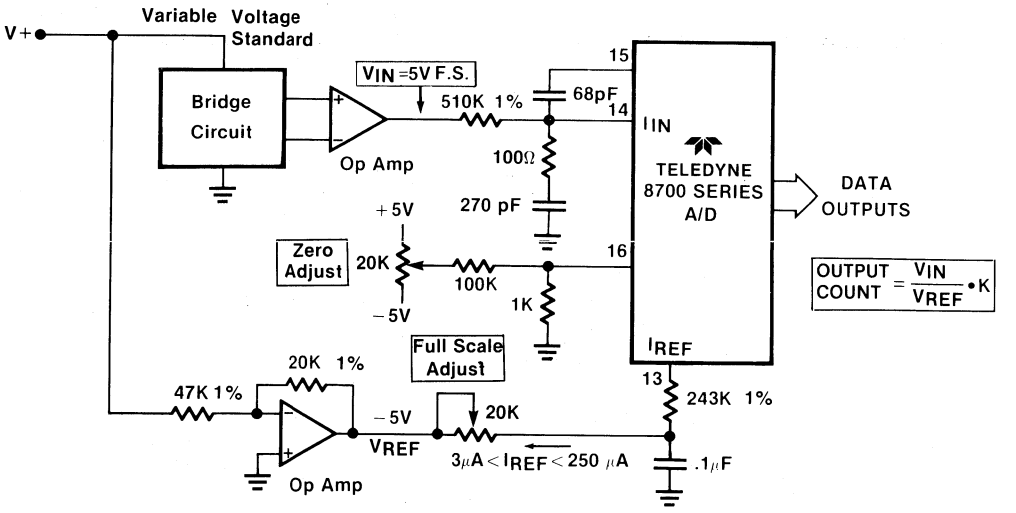


15

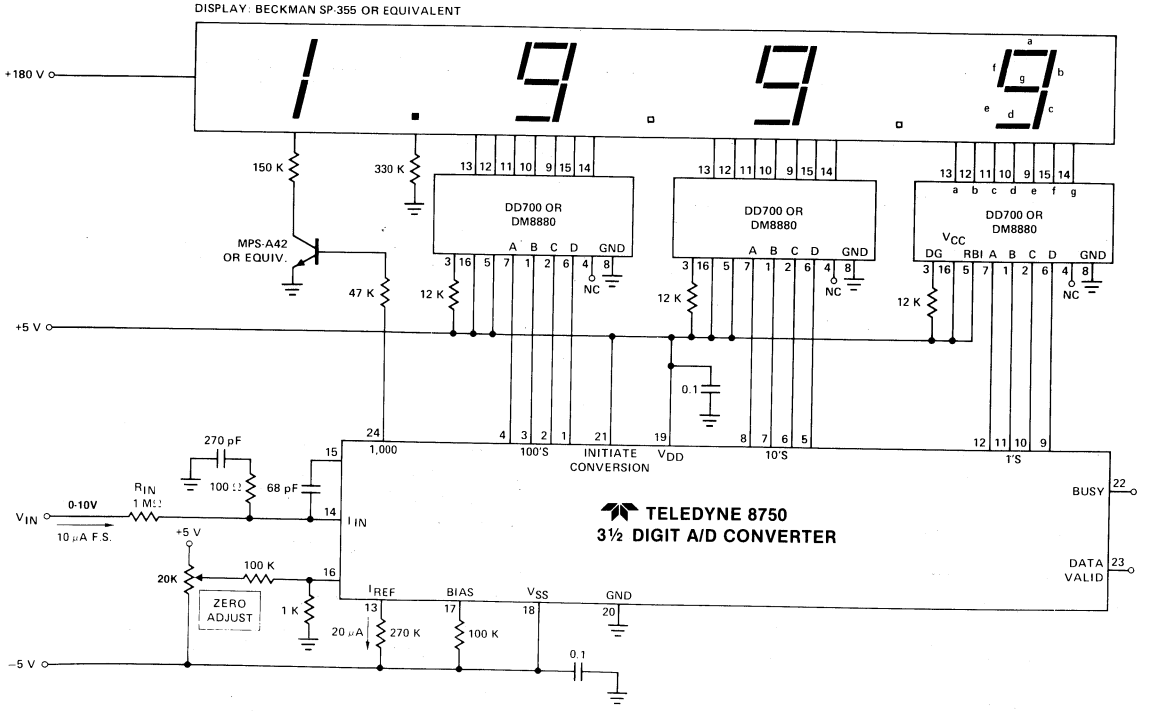
INDEX

LED Panel Meter
Ratiometric Applications
3½ Digit A/D With Gas Discharge Display
Overrange/Underrange Indicator
Autoranging
Dual 3½ Digit LED Display
Analog Peak Detector
8-Channel Data Acquisition System
16-Channel Data Acquisition System
PC Board for 1, 8, or 16-Channel Data Acquisition System
16-Channel Data Acquisition System Pin Out Data
PC Board Assembly Information
Parts List for 16-Channel Data Acquisition System
Design Information
Typical Performance Curves
Negative Supply Generator
8700 Series Connection Diagram

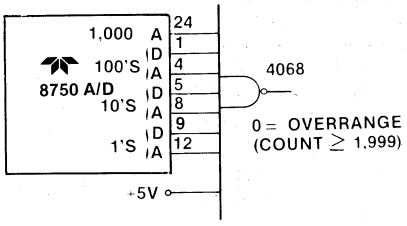
RATIOMETRIC APPLICATIONS



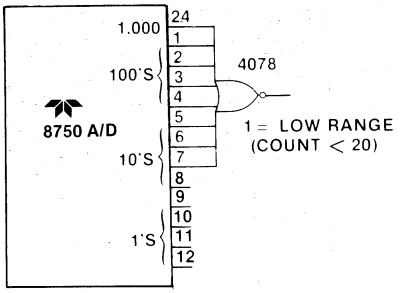
3½ DIGIT A/D WITH GAS DISCHARGE DISPLAY



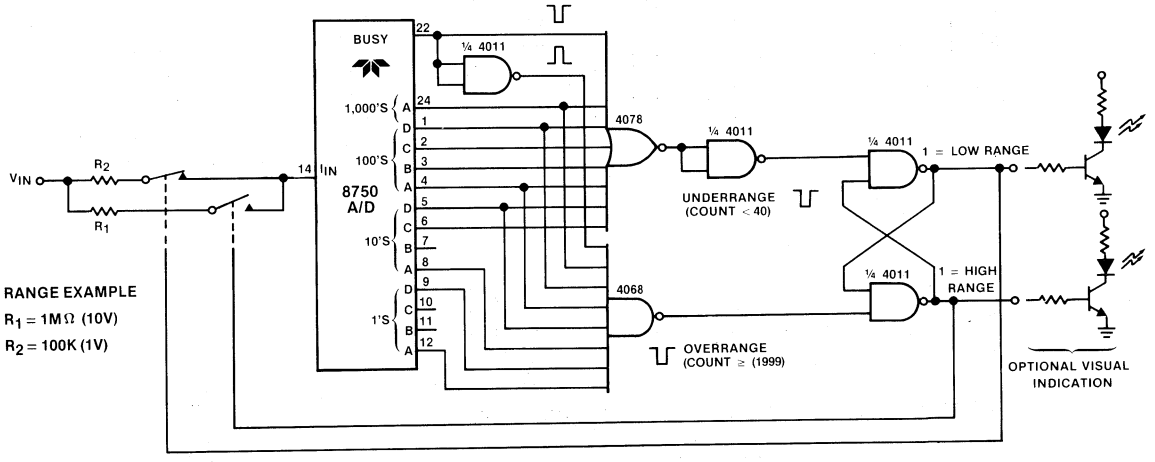
OVERRANGE INDICATOR



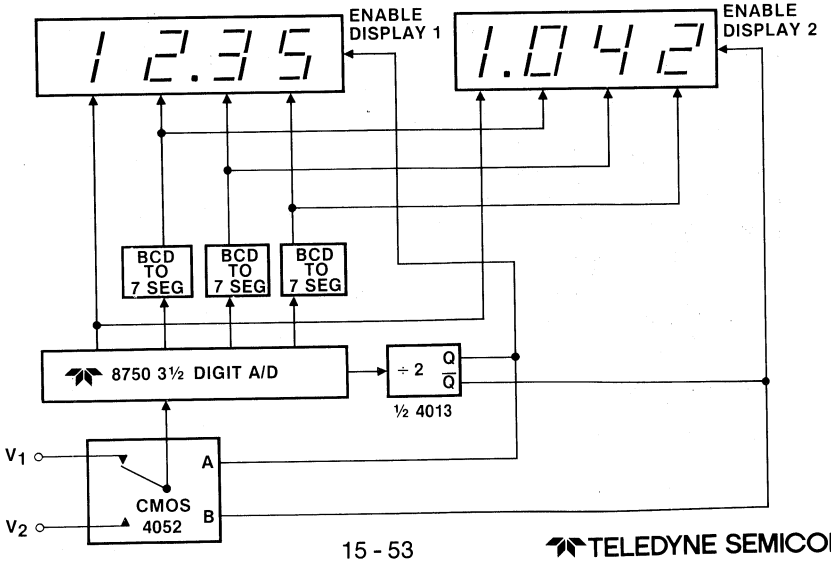
UNDERRANGE INDICATOR



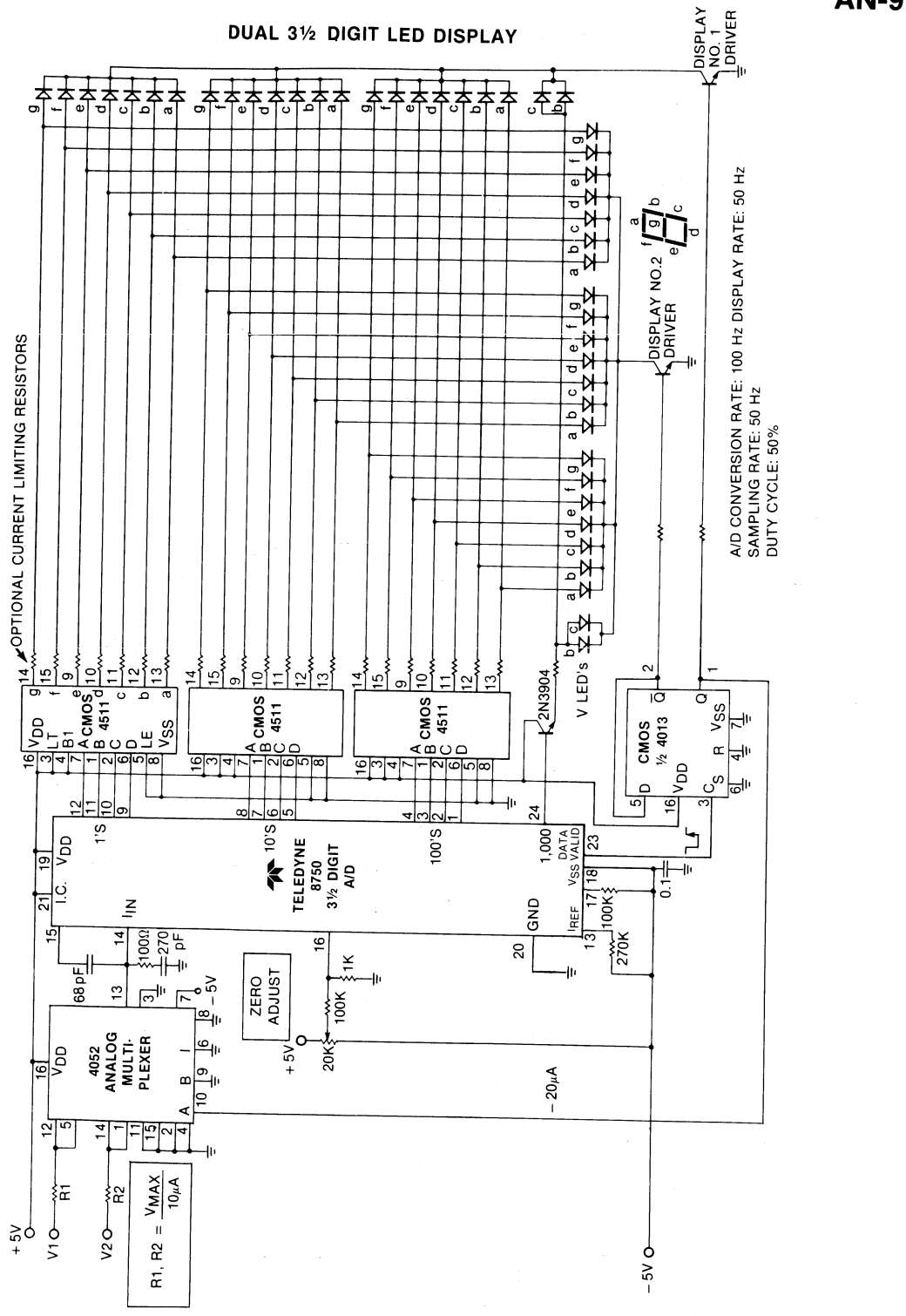
A/D WITH TWO STEP AUTORANGE



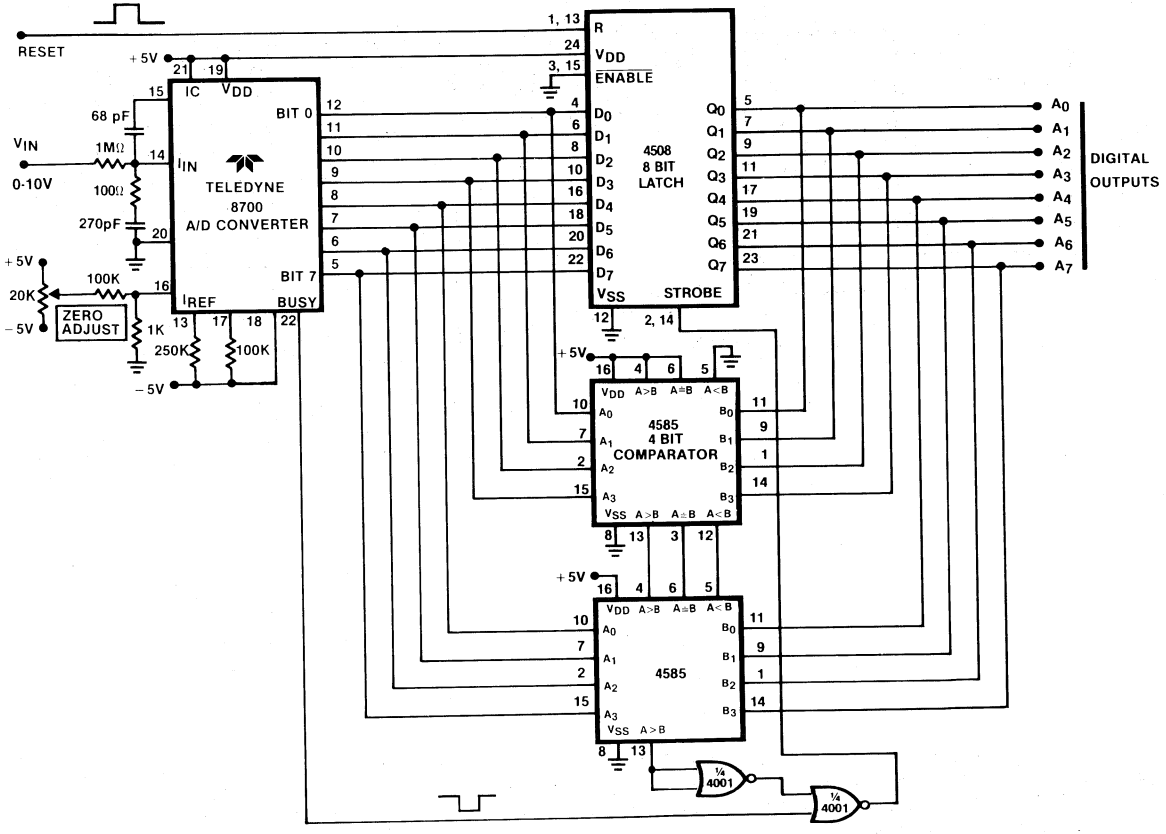
DUAL 3½ DIGIT LED DISPLAY



DUAL 3½ DIGIT LED DISPLAY



ANALOG PEAK DETECTOR WITH DIGITAL HOLD

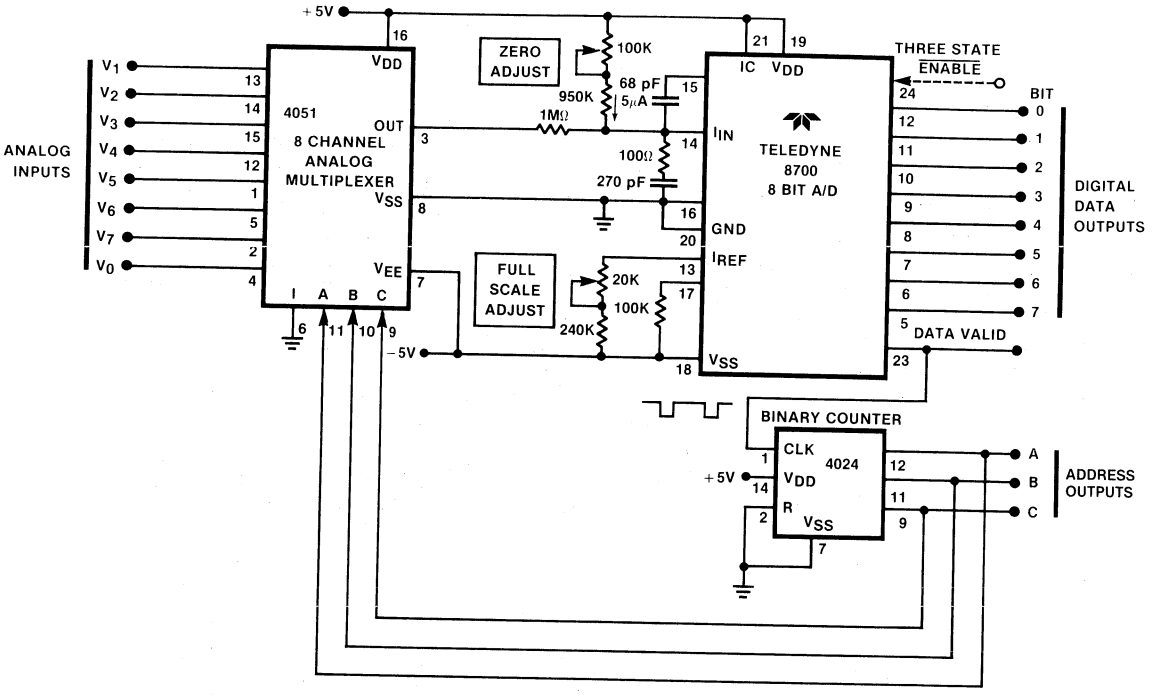


Analog peak detection is accomplished by repeatedly measuring the input signal with an A/D converter and comparing the current reading with the previous reading. If the current reading is larger than the previous, the current reading is stored in the latch and becomes the new peak value. Since the peak is stored in a CMOS latch, the peak can be stored indefinitely.

The TELEDYNE 8700 A/D converter measures the analog input at a 1 KHz rate and computes the binary value of the input. After each 1ms measurement, the binary value is ched in the output of the A/D. This value is then presented to both the 4585 comparators and the 4508 8-bit latch. If the A/D's value is greater than that of the 4508 memory, pin 13 (A > B) of the 4585 goes high. This allows the strobe pulse to go through the 4001 NOR gate to the 4508 memory. The new value is then stored and becomes the reference for subsequent readings. Each time the A/D has a value greater than that stored in the latch, the latch is updated with the larger peak. The system is reset by pulsing the 4508 reset pin high, causing the output to go to 0000 0000.

This system uses an 8-bit A/D to give 0.4% resolution. If greater resolution is required, the 8700 can be replaced by the 8701 (10-bit) for 0.1% resolution or the 8702 (12-bit) for 0.025% resolution. Since this will require 10 or 12 bits to be compared instead of 8, the memory and comparator need to be expanded by adding one additional 4508 and one 4585.

8—CHANNEL DATA ACQUISITION SYSTEM



A low-cost data acquisition system with 8 inputs and 8 bits (0.4%) of resolution at the ouput can be built by using the TELEDYNE 8700 CMOS A/D converter and adding the 4051 8 channel CMOS multiplexer and the 4024 binary counter.

Each input is measured for 1ms, then the digital value is placed in the output latch and remains for 1ms while the next input is being measured. After each 1ms measurement (conversion), the data valid line goes low for 5μs to indicate that the output latch is being updated. (The data must not be read during this period.) The negative edge of the data valid pulse is used to advance the binary counter by one. So after each conversion the 4051, via the 4024, automatically advances to the next input. The sampling sequence is therefore V1, V2,...V7, V0 and then back to V1. The 8700 resets itself for 2.5μs after the data valid pulse so the analog switch has a total of 7.5μs to settle down. This is more than adequate to assure that the A/D will ignore any switching transients.

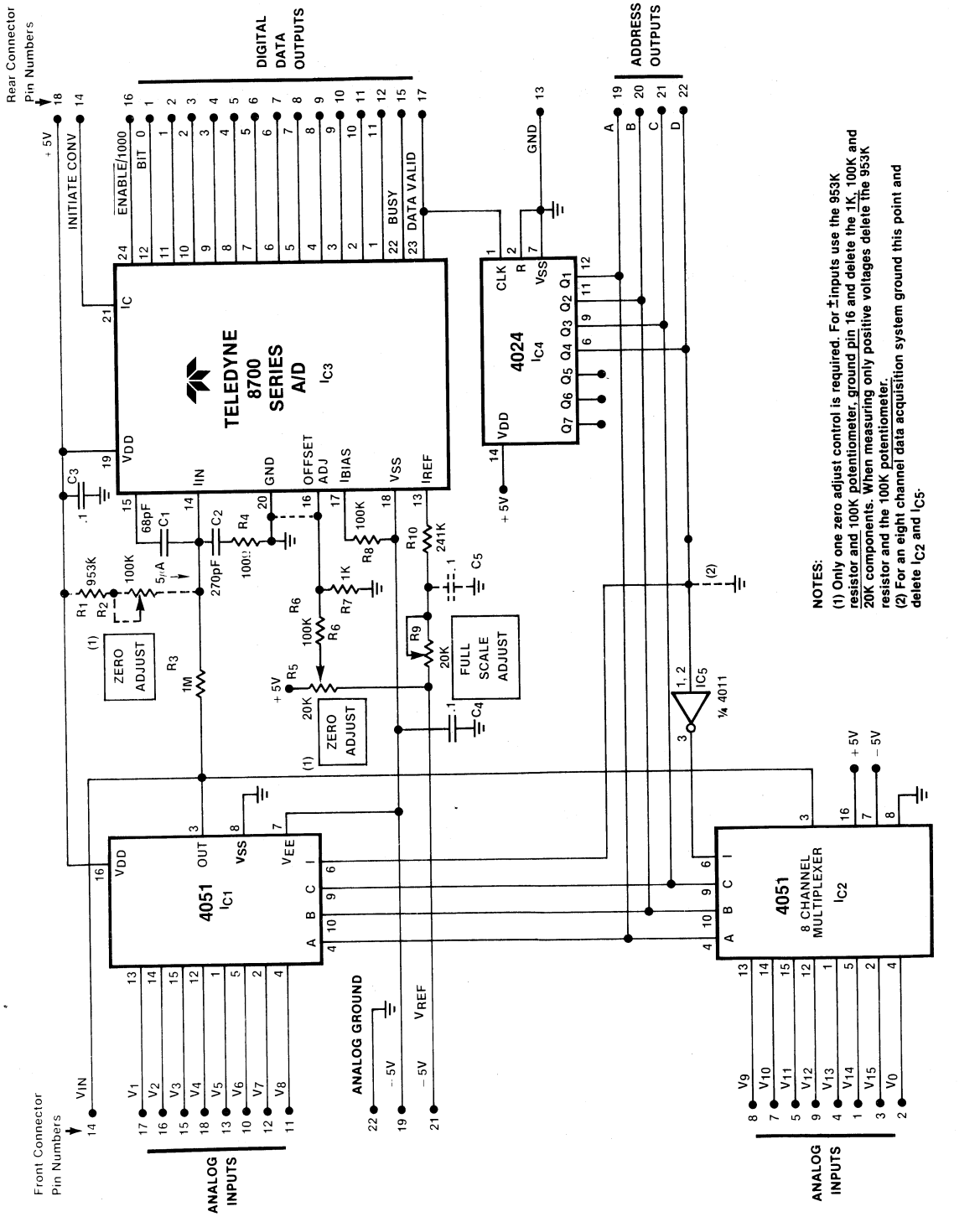
For the circuit shown, the input voltage range is limited by the 4051 to ± 5 volts (V_{DD}, V_{EE}). If more input voltage range is needed, then V_{SS} and V_{EE} can be increased or the 1MΩ resistor can be replaced by individual resistors in front of each analog input. The exact value of each resistor is determined by dividing the maximum input voltage by 5μA. ($R_{IN} = V_{max} \div 5\mu A$).

The 950K and 100K resistor are used to provide an offset current of 5μA, allowing the analog input voltage to be negative as well as positive. If the input voltage does not go negative, then these two resistors can be deleted.

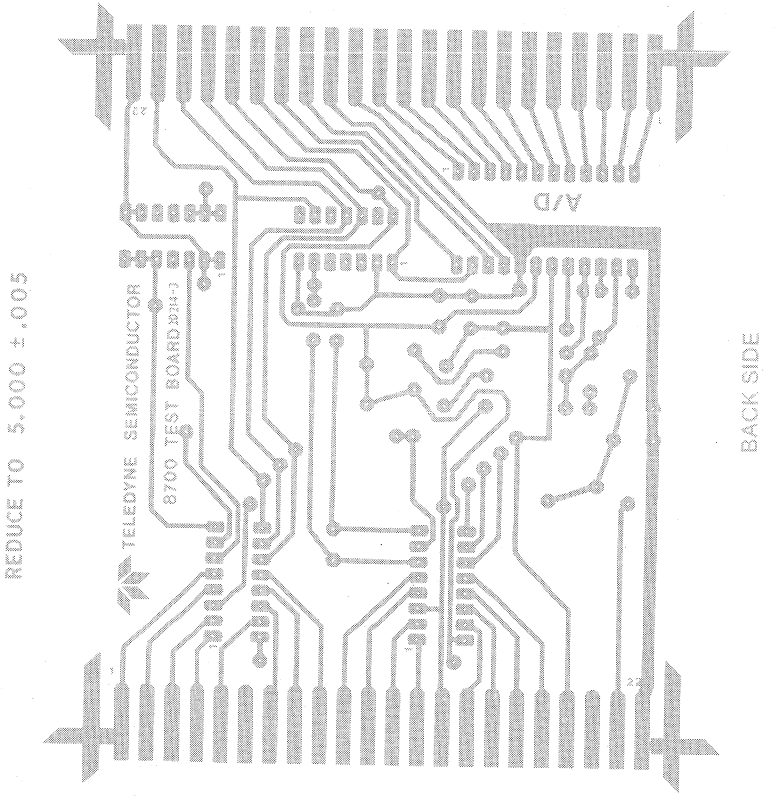
By adding additional 4051's, the number of analog inputs can be increased in multiples of eight. The additional binary outputs of the 4024 are then simply decoded to control the inhibit (1) input of each 4051.

If three-state outputs are needed for interfacing to a data buss, then the 8700 can be replaced by the 8703. The 8703 is identical to the 8700 except that the digital data outputs are three-state outputs controlled by pin 24 ($\overline{\text{ENABLE}}$).

16—CHANNEL DATA ACQUISITION SYSTEM

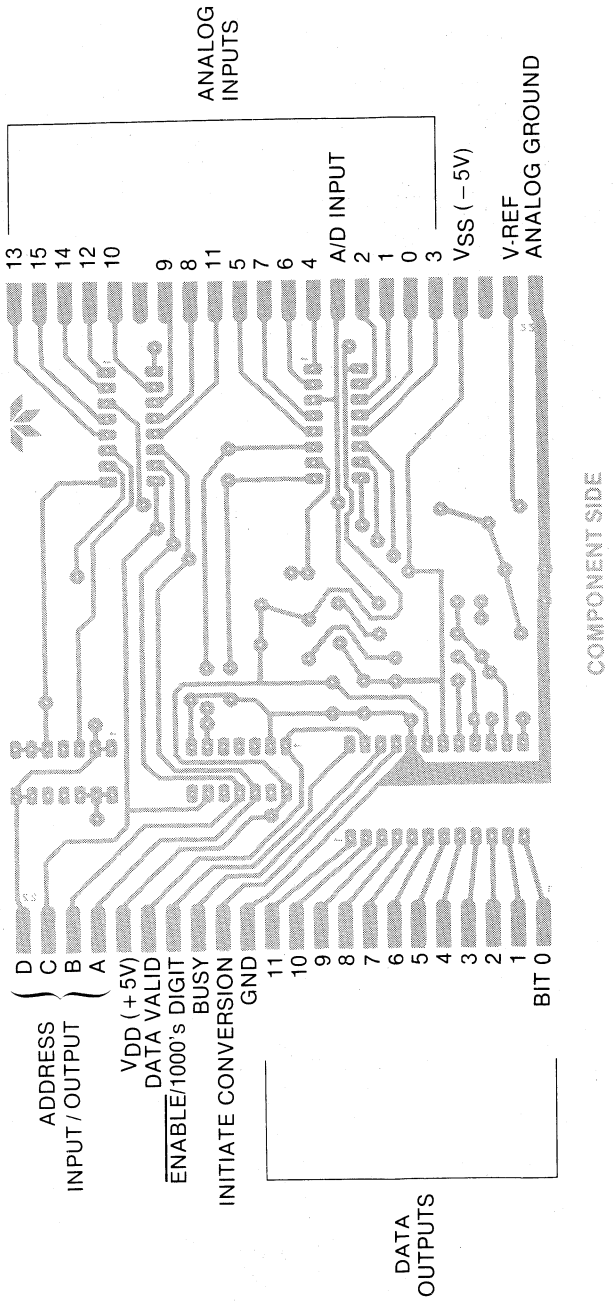


8700 PC BOARD METAL PATTERN
PC BOARD FOR 1, 8, 16 CHANNEL DATA ACQUISITION SYSTEM

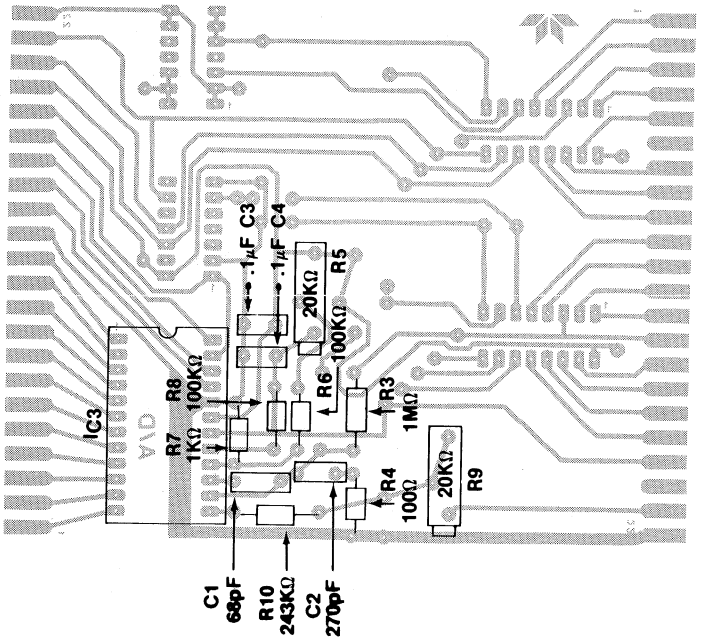


Note: PC board can be ordered from Teledyne as part #8700PC.

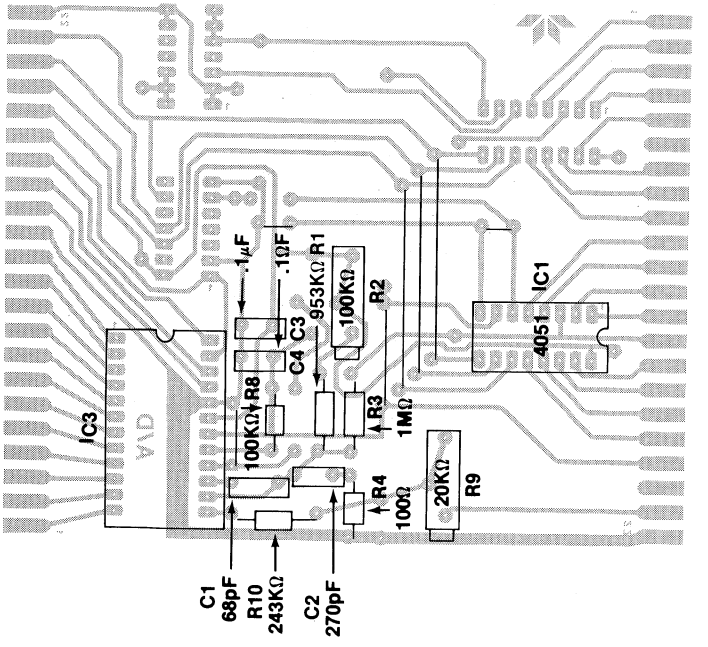
PIN-OUT DATA FOR 16 CHANNEL DATA ACQUISITION SYSTEM



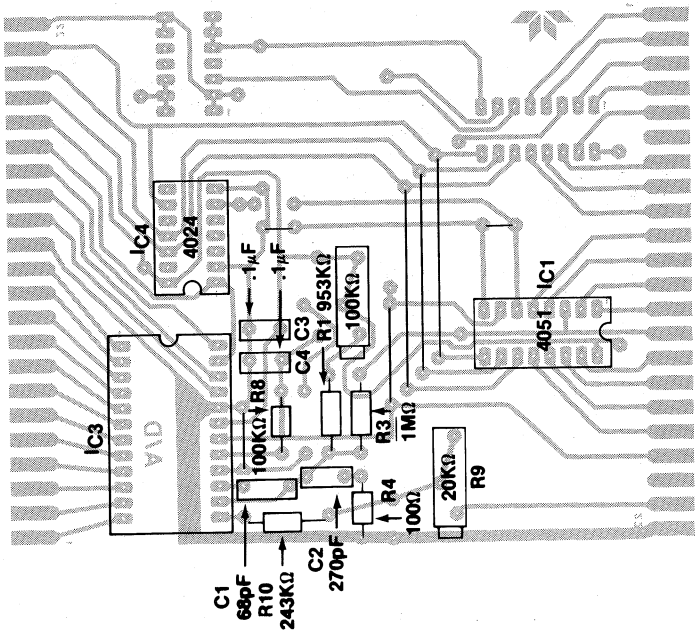
STANDARD TEST CIRCUIT



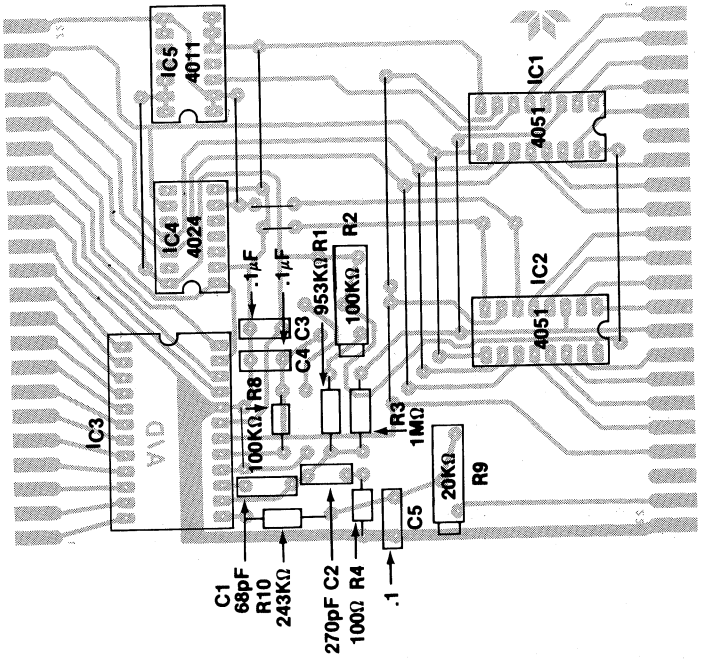
A/D WITH 8-CHANNEL ANALOG INPUT SELECTOR



8-CHANNEL DATA ACQUISITION SYSTEM



16-CHANNEL DATA ACQUISITION SYSTEM



15

PARTS LIST

16 CHANNEL DATA ACQUISITION SYSTEM

Ref #	Part Number	Description
IC1, IC2	4051	CMOS — 8 CHANNEL ANALOG SWITCH
IC3	8700 TYPE	CMOS — TELEDYNE A/D CONVERTER
IC4	4024	CMOS — 7 bit BINARY COUNTER
IC5	4011	CMOS — QUAD 2-INPUT NAND GATE
C1	68pF ± 10%	Low leakage mica, ceramic, etc.
C2	270pF ± 20%	Ceramic, mica, etc.
C3, C4, C5	0.1μF ± 20%	Ceramic, mylar, electrolytic, tantalum, etc.
R1	* 953K ± 1%	Carbon, carbon film, metal film, etc.
R2	* 100K ± 10%	Trimmer resistor
R3	* 1MΩ ± 1%	Carbon, carbon film, metal film, etc.
R4	100Ω ± 10%	Carbon resistor
R5	20K ± 10%	Trimmer resistor
R6	100K ± 5%	Carbon resistor
R7	1K ± 5%	Carbon resistor
R8	100K ± 10%	Carbon resistor
R9	* 20K ± 10%	Trimmer resistor
R10	* 243K ± 1%	Carbon, carbon film, metal film, etc.

★ The stability of these components directly affects the accuracy of the overall system. Choose components whose stability is consistent with the accuracy and temperature range required. For example, if an 8-bit A/D is used at a constant temperature, then 5% carbon resistors may be adequate since an 8-bit A/D's resolution is only 0.4%. However, if a 12-bit A/D (0.025% resolution) is to be used over the -55°C to + 125°C temperature range, then these components will be very critical and should have a stability of 5 to 15 ppm for fixed resistors and 25 to 50 ppm for variable resistors.

The following parts list of possible suppliers is intended to be of assistance in putting a converter design into production. It should not be interpreted as a comprehensive list of suppliers, nor does it constitute an endorsement by Teledyne Semiconductor.

TYPICAL COMPONENT SOURCES FOR PRECISION APPLICATION

A. Precision fixed resistors

Value	Tol.	Typical Source	Type	Temp. Coeff./°C
243K	± 1%	Mepco/Electra	5033R	± 5ppm/ ± 25ppm/ ± 100ppm
953K	± 1%	Mepco/Electra	5033R	± 5ppm/ ± 25ppm/ ± 100ppm
1MΩ	± 1%	Mepco/Electra	5033R	± 5ppm/ ± 25ppm/ ± 100ppm

B. Variable resistors

20K/100K	± 10%	Mepco/Electra	8035	± 100ppm
20K/100K	± 10%	Spectrol	43P	± 100ppm

C. Capacitors

68pF	± 10%	Union Carbide	C114K680K1X1CA	± 800ppm
68pF	± 10%	Union Carbide	C114G680K565CM	± 30ppm
68pF	± 5%	Corning	CY06C680G	± 25ppm

DESIGN INFORMATION

1. AVOID INTRODUCING ERRORS:

Proper design procedures are necessary to obtain best accuracy from 8700 series converters.

a. Do not route logic signals under the 8700 or near any of the three analog terminals I_{IN}, I_{REF}, and Zero Adjust (pins 13, 14, 15, 16).

b. Plan your grounding. Keep the analog ground isolated from the logic ground by making the two electrically common only at the system ground.

c. Filter the supply voltages by using bypass capacitors of value 0.1μF or greater connected in shunt between the supply line and the logic ground (pin 20). Locate the capacitors as close as to the 8700 as practical.

d. Provide a reference as stable as the conversion accuracy you expect. Remember:

$$\text{DIGITAL COUNTS} = \frac{I_{IN}}{I_{REF}} \bullet A = \frac{V_{IN} \div R_{IN}}{V_{REF} \div R_{REF}} \bullet A$$

The conversion accuracy is a direct function of the V_{REF}. In terms of V_{REF} voltage regulation, the 8-bit requires ±.04%, the 10-bit, ±.01%, the 12-bit, ±.0025%, and the 3½ digit BCD, ±.005%,to introduce less than 1/10 LSB error.

e. Choose a full scale voltage range as large as possible; this will minimize the effect of zero drift and input noise. For example, a 50μV zero drift or noise voltage on the 8701 (10-bit) will produce a ± ½ LSB error at 500mV full scale, but only ± 1/40 LSB at 10V full scale.

2. OTHER SUGGESTIONS FOR IMPROVING PERFORMANCE:

a. For C_{INT}, virtually any type of non-polarized 68pF ± 10% is acceptable. Locate as near to the converter as possible and away from noisy lines.

b. Locate R_{DAMP} and C_{DAMP} as near the converter as possible and away from noisy lines. The value of R_{DAMP} = 100Ω and C_{DAMP} = 270pF are nominal; these two elements stabilize the input op amp to prevent oscillations.

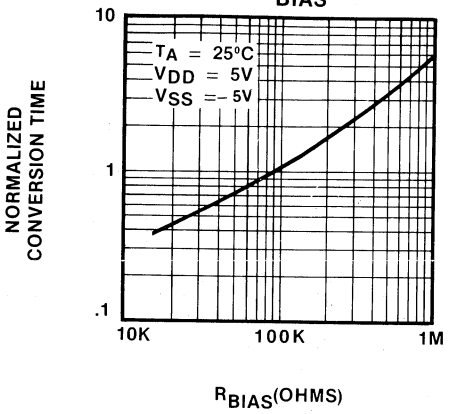
3. CAUTION: WHEN USING ZENERS, OP AMPS AND VOLTAGE REGULATORS:

These devices are often used as input amplifiers, voltage references and power supplies for A/D converters. It is worth noting that these devices can generate quite a bit of "High Frequency" noise. Normally, this noise does not interfere with the operation of the A/D converter. However, excessive noise from zeners, used as voltage references for example, have been found to be the cause of strange counting sequences and non-linear A/D operation. It should therefore be standard practice to bypass all zeners and voltage regulators with at least 0.1μF capacitors. (If the zener is exceptionally noisy, 1 to 10μF capacitors may be required. Remember that zeners are often used as white noise sources in noise generators.)

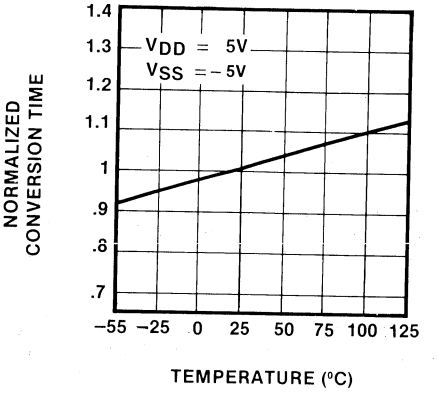
If erratic operation is still observed, then either the op amp's feedback resistor or the output should be bypassed. Note also that the noise level of zeners, op amps and voltage regulators varies from lot to lot and especially from one manufacturer to another. Bypassing these devices during the design stage will prevent the noise level variation from becoming a possible production problem.

TYPICAL PERFORMANCE CURVES

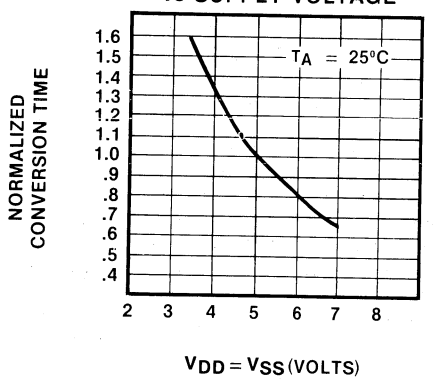
CONVERSION TIME vs R_{BIAS}



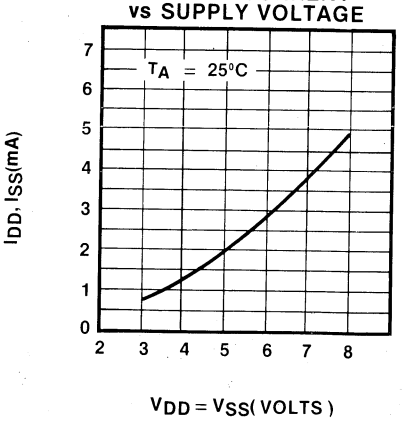
CONVERSION TIME vs TEMPERATURE



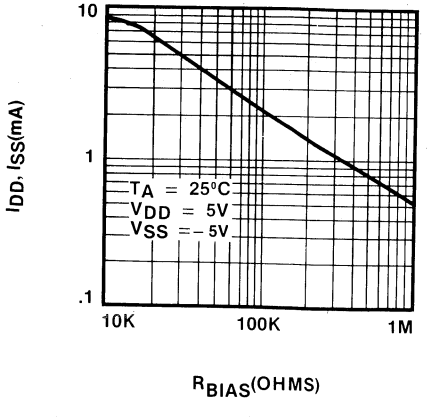
CONVERSION TIME vs SUPPLY VOLTAGE



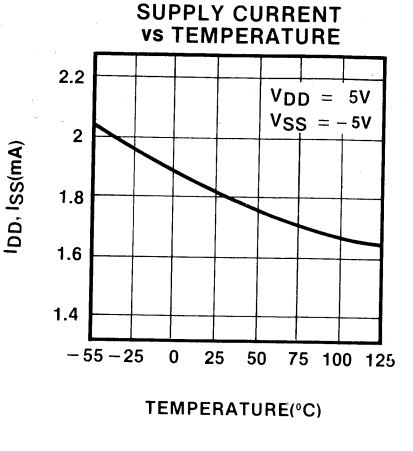
SUPPLY CURRENT vs SUPPLY VOLTAGE



SUPPLY CURRENT vs R_{BIAS}

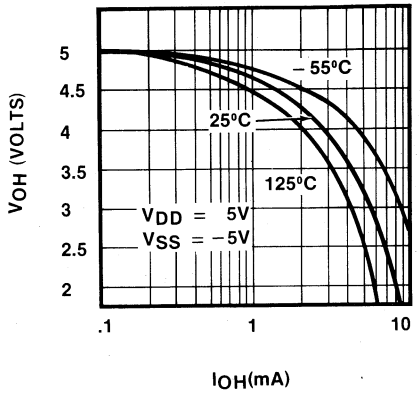


SUPPLY CURRENT vs TEMPERATURE

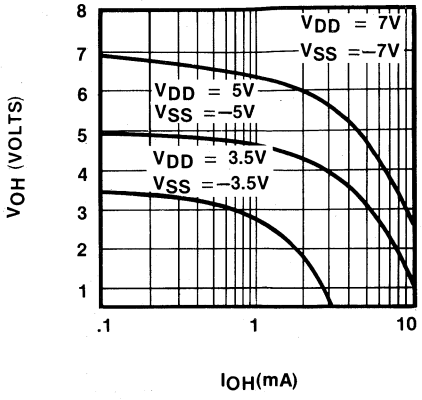


TYPICAL PERFORMANCE CURVES

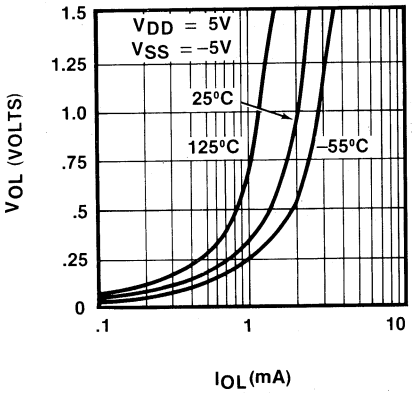
OUTPUT SOURCE CURRENT vs TEMPERATURE



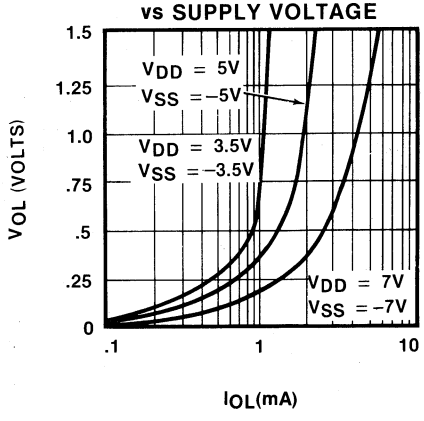
OUTPUT SOURCE CURRENT vs SUPPLY VOLTAGE



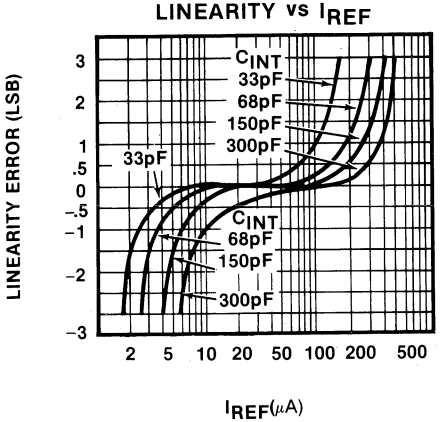
OUTPUT SINK CURRENT vs TEMPERATURE



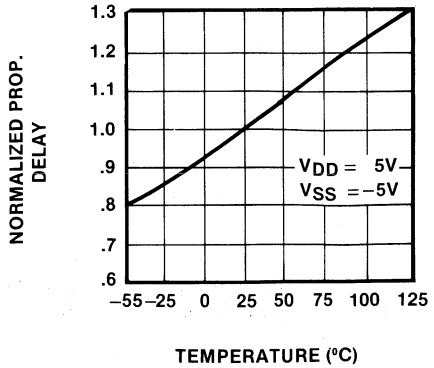
OUTPUT SINK CURRENT vs SUPPLY VOLTAGE



LINEARITY vs I_{REF}

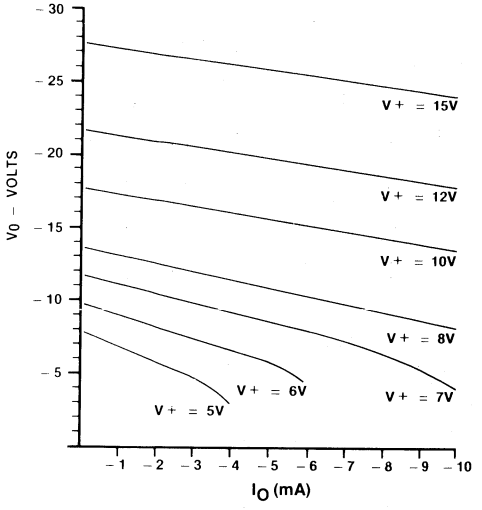


TRI-STATE PROPAGATION DELAY

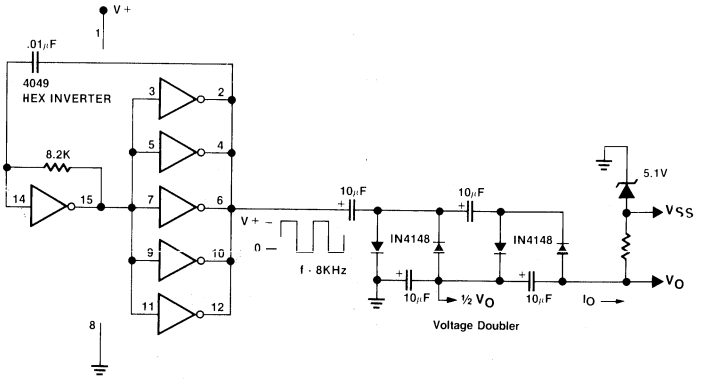


15

NEGATIVE SUPPLY GENERATOR



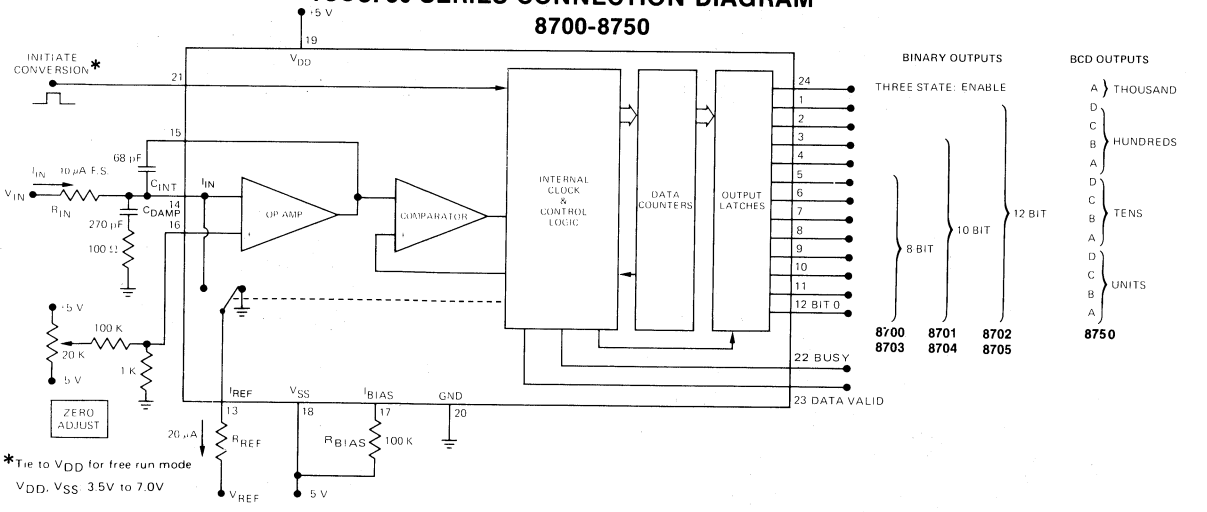
OUTPUT VOLTAGE VS OUTPUT CURRENT



A negative voltage for V_{SS} and V_{REF} can be generated from the positive supply by using a hex inverter as a free running oscillator to drive a voltage doubler. The five inverters are paralleled to provide a low output impedance. Since the 4049 is a standard 4000 CMOS part, the circuit can be operated from 3 to 15 volts. 10μF capacitors were used in order to minimize output ripple at low V+ voltages.

When higher input voltages (V+) are available the 10μF capacitors can be lowered to 1 or 0.1μF depending on the output loading. If this circuit generates more voltage than is needed, one half of the diodes and capacitors can be eliminated to reduce cost. The output voltage will then be one half of that shown in the graph and is available on the negative side of the 10μF capacitor connected to ground.

TSC8700 SERIES CONNECTION DIAGRAM
8700-8750

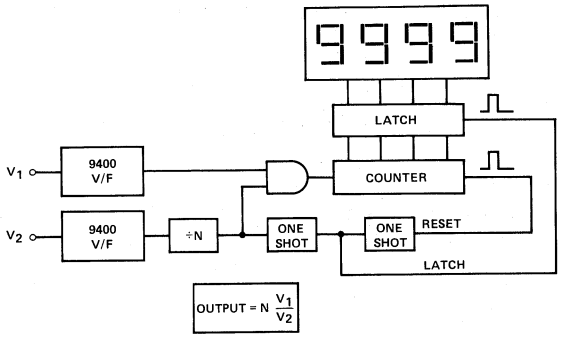


The Teledyne Semiconductor 8700 series are integrating A/D converters. These are available with 8-, 10-, or 12-bit resolutions, with or without three-state outputs, and also in a 3½ digit parallel BDC format. Individual data sheets are available from Teledyne Semiconductor.

Application Note 10
Applications of the TSC9400 Voltage to Frequency Frequency to Voltage Converter

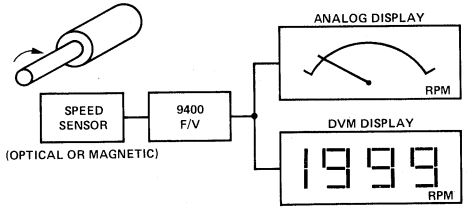
By Michael O. Paiva

RATIOMETRIC MEASUREMENT (ANALOG DIVISION)



One of the most difficult circuits to build is one which will divide one analog signal by another. Two V/F converters can do such division with ease. The numerator is counted directly as a signal, while the denominator forms the time base.

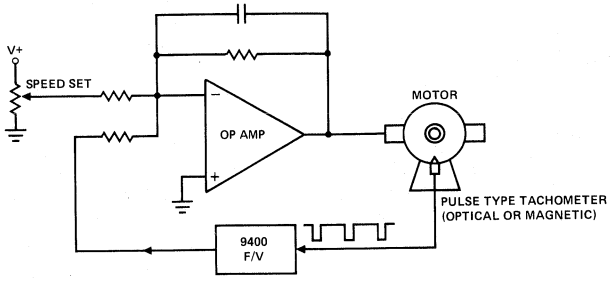
RPM/SPEED INDICATOR



Flow rates and revolutions per second are nothing more than frequency signals since they measure the number of events per time period. Optical and magnetic sensors will convert these flows and revolutions into a digital signal which in turn can be converted to a proportional voltage by the use of an F/V converter. A simple voltmeter will then give a visual indication of the speed.

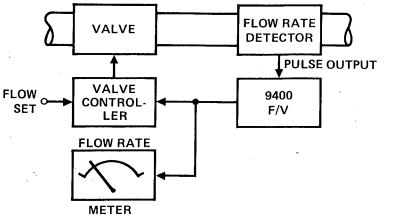
15

MOTOR SPEED CONTROL



The motor's speed is measured with the F/V, which converts RPM into a proportional voltage. This voltage is used in a negative feedback system to maintain the motor at the controlled setting.

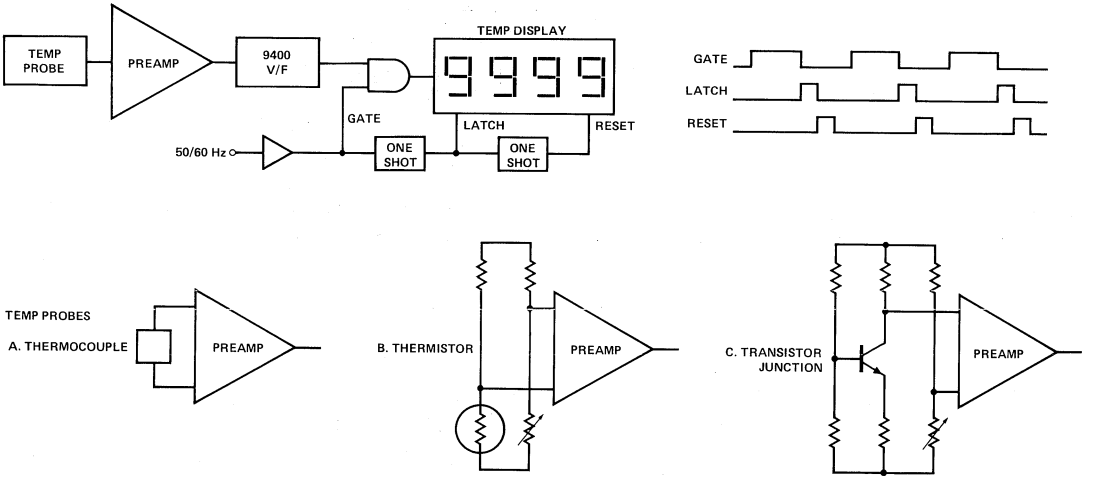
PROPORTIONAL FLOW RATE CONTROLLER



A 9400 F/V can be used to regulate the amount of liquid or gas flowing through a pipeline.

The flow rate detector generates a pulse train whose frequency is proportional to the rate of flow through it. The F/V converts this frequency to a proportional analog voltage which is used to drive the valve controller. The valve controller regulates the valve so that the flow is steady even though pipeline pressure goes up and down. A voltmeter connected to the F/V output will indicate the actual instantaneous flow rate.

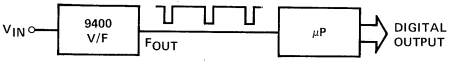
TEMPERATURE METER



A temperature meter using the voltage output of a probe, such as one of the three shown, can be economically and straightforwardly implemented with the 9400 V/F. The V/F output is simply counted to display the temperature.

For long distance data transmission, the 9400 can be used to modulate an RF transmitter.

A/D CONVERSION WITH A MICROPROCESSOR



There are two schemes that can be utilized to accomplish A/D conversion with a microprocessor:

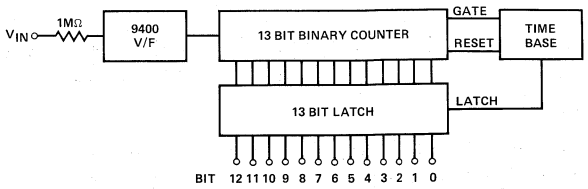
1. Depending on the number of digits of resolution required, V_{OUT} is measured by counting the V/F frequency for 1ms, 10ms, 100ms, or 1 second. The final count is then directly proportional to the input voltage. (The microprocessor provides the time base.)

2. V_{IN} is measured by determining the time between two pulses (negative edges). The F_{OUT} signal is used as a gate for counting the microprocessor's clock. The final count will then be inversely proportional to the input signal.

   By taking the one's complement (changing 1's to 0's and 0's to 1's) of the final binary count a value directly proportional to the input will result.

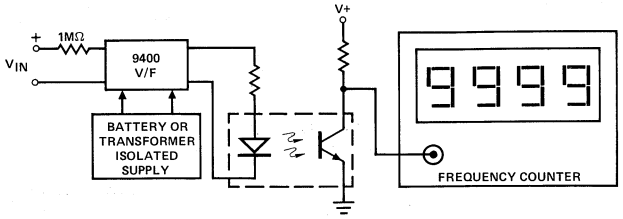
   This technique will give a faster conversion time when resolution is very important, but dynamic range is limited.

13 BIT A/D CONVERTER



A 13 bit binary or 4 digit BCD A/D converter can be built by combining the 9400 V/F with a counter, latch and time base. When the V/F is set up for 10KHz full scale a 1 second time base will provide one conversion per second.

4 DIGIT VOLTMETER W/OPTO-ISOLATED INPUT

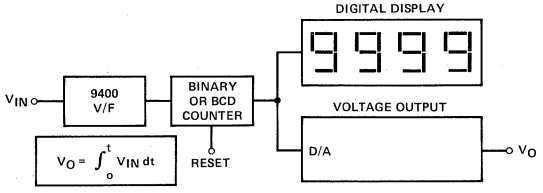


The use of a frequency counter will give a display of the V/F's frequency which is directly proportional to the input voltage.

When the V/F is running at 10KHz full scale, a 0.1 second time base will give 3 digit resolution with 10 readings per second.

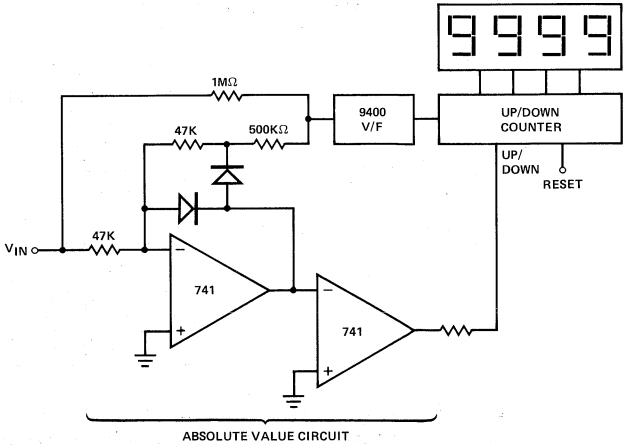
The opto isolator is used for transmitting the frequency so that there is no DC path to the frequency counter. This is especially handy in medical applications where a voltage probe should not be directly connected to a human body.

LONG TERM INTEGRATOR WITH INFINITE HOLD

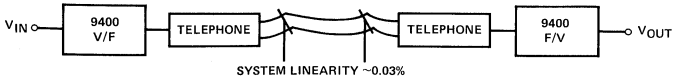


This system will integrate an input signal for minutes or days and hold its output indefinitely. The data is held in a digital counter and will stay there until the counter is reset. Typical applications involve controlling the amount of surface metal deposited in a plating system or how much charge a battery has taken on.

LONG TERM INTEGRATOR FOR BIPOLAR (+/–) SIGNALS



When the input signal is negative as well as positive there needs to be a way of generating "negative" frequencies. An absolute value circuit accomplishes this by giving the V/F a positive voltage only; and also telling the counter to count up for a positive voltage and to count down for a negative voltage.

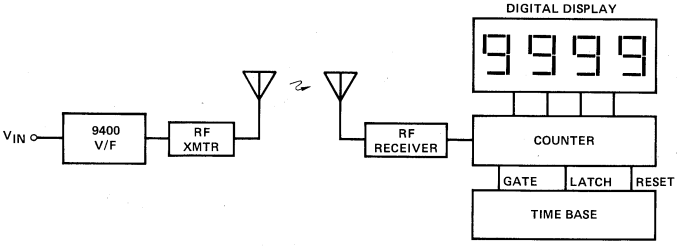


The 9400's square wave output is ideal for transmitting analog data over telephone lines. A square wave is actually preferred over a pulse waveform for data transmission since the square wave takes up less frequency spectrum than a pulse waveform.

The square wave's spectrum can be further reduced by use of low pass filters.

At the other end of the telephone line a 9400 F/V converts the frequency signal back into a voltage output which is linearly proportional to the original input voltage.

TELEMETRY

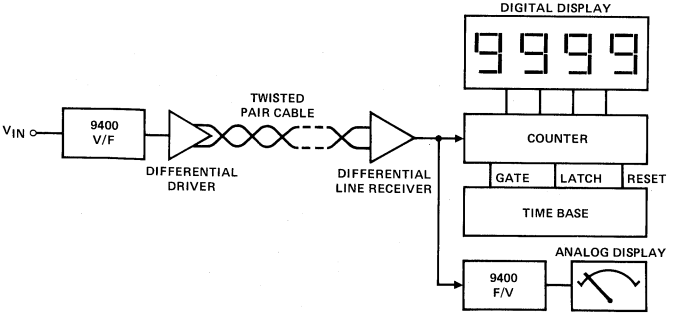


In a telemetry system the 9400 converts the analog input (V_{IN}) into frequencies (10Hz to 100KHz) which can be used to modulate an RF transmitter.

At the other end a receiver picks up the RF signal and modulates it back into the 10Hz to 100KHz spectrum. A frequency counter connected to this signal will then give a count which is linearly proportional to the original analog voltage (V_{IN}).

If a linearly proportional analog output voltage is required, then the counter can be replaced by a 9400 used in the F/V mode.

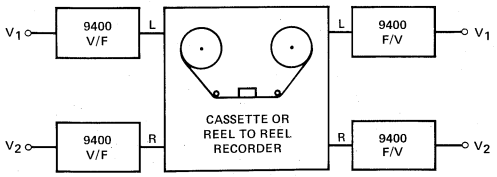
HIGH NOISE IMMUNITY DATA TRANSMISSION



When transmitting analog data over long distances it is advantageous to convert the analog signal into a digital signal which will be less susceptible to noise pick-up.

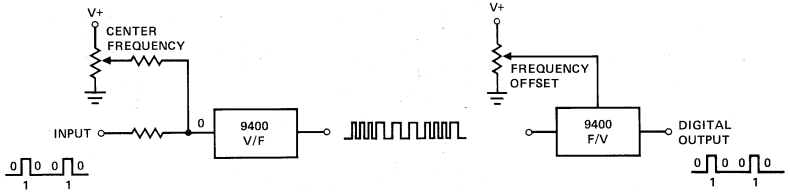
In the above system the 9400 converts the input voltage into either a pulse or square wave which is transmitted on a pair of wires by use of a line driver and receiver. At the other end the original voltage (V_{IN}) can be digitally displayed on a frequency counter or converted back to an analog voltage by use of a 9400 F/V converter.

DC RESPONSE DATA RECORDING SYSTEM



Low frequency analog data (DC to 10KHz) can be recorded anywhere, stored and then reproduced. By varying the playback speed, the frequency spectrum of the original data can be shifted up or down.

FSK GENERATION AND DECODING



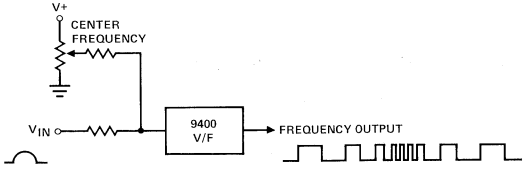
Frequency shift keying (FSK) is a simple means of transmitting digital data over a signal path (two wires, telephone lines, AM transmitters or FM transmitters).

Typically only two frequencies are transmitted. One corresponds to a logical "0" while the other corresponds to a logical "1".

A 9400 V/F will generate these two frequencies when connected as shown above. The potentiometer sets the V/F to the lower frequency. The digital input will then determine which frequency is selected. A "0" selects the lower frequency while a "1" selects the upper frequency.

The digital frequency signal is converted back into a digital format by a 9400 used in the F/V mode.

ULTRA LINEAR FREQUENCY MODULATOR

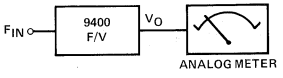


Since the 9400 is a very linear V/F converter an FM modulator is very easy to build.

The potentiometer determines the center frequency while V_{IN} will determine the amount of modulation (FM deviation) around the center frequency. V_{IN} can be negative as well as positive.

15

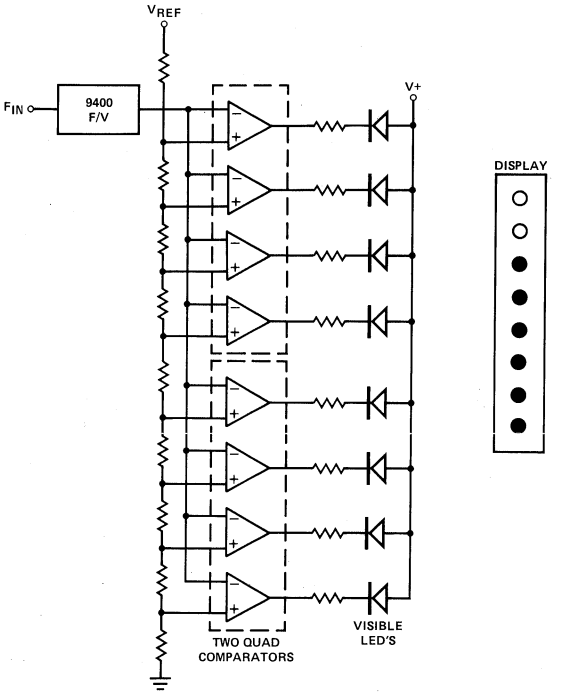
FREQUENCY METER



The 9400 will convert any frequency below 100KHz into an output voltage, which is linearly proportional to the input frequency. The equivalent frequency is then displayed on an analog meter.

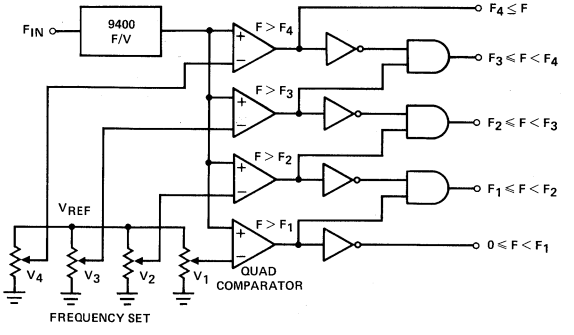
If the incoming frequency is above 100KHz a frequency divider in front of the 9400 can be used to scale the frequency down to the 100KHz region.

TACHOMETER BAR GRAPH DISPLAY



A tachometer can be constructed by using the 9400 in the F/V mode to convert the frequency information (RPM) into a linearly proportional voltage. This voltage is then compared to one of n comparators (8 in this example). When the voltage exceeds the trip point of a comparator the respective LED will light up and continue to stay lit as long as the voltage exceeds the trip point. This will give a bar graph type display with the height of the bar being proportional to RPM.

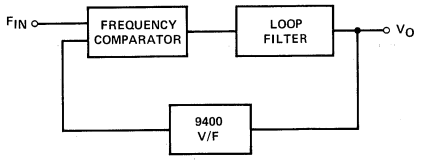
FREQUENCY/TONE DECODER



The frequency or tone to be detected is converted into a proportional analog voltage by the 9400 F/V converter. The quad comparators sense when the voltage (frequency) exceeds any of the four preset frequency limits. A logical "1" at any of the five outputs indicates that the frequency is within those limits.

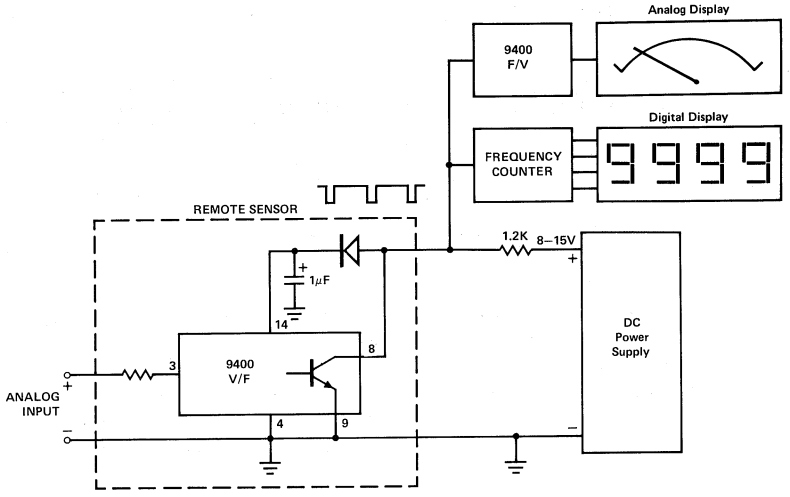
This system is useful for determining which frequency band a signal is in or for remote control where each frequency band corresponds to a different command.

FM DEMODULATION WITH A PHASE LOCKED LOOP



The high linearity of the 9400 (0.01%) is used to greatly improve the performance of a phase locked loop, resulting in very precise tracking of V_O with respect to F_{IN}.

ANALOG DATA TRANSMISSION ON DC SUPPLY LINES (TWO WIRE TRANSMITTER)



By converting an analog voltage to a linearly proportional pulse train of short duration, it is possible to transmit this data on the same wires that are used to energize the V/F converter.

The 9400 V/F shorts out the DC supply for 3μs out of each period. At 100KHz the supply line is down 30% of the 10μs period. As the frequency is lowered the down time decreases so that at 1KHz the line is down only 0.3% of the time.

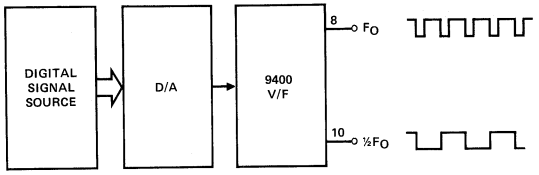
Two precautions are necessary to assure that the system does not stop functioning during the shorting period. At the power supply end a 1.2K resistor limits the current to 10mA on a 15V supply line. This prevents the 9400 from being operated beyond its output rating and at the same time it prevents the supply from being shorted out. At the V/F end a capacitor is used to keep the 9400 energized while the diode keeps the capacitor from being discharged.

Since the 9400 requires only 2mA of current, a 1μF capacitor ensures a stable voltage (the ripple is only 6mV). Since the 3μs pulses appear at the left side of the 1.2K resistor, it is easy to sense the signal here and convert the data back into a recognizable format. A frequency counter connected at this point will directly display the input voltage by counting the frequency.

If an analog output is required, a 9400 in the F/V mode can be used to convert the frequency back into a voltage. The overall linearity is in the order of 0.03%, when both V/F and F/V are used. If only the V/F is used, then 0.01% linearity can easily be achieved.

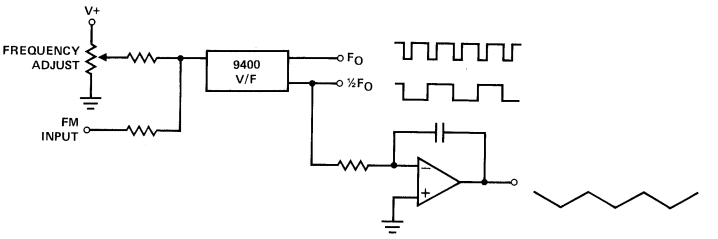
15

DIGITALLY CONTROLLED FREQUENCY SOURCE



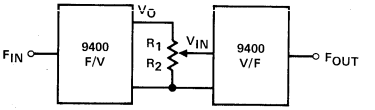
This system generates frequencies which are controlled by a microprocessor counter, register, or by thumb-wheel switches. Applications for such a system include computer controlled test equipment and numerically controlled machine tools.

WIDE FREQUENCY RANGE PULSE GENERATOR



The 9400 V/F is useful in the laboratory as a portable, battery operated low cost frequency source. The 9400 provides both pulse and square wave outputs. By adding an Op Amp integrator, a triangular waveform can also be generated. The outputs can be frequency modulated via the FM input.

FREQUENCY MULTIPLIER/DIVIDER WITH INFINITE RESOLUTION

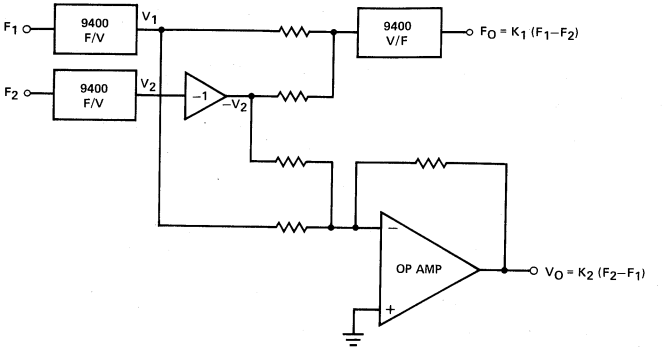


$$F_{OUT} = K_1 K_2 \left(\frac{R_2}{R_1 + R_2}\right) F_{IN}$$

Frequency scaling can easily be performed by first converting the incoming frequency into a proportional DC voltage. This is accomplished by using the 9400 in the F/V mode. Once the frequency is in a voltage format it is easy to scale this voltage up or down by use of a single potentiometer. The resultant voltage is then applied to a 9400 V/F which generates a proportional output frequency.

Since the potentiometer is infinitely variable, the division/multiplication factor can be any number, including fractions, (K_1 is simply V_O/F_{IN} while K_2 is F_O/V_{IN}).

FREQUENCY DIFFERENCE MEASUREMENT



Frequency difference measurement is accomplished by using two 9400's in the F/V mode to convert both frequencies into two proportional analog voltages (V_1 and V_2). V_2 is inverted by a unity gain inverter. V_1 and $-V_2$ are then added by the summing Op Amp to give a voltage proportional to the frequency difference between F_2 and F_1.

Since the 9400 V/F input is actually the summing junction to an Op Amp, V_1 and $-V_2$ can be summed at the 9400 input to generate a frequency output which is proportional to the difference between F_1 and F_2.

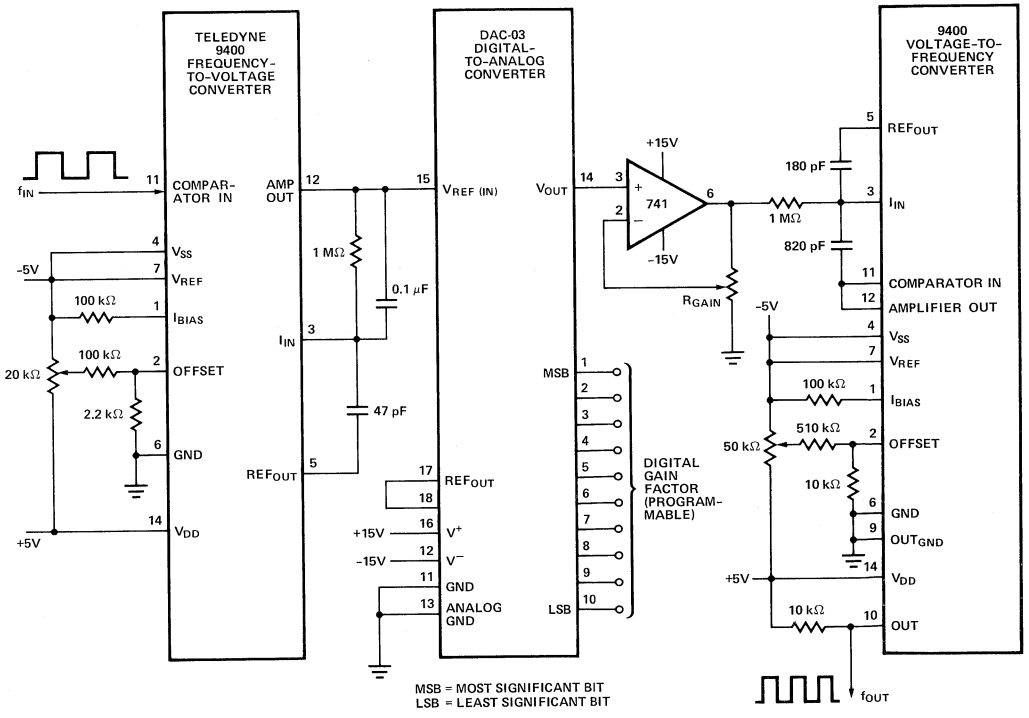
CONVERTERS SIMPLIFY DESIGN OF FREQUENCY MULTIPLIER*

By using a programmable digital-to-analog converter in combination with frequency-to-voltage and voltage-to-frequency converters, this circuit can multiply an input frequency by any number. Because it needs neither combinational logic nor a high-speed counter, it is more flexible than competing designs, uses fewer parts, and is simpler to build.

As shown in the figure, the V/F converter, a Teledyne 9400, transforms the input frequency into a corresponding voltage. An inexpensive device, the converter requires only a few external components for setting its upper operating frequency as high as 100 kilohertz.

Next the signal is applied to the reference port of the DAC-03 d-a converter, where it is amplified by the frequency-multiplying factor programmed into the converter by thumbwheel switches or a microprocessor. The d-a converter's output is the product of the analog input voltage and the digital gain factor.

R_3 sets the gain of the 741 op amp to any value, providing trim adjustment or a convenient way to scale the d-a converter's output to a much higher or lower voltage for the final stage, a 9400 converter that operates in the voltage-to-frequency mode. The 741 and R_3 can also be used to set circuit gain to non-integer values. The V/F device then converts the input voltage into a proportionally higher or lower frequency.



Circuit uses frequency-to-voltage-to-frequency conversion, with intermediate stage of gain between conversions, for multiplying input frequency by any number. Digital-to-analog converter is programmed digitally, by thumbwheel switches or microprocessor, for coarse selection of frequency-multiplying factor; 741 provides fine gain, enables choice of non-integer multiplication values.

Application Note 11
TSC7106/7107
Digital Meter Applications
Including Kit Assembly Instructions

Instructions for the LCD and LED Kits

Two kits are offered; the TSC7106 EV/Kit and the TSC7107 EV/Kit. Each kit contains the appropriate IC, a circuit board, a display (LCD/TSC7106, LED/TSC7107), passive components and miscellaneous hardware.

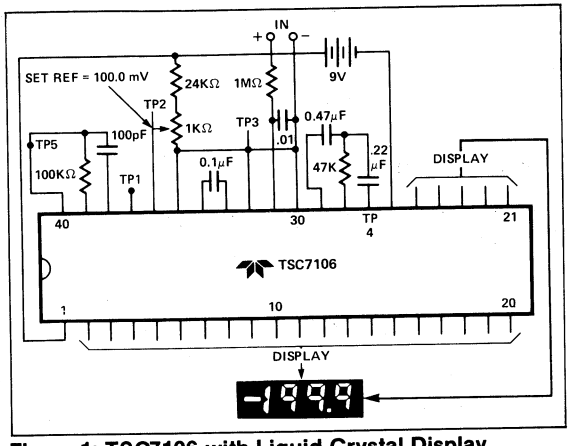


Figure 1: TSC7106 with Liquid Crystal Display

The TSC7106 and TSC7107 contain all the acive circuitry for a 3-1/2 digit panel meter on a single chip. The TSC7106 is designed to interface with a liquid crystal display (LCD), while the TSC7107 is intended for the light-emitting diode (LED) display. Both circuits contain BCD to seven segment decoders, display drivers, a clock and a reference. To build a high-performance panel meter, (with auto-zero and auto polarity features) it is only necessary to add a display, four resistors, four capacitors, and an input filter if required.

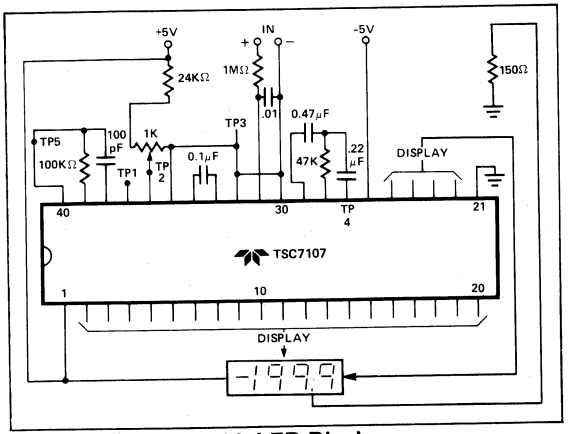


Figure 2: TSC7107 with LED Display

Assembly

The circuit board layouts and assembly drawings are shown in Figure 17 (TSC7106) and Figure 18 (TSC7107). Pin strips are used to provide a low-cost socket. One IC board can thus be used to evaluate several IC's. Solder terminals are provided for the first five test points and for the ± 5 V input on the TSC7107 kit. A provision has been made for separating REF LO from COMMON when using an external reference zener. Provision has also been made for connecting an external clock. A value of 150 ohms is used for decimal point (TSC7107 EV/Kit).

Liquid Crystal Display (TSC7106)

The TSC7106 generates the symmetrical square wave to the back plane (B.P.) internally. The user should generate the decimal point from the plane drive by inverting the B.P. (pin 21) output.

In some displays, a satisfactory decimal point can be achieved by tying the decimal plane to COMMON (pin 32). This pin is internally regulated at about 2.8 volts below V^+. Prolonged use of this technique, however, may permanently burn-in the decimal, because COMMON is not exactly midway between B.P. high and B.P. low. In applications where the decimal point remains fixed, a simple MOS inverter can be used (Figure 3). For instruments where the decimal point

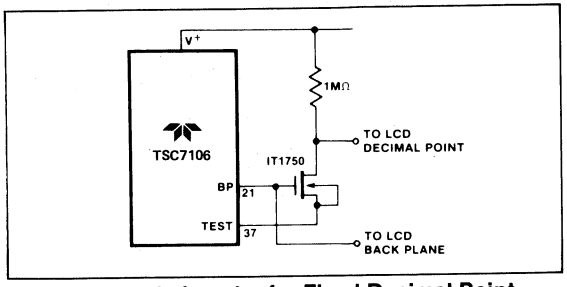


Figure 3: Simple Inverter for Fixed Decimal Point

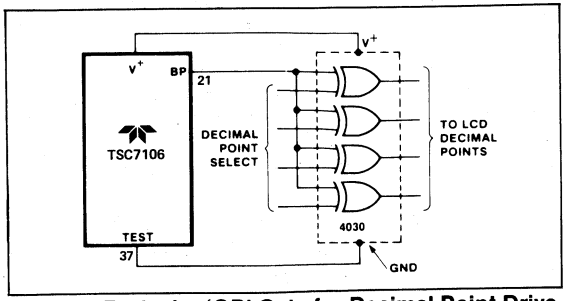


Figure 4: Exclusive 'OR' Gate for Decimal Point Drive

must be shifted, a quad exclusive OR gate is recommended (Figure 4). Note that in both instances, TEST (pin 37, TP1) is used as V^- for the inverters. This pin is capable of sinking about 1 mA and is approximately 5 volts below V^+. The B.P. output (pin 21) oscillates between V^+ and TEST.

Light Emitting Diode Display (TSC7107)

The TSC7107 will sink 8 mA per segment. This drive produces a bright display suitable for most applications. A fixed decimal point can be turned on by tying the appropriate cathode to ground through a 150 ohm resistor. The circuit boards supplied with the kits will accommodate either HP 0.3 displays or the MAN 3700 types. Note that the HP has the decimal point cathode on pin 6, whereas the MAN 3700 has the decimal point cathode on pin 9. Not all the decimal points are brought out to jumper pads. It may be necessary to wire directly from the 150 ohm resistor to the display. For multiple range instruments, a 7400 series CMOS quad gate should be used.

Full-Scale Readings

200 mV Full-Scale — The kits have been optimized for 200 mV Full-Scale. The component values supplied are those specified in Figures 1 and 2.

2,000 V Full-Scale — The component values in Table 1 change the integrator time constant and reference and the auto-zero capacitor time constant. These extra components are not supplied in the kits. In addition, the decimal point jumper should be changed so that the display reads 1.999.

Table 1: Component Values for Full Scale Options

Component (Type)	200.0 mV Full Scale	2.000 V Full Scale
C_2 (mylar)	0.47 μF	.047 μF
R_1	24KΩ	1.5KΩ*
R_2	47KΩ	470KΩ

*Changing R_1 to 1.5KΩ will reduce the battery life of the 7106 kit. As an alternative, the potentiometer can be changed to 25KΩ.

Clock

Setting the clock oscillator at precisely 48 kHz will result in the optimum line frequency (60 Hz) noise rejection (Figure 5). Since the integration period is an integral number of the line frequency period, the RC oscillator supplied in the kit runs at approximately 48 kHz giving a measurement frequency of three readings per second. Countries with 50 Hz line frequencies should set the clock to 40 kHz by increasing the value of the 100 k ohm resistor across pins 39 and 40 to 120 k ohms.

An external clock can also be used. In the TSC7106, the internal logic is referenced to TEST. External clock waveforms should therefore swing between TEST and V^+ (Figure 6A). In the TSC7107, the internal logic is referenced to GND so any generator whose output swings from ground to +5 V will work well, (Figure 6b).

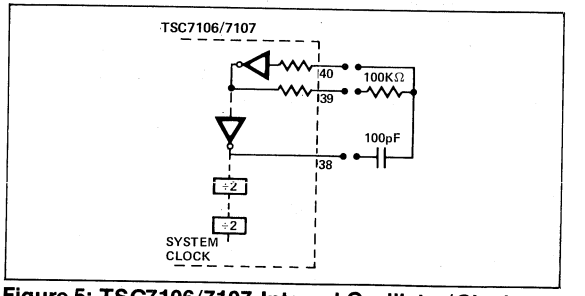


Figure 5: TSC7106/7107 Internal Oscillator/Clock

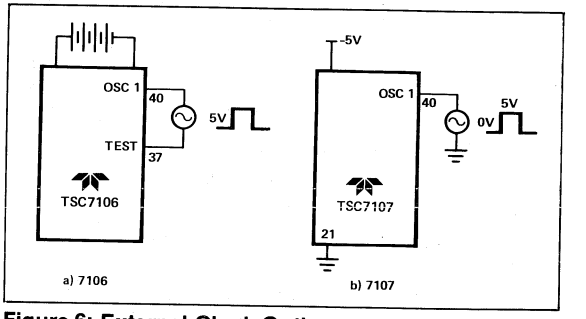


Figure 6: External Clock Options

Capacitors

The dual slope technique cancels the effects of long term stability and temperature coefficient. The integration capacitor should have low dielectric loss. Inexpensive polypropelene capacitors have the low dielectric loss characteristics and are recommended. Mylar capacitors may be used for C1 (reference) and C2 (auto-zero).

Reference

The voltage between V^+ and COMMON is internally regulated at about 2.8 volts. This reference is adequate for many applications. For improved performance use TSC7106A/-7107A devices.

For 200 mV Full-Scale, the voltage applied between REF HI and REF LO should be set at about 100 mV. For 2.000 V Full-Scale, set the reference voltage at 1.0.V. The reference inputs are floating, and the only restriction on the applied voltage is that it should lie in the range V^- to V^+. For calibration, place 190.0 mV on input and adjust REF pot (R_4) for 1900 readout.

For greater temperature stability, an external reference can be added as shown in Figures 7a and 7b.

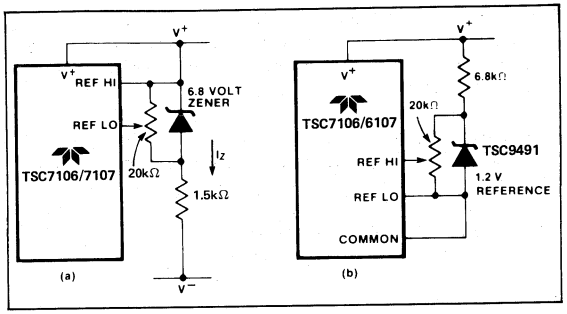


Figure 7: Using an External Reference

Power Supplies

The TSC7106 kit is intended to be operated from a 9 V battery. INPUT LO is shorted to COMMON, causing V^+ to sit at 2.8 volts positive with respect to INPUT LO, and V^- at 6.2 volts negative with respect to INPUT LO.

The TSC7107 kit should be operated from ±5 volts. Noisy supplies should be bypassed with 6.8 μF tantalum capacitors to ground at the point where the supplies enter the board.

If a -5 volt supply is unavailable, a suitable negative rail can be generated locally using the circuit shown in Figure 8.

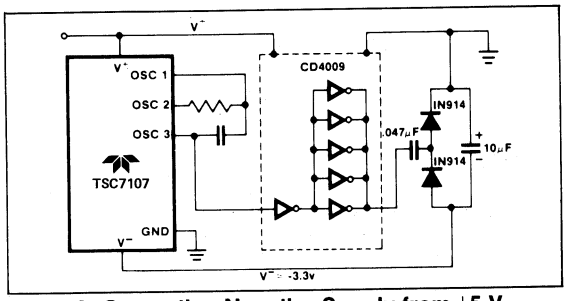


Figure 8: Generating Negative Supply from +5 V

Input Filters

With the leakage current in the order of 1 pA at 25°C, high impedance passive filters may be used. The RC filter used in the evaluation kits (1 megohm — 0.01 μF) introduces a negligible 1 μV error.

Sources of Supply

The following list of suppliers is intended to help with the development of production meters. It should not be interpreted as a comprehensive list of suppliers, nor does it constitute an endorsement by Teledyne Semiconductor:

Suppliers of LCD's

1. Hamlin Inc., WI (414) 648-2361
2. Crystalloid Electronics, OH (216) 688-1180
3. Printed Circuits Integrated, CA (408) 733-4603
4. IEE Inc., CA (213) 787-0311

Suppliers of LED's

1. AND, CA (415) 347-9916
2. Litronix Inc., CA (408) 257-7910
3. Hewlett-Packard, CA (415) 493-1212
4. General Instruments, CA (415) 493-0400

Suppliers of Polypropelene Capacitors

1. Plessey Capacitors, CA (213) 889-4120
2. IMB Electronic Products, CA (213) 921-3407
3. Elcap Electronics, CA (714) 979-4400
4. TRW Capacitors, NB (308) 284-3611

Preliminary Tests

1. Solder flux or other impurities on PC boards may cause leakage paths between IC pins and board traces, reducing performance. Rubbing alcohol or another appropriate cleaning agent should be used to remove impurities.
2. In order to insure that unused segments on the LCD displays do not turn on, tie them to the Back Plane pin (pin 22).
3. Auto-Zero — With the inputs shorted the display should read zero. The negative sign will be on about one half of the time, showing the input to be exactly zero volts.
4. Polarity — A negative sign indicates a negative reading. No sign indicates a positive reading.
5. Overrange — For inputs greater than Full-Scale, only 1 or -1 will be displayed. The three least significant digits will be suppressed.
6. Calibration — The instrument should be calibrated at 1900 counts by using a high-quality 4 1/2 digit DVM.

Applications

Input Attenuator

There are times it is desirable to have full scale readings other than 199.9 mV or 1.999 V. To measure voltages greater than 2V, an input attenuator is needed as shown in Figure 9.

The Full-Scale sensitivity is given by:

$$V_{IN}\ (\text{Full-Scale}) = 1.999\ V_{REF} \times \frac{R_2}{(R_1 + R_2)}$$

It is important that R_1 and R_2 remain fixed for the calibration period of the instrument. Metal film resistors with good long-term drift characteristics, and low temperature coefficients are recommended.

The input attenuator reduces the input resistance of the circuit from $>10^{12}$ ohms to $(R_1 + R_2)$. This places an upper limit of about 10 megohms on the input resistance that can readily be achieved when using an attenuator before the A/D input current causes offset errors.

To measure Full-Scale voltage less than 199.9 mV, an operational amplifier is used prior to the TSC7106/7 inputs. Note that the auto-zero circuitry within the IC can not take care of the op amp offset or voltage drift. For example, the use of the 308A will add 1 μV/°C voltage drift typical.

15

Figure 10 shows a circuit with ±20 mV Full-Scale and an input resistance greater than 10 megohms.

For scale factors between 100 mV and 1 mV per least significant digit (LSD), simply determine the reference voltage required for the following equation:

V_{REF} = (Voltage Change represented by one LSD) x 10^3

For scale factors greater than 1 mV/LSD, the most straight forward approach is to use an input attenuator in conjunction with a 1 volt reference.

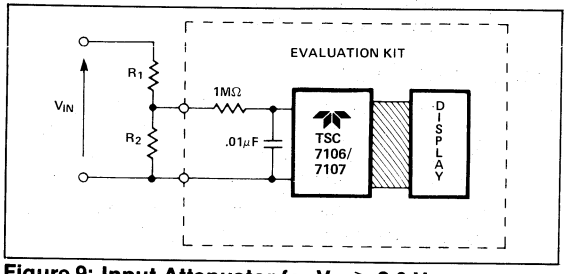


Figure 9: Input Attenuator for $V_{IN} \geq 2.0$ V

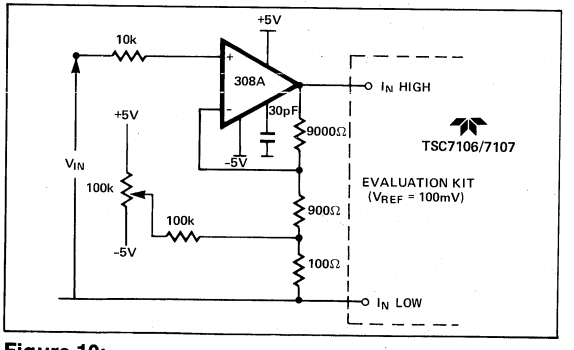


Figure 10:

AC Voltage Measurements

It is necessary to build an AC to DC converter to measure AC voltages with the TSC7106/7. Figure 11 shows a circuit used extensively in commercial 3 1/2 digit DVM's. The circuit responds to the average value of the sinusoidal waveform and assumes low distortion. It has 10 megohms input impedance, 20 Hz to 5 kHz bandwidth, and is AC coupled to the kit introducing to DC errors.

Multi-Range DVM's

Two schemes commonly used are shown in Figures 12a and 12b. The circuit of Figure 12a has the advantage that any switch contact resistance appears in series with the TSC7106/7 input resistance. Since the input resistance is $>10^{12}$ ohms, errors due to the switch are negligible. Precision voltage attenuators (R_1 through R_5) are available from a number of manufacturers. Allen Bradley, for example, makes a thin film network which contains 1 k, 9 k, 90 k, 900 k and 9 M resistors in one package (FN207) — ideal for a five range voltmeter. However, it is less expensive to use medium precision resistors in series with potentiometers for the attenuator. Then the schematic of Figure 12b has some of the advantages because the resistors in the attenuator are non-interactive. It is also more amenable to solid state range switching. An analog switch or FETs may be used in place of the mechanical switch. Then, by adding a couple of zener diodes (or ordinary silicon diodes in the case of a 200 mV F.S. panel meter) the solid state switch is totally protected against overvoltages. By contrast, the configuration of Figure 12a exposes the switch to the full-input voltage, which may be several hundred volts. However, in Figure 12b the switch resistance forms part of the attenuator and could contribute an error.

Resistance Measurements

The ratiometric technique is used. The unknown resistance is put in series with a known standard and a current passed through the pair. The voltage developed across the unknown is applied to the input (between IN HI and IN LO), and the voltage across the known resistor applied to the reference input (REF HI and REF LO). If the unknown equals the standard, the display will read 1000. The displayed reading can be determined from the following expression:

$$\text{Displayed Reading} = \frac{\text{R Unknown}}{\text{R Standard}} \times 1000$$

Figure 13 shows a typical measurement circuit. Note that due to its ratiometric nature, the technique does not require an accurately defined reference voltage. The display will overrange for R Unknown ≥ 2 x R Standard.

Current Measurements

The use of a shunt resistor converts the current to a voltage. The relationship between the current and the displayed reading for the circuit of Figure 14 is found by:

$$\text{Displayed Reading} = \frac{I_{IN} \times R_S}{V_{REF}} \times 1000$$

When measuring current the 199.9 mV scale is used. This limits the voltage drop to 100 μV per count. A multi-range current meter circuit is shown in Figure 15. Note that although the input current passes through the selector switch, IR drops across the switch do not contribute to the measured voltage.

Temperature Measurements

A diode connected transistor may be used as the temperature sensing element. V_{BE} has a temperature coefficient of −2.1 mV/°C. A scale factor of 0.1°C/count may be obtained by setting the reference at 210 mV.

At 0°C and 100μA bias current, the diode connected transistor will have a forward voltage drop of approximately 550 mV. A fixed 500 mV source is set up to offset the diode drop. In the circuit of Figure 16, adjust R5 to give 000.0 output reading with Q1 at 0°C. Then adjust for R4 for a 100.0 reading with Q1 at 100°C.

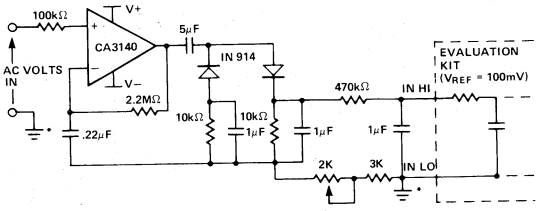


Figure 11: AC to DC Converter

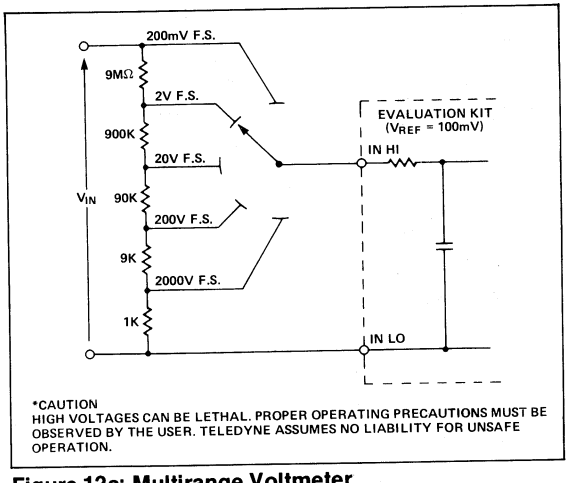


Figure 12a: Multirange Voltmeter

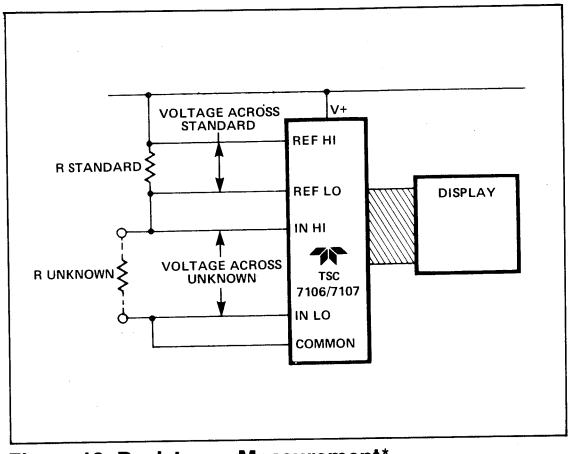


Figure 13: Resistance Measurement*
(*Requires some modification to the kit)

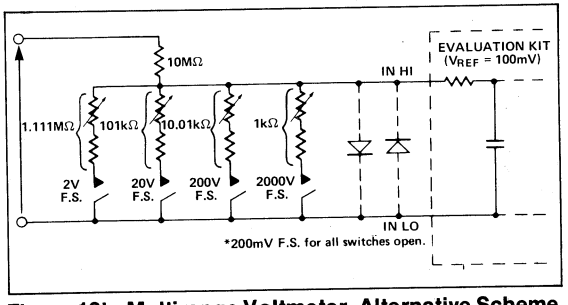


Figure 12b: Multirange Voltmeter, Alternative Scheme

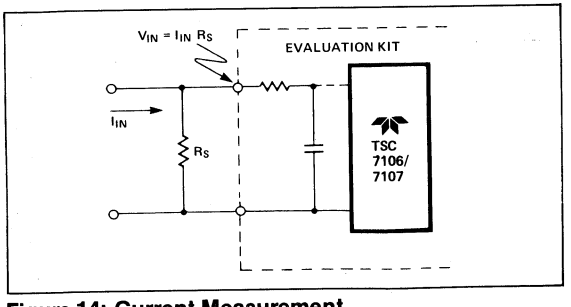


Figure 14: Current Measurement

15

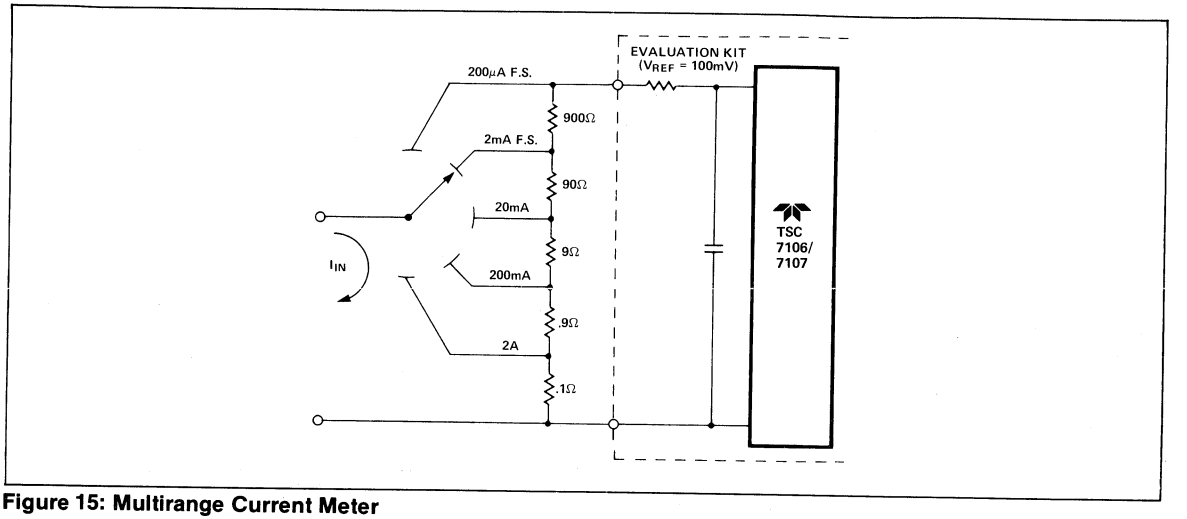


Figure 15: Multirange Current Meter

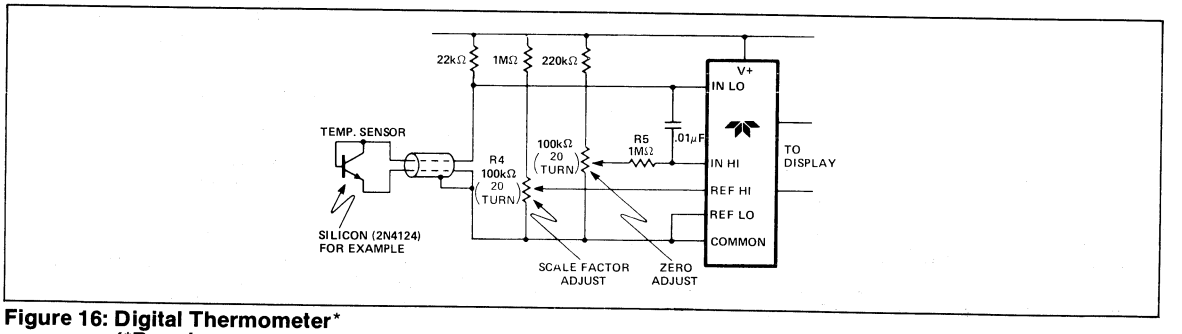
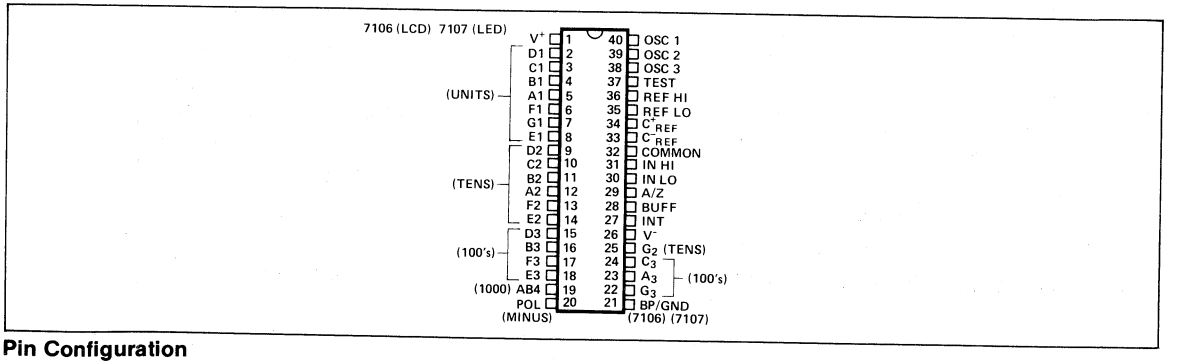
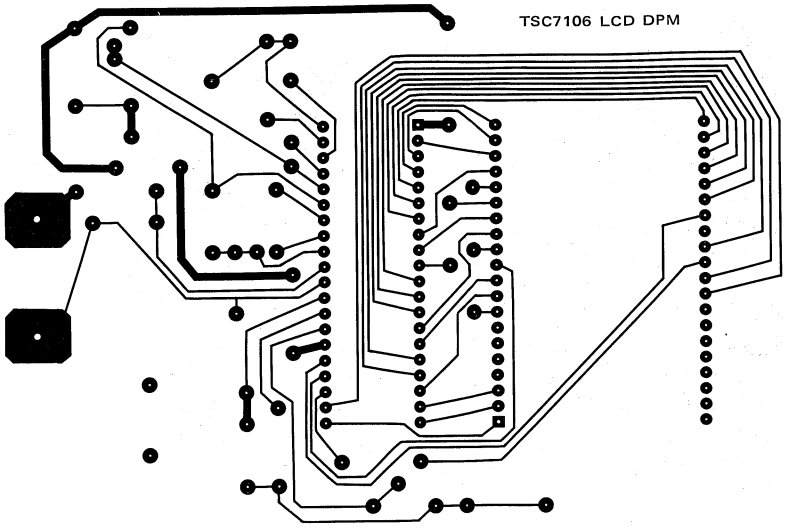


Figure 16: Digital Thermometer*
(*Requires some modification to the kit)



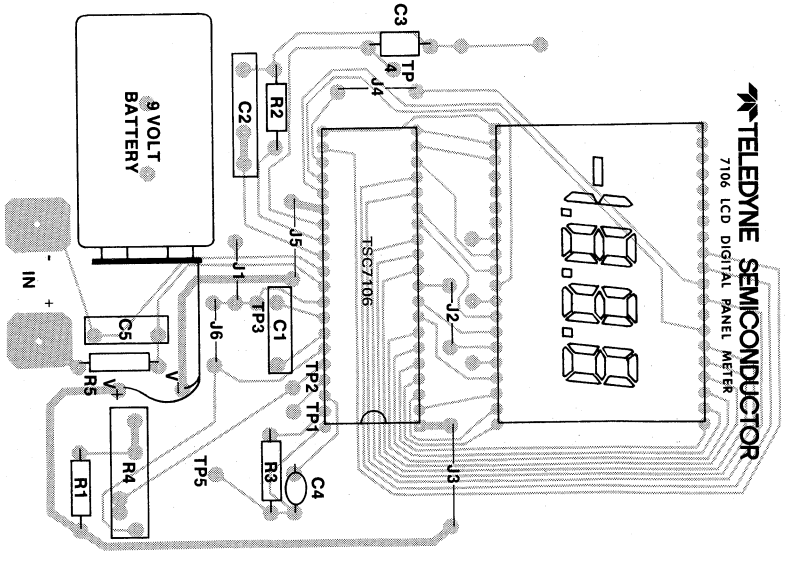
Pin Configuration



ACTUAL SIZE NOT SHOWN

LEGEND:

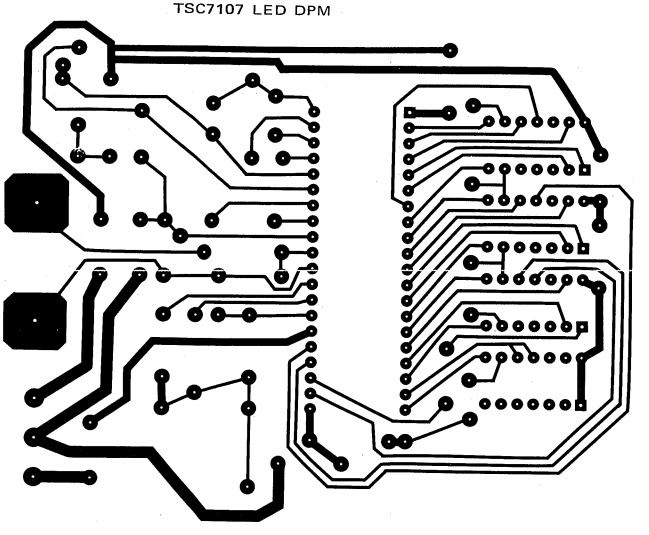
C1	0.1 Mf	R1	24 K 1/4 W 5%
C2	0.47 Mf	R2	47 K 1/4 W 5%
C3	0.22 Mf	R3	100 K 1/4 W 5%
C4	100 pf	R4	1 K POT
C5	0.01 Mf	R5	1 M 1/4 W 5%



ACTUAL SIZE NOT SHOWN

Figure 17: TSC7106 – Circuit Board Layout and Component Placement

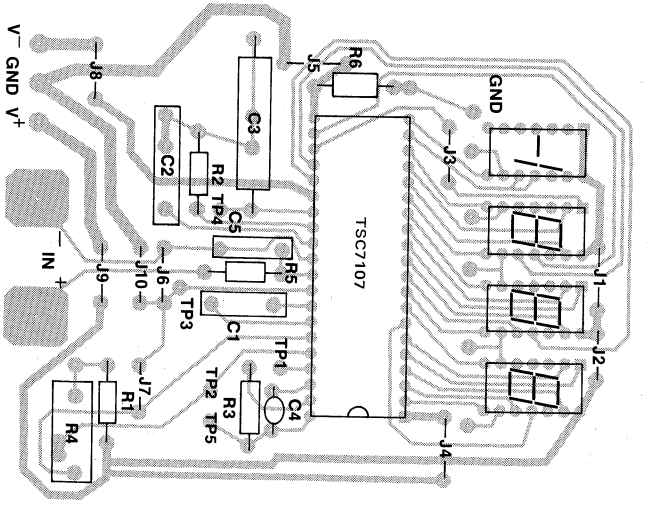
TSC7107 LED DPM



ACTUAL SIZE NOT SHOWN

LEGEND

C1	0.1 Mf	R1	24 K 1/4 W 5%
C2	0.47 Mf	R2	47 K 1/4 W 5%
C3	0.22 Mf	R3	100 K 1/4 W 5%
C4	100 pf	R4	1 K POT
C5	0.01 Mf	R5	1 M 1/4 W 5%
		R6	150 Ω 1/4 W 5%



ACTUAL SIZE NOT SHOWN

Figure 18: TSC7107 – Circuit Board Layout and Component Placement

TELEDYNE SEMICONDUCTOR

Application Note 12
A Single IC Digital Thermocouple Thermometer Using the TSC7106

By Al Kadis

Due to the extremely low input noise characteristics of the TSC7106/7107, the user may build a digital thermocouple thermometer with only one active component and fifteen passive components. With this circuit, both type J and type K thermocouples may be used. The type J will measure over the temperature range of 10 to 530° C with a conformity of ±2° C. The type K will measure over a temperature range of 0° C to 1000° C with a conformity of ±3° C.

In operation, the TSC7106 provides all A/D functions including seven segment decoder, display drive, reference, and a clock. True differential low noise input allows the bridge circuit shown in Figure 2 with no other active components. This circuit will give a three month life when operated from a normal alkaline 9 volt battery.

The circuit using a type J thermocouple will be discussed here. (The circuit for the type K thermocouple is similar except for the changing of component values and the replacement of the type J thermocouple with type K). The extremely low noise front-end of the TSC7106/7107 allows the IC to operate reliably at one-half its minimum reference voltage specifications, approximately 50 microvolts per count.

A thermocouple is made by the junction of two dissimilar metals. Figure 1 shows the type J (iron and constantan) thermocouple in a temperature measuring mode.

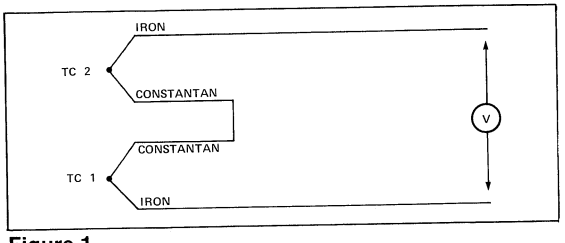


Figure 1.

A voltage is generated as a function of the difference in temperature between the two iron — constantan thermocouples — TC 1 and TC 2. If TC 1 is kept at a constant temperature (such as the freezing temperature of water), the voltage generated as a function of temperature of TC 2 is displayed in the normal type J thermocouple charts. The sensitivity at room temperature is approximately 50.4 μV/° C.

Figure 2 shows the circuit for a portable battery operated thermocouple thermometer using the TSC7106. The circuit uses six components in addition to those required for the standard TSC7106 circuitry. The TSC7106 is designed for normal 200 mV operation. Then the reference voltage is readjusted to 50.4 mV which corresponds to 1,000 times the one degree sensitivity of the type J thermocouple.

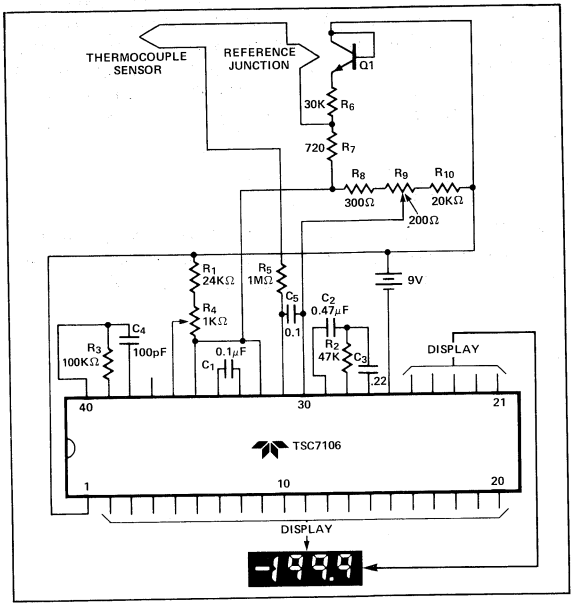


Figure 2.

Since the thermocouple reference can not be easily maintained at a constant temperature, a circuit is used which provides a voltage that changes with temperature in an equal and opposite manner to the thermocouple. When combined with the thermocouple this has the effect of simulating the reference at a constant temperature over the normal ambient.

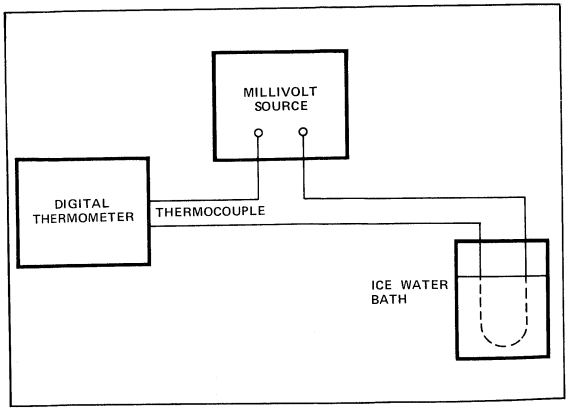


Figure 3.

15

The circuit generating the compensating voltage is composed of Q1, R6 and R7. Q1 may be any small signal transistor.

A voltage equal and opposite to that generated by the thermocouple occurs as follows: Q1 base and collector leads are tied together allowing Q1 to operate as a diode. In this mode, the forward voltage drop of the diode connected transistor is -2.1 millivolts per degree centegrade. R7 is returned to the TSC7106 reference. The junction of R6 and R7 will vary by the ratio of

$$2.1\ mV/^\circ C \quad \frac{720}{30{,}000} = 50.4\ \mu V/^\circ C.$$

One end of the thermocouple is attached to this point. The thermocouple reference and the transistor should be thermally bonded. In this manner, temperature changes of the thermocouple will be compensated by the transistor and resistor divider R6 and R7. R8, R9 and R10 form the other leg of a bridge. The 200 Ω pot (R9) center arm is fed to the negative or reference section of the input amplifier. The thermocouple output is fed to the positive section.

Calibration is accomplished by the use of an ice water bath and millivolt source as shown in Figure 3. The ice water bath is used as a O° C reference. The millivolt source is used to simulate thermocouple temperature over the range of 10 to 530° C. R9 is used for zero adjustment and R4 is used for full-scale. The thermocouple temperature curve is calibrated for best accuracy over the user's temperature range. Type K thermocouple is fabricated in a similar manner by changing the thermocouple type and resistor values and readjusting 0 and full-scale. The TSC7107 may also be used as a laboratory thermometer with similar circuitry.

TELEDYNE SEMICONDUCTOR

Application Note 16
TSC7135 Microprocessor Interface

By Wes Freeman

Many data acquisition systems require both a visual display and a computer interface. The TSC7135 from Teledyne Semiconductor is a 4-1/2 digit Analog-to-Digital converter (ADC) which can easily provide both of these functions. The TSC7135's multiplexed BCD outputs interface easily to low cost LED or LCD decoder/drivers, such as the TSC7211A (LCD) and TSC7212A (LED) or TSC700A (high-current LED). Also, the TSC7135's data outputs simplify computer interfacing.

This application note will present both the hardware and software required to interface the TSC7135 to a microprocessor. The circuit was developed for a 6502 μP and 6522 I/O port, but the design can easily be modified for other μPs and I/O ports.

The TSC7135 has several features which make it an attractive choice for data acquisition where speed is not an overriding consideration. The analog features include:

- High resolution ..... 20,000 counts
- High accuracy ..... ± 1 count
- Low roll-over error ..... ± 1 count
- Valid polarity at 000 reading (the + and - zero states give an extra bit of resolution)
- Negligible zero drift - definitely not the case with a bipolar DAC/SAR type ADC

Timing Relationship Between TSC7135 Outputs

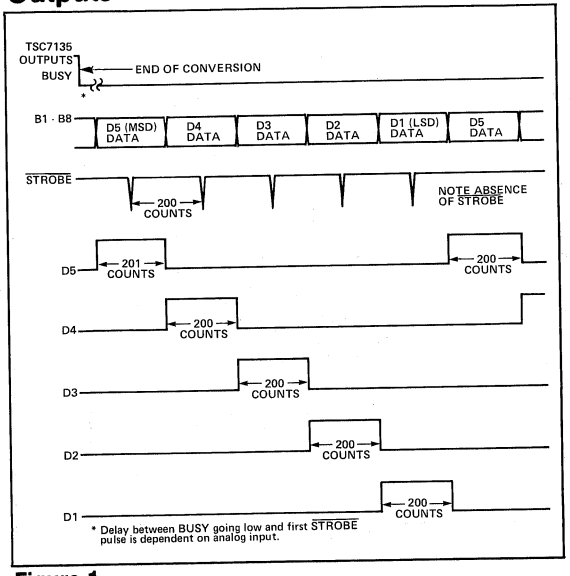


Figure 1

- The dual-slope conversion method rejects 50 Hz, 60 Hz, and 400 Hz noise.
- The ratiometric reference and differential inputs provide flexible transducer interfacing.

The TSC7135 also has features that simplify system design:

- Easy μP Interfacing
- Overrange and underrange flags for autoranging and process control decisions
- Operation from ± 5 V supplies, with only 10 mW typical power dissipation
- TTL compatible outputs (1.6 mA sink current)

The TSC7135 provides output signals which, together with one port of an LSI I/O chip, simplify a microprocessor interface. The relationship between the various TSC7135 outputs is shown in Figure 1. The specific function of these outputs are as follows:

TSC7135	Pin Function
• B1-B8	BCD coded data is output on the B1-B8 pins.
• DS5-DS1	Digit Select 5 (most significant digit) through Digit Select 1 (least significant) go high as data on B1-B8 becomes valid for that digit.
• STROBE	For the first digit scan after a conversion $\overline{\text{STROBE}}$ goes low (for 1/2 clock period) in the middle of each digit strobe. After five pulses, $\overline{\text{STROBE}}$ stays high until the next conversion is complete.
• BUSY	BUSY is high while the TSC7135 is in Integrate or Deintegrate phases of a conversion. The falling of BUSY can, therefore, be used as an end of conversion signal.
• POL	POLARITY is high if the analog input polarity is positive.
• OR	OVERRANGE goes high if the analog input is greater than full scale (reading > 20,000), while UNDERRANGE goes high if the reading is 1,800 or less.
• UR	

The TSC7135 also has a RUN/$\overline{\text{HOLD}}$ input. If RUN/$\overline{\text{HOLD}}$ is held low, the converter will remain in the auto-zero phase. A new conversion will not begin until RUN/$\overline{\text{HOLD}}$ goes high. This input can be used to generate conversions on command.

15

Interface Hardware

The complete TSC7135 to SYP6522 interface schematic is shown in Fiqure 2. BCD data, POL, OR, UR, and DS5 are connected to the 6522's PA0 through PA7 inputs. The TSC7135's $\overline{\text{STROBE}}$ output interrupts the microprocessor via the 6522's CA1 interrupt. RUN/$\overline{\text{HOLD}}$ can be controlled by programming CA2 as an output.

At first glance, the circuit may appear incomplete because digit selects DS4 through DS1 are not connected. However, DS5 is the only digit select required. As mentioned previously, there are only 5 $\overline{\text{STROBE}}$ pulses per conversion cycle, with the first $\overline{\text{STROBE}}$ occurring during DS5. The μP decodes the logical "AND" of DS5 and $\overline{\text{STROBE}}$ (DS5 · $\overline{\text{STROBE}}$) as a conversion complete signal.

If the μP finds (DS · $\overline{\text{STROBE}}$) true upon responding to an interrupt, an "end of conversion" is assumed and assembling of BCD data from the TSC7135 begins. Each of the next four interrupts will provide another BCD digit. The μP counts interrupts in a register and stores the corresponding BCD data in successive memory locations. After five $\overline{\text{STROBE}}$ pulses, all BCD data has been transferred to the μP and conversion is complete.

One constraint of this interface method is that the μP must respond to each digit's interrupt before the next digit becomes valid. The 6522's CA1 input can be programmed to latch data into Port A, as well as provide an interrupt to the μP. Since latched data remains valid until the next $\overline{\text{STROBE}}$ pulse, the μP has the full interval between $\overline{\text{STROBE}}$ pulses to service each interrupt. $\overline{\text{STROBE}}$ pulses are 200 clock cycles apart. A TSC7135 clock frequency of 100 kHz will allow the μP two milliseconds (10 μsec x 200 clock cycles) to respond to each interrupt without losing data.

Interface Software

Software for the TSC7135 to 6502 interface can be divided into three routines: (1) Programming the 6522's Port A for latched input and interrupt from pin CA1; (2) the interrupt service routine which actually acquires and stores BCD data from the TSC7135; (3) display or manipulation of the acquired data. Figure 3 is a 6502 assembly language listing of the first two routines. An interrupt service routine flow chart is shown in Figure 4. Since the end of a digit scan leaves 5 digits of BCD data in successive memory locations, the user will find the interface software easy to incorporate into a specific display or manipulation routine.

The 6522 I/O port must be programmed before data can be received from the TSC7135. The code in Figure 3, beginning at location "SET-UP", writes data into the 6522's control registers to enable the following functions: (1) Port A will be a latched input, controlled by input CA1; (2) CA2 will be an output, programmed high (TSC7135 in "RUN" mode); (3) Interrupt enabled on the falling edge of CA1. The function of data written to each 6522 register is defined in Figure 5.

When programmed for interrupt operation, the 6522 will pull its IRQ output low on the falling edge of each $\overline{\text{STROBE}}$ pulse from the TSC7135. Assuming interrupts are enabled, IRQ going low will cause the 6502 μP to load the address of an interrupt service routine from memory locations FFFE and

TSC7135 to 6502 μP Interface Schematic

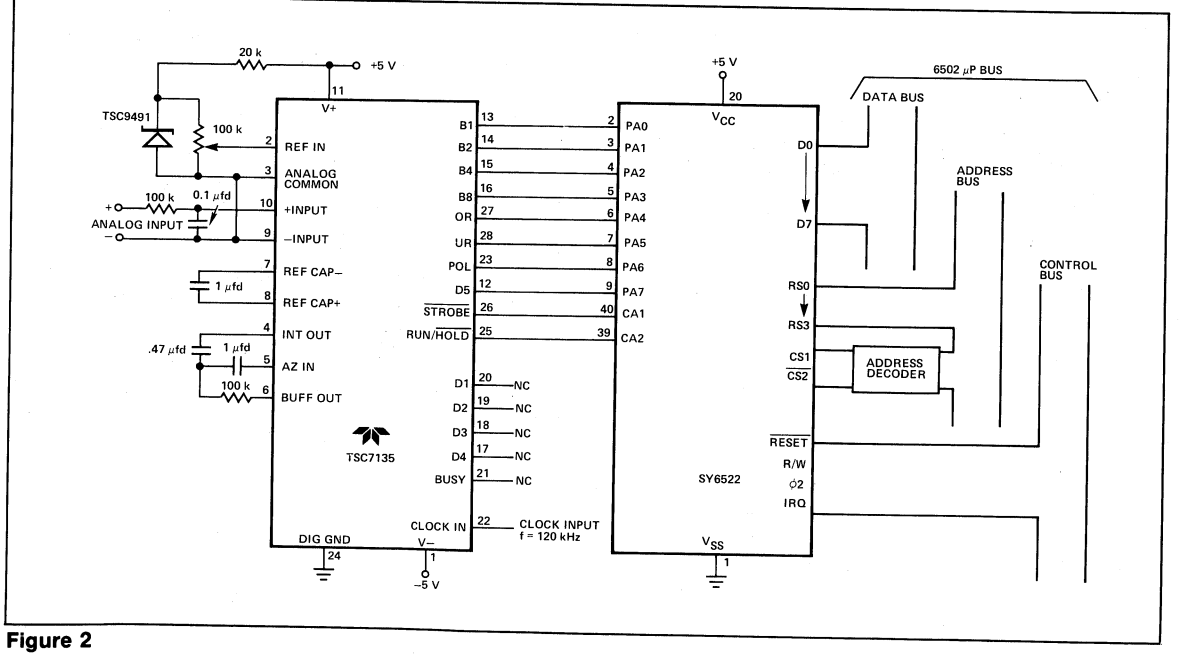


Figure 2

FFFF. This routine will typically identify the interrupting device, determine its priority and jump to a program to service the interrupt. The user must provide software to vector interrupts coming from the TSC7135 to the service routine located at location "INTVEC" of Figure 3. The TSC7135 - 6522 hardware can accommodate interrupt service delays of up to two msec, so a relatively low-priority interrupt status can be used.

6502 - Assembly Language Listing

```
;
;-------------------------------------------------
; TSC7135 INTERFACE TO A 6502 MICROPROCESSOR
;  USING A 6522 I/O PORT
;
; RESULTS ARE STORED IN 5 BYTES OF ZERO-PAGE
;  MEMORY, BEGINNING AT LOCATION "DIGSTOR"
;  (MOST SIGNIFICANT DIGIT FIRST)
;
; USER MUST PROVIDE INTERRUPT VECTOR FROM
;  THE 6522'S CA1 INTERRUPT TO A ROUTINE
;  AT "INTVEC"
;
;-------------------------------------------------
;
;SET UP 6522 FOR INTERRUPT OPERATION
;
IO&RT   .EQU    0A800   ;ADDRESS OF 6522 I/O PORT
SETUP   .EQU    028D    ;ADDR OF 6522 SET UP ROUTINE
;
        .ORG    SETUP
        LDA     #01     ;SET PORT A FOR
        STA     IO&RT+0B;LATCHED INPUT
        LDA     #0E     ;CA1=INT ON NEG EDGE
        STA     IO&RT+0C;CA2=HIGH (7135 IN "RUN" MODE)
        LDA     #082    ;ENABLE CA1 INTERRUPT
        STA     IO&RT+0E;
        JMP     MAINPRG ;I/O PORT SETUP COMPLETE, SO
                        ; JUMP TO OPERATING SYSTEM OR
                        ; TO MAIN PROGRAM
;
;BEGIN INTERRUPT SERVICE ROUTINE
;
XSTOR   .EQU    81      ;SAVE X REGISTER
DIGSTOR .EQU    82      ;SAVE RESULTS HERE
INTVEC  .EQU    02E0    ;6522'S CA1 INTERRUPT ROUTINE
        .ORG    INTVEC
;
        LDA     IO&RT+1 ;GET DIGIT FROM 6522
        BPL     NXTDIG  ;IF MSB=0, THIS IS NOT THE MOST
                        ; SIGNIF DIGIT, SO CONTINUE
        BIT     OVRBIT  ;CHECK FOR OVERRANGE
        BNE     OVRANG  ;BRANCH TO ERROR ROUTINE
        LDX     #00     ;SET THE DIGIT POINTER
        STX     XSTOR   ; AND STORE
;
NXTDIG  LDX     XSTOR   ;GET DIGIT POINTER
        STA     DIGSTOR,X ;STORE DIGIT IN ZERO PAGE
        INX             ; AND POINT TO
        STX     XSTOR   ; THE NEXT DIGIT
        CPX     #05     ;5 DIGITS COMPLETES ONE SCAN
        BEQ     DONE    ;CONVERSION COMPLETE, PROCESS
                        ;OR DISPLAY DATA
                        ;THE 'DONE' ROUTINE MUST END WITH 'RTI'
        RTI             ;RETURN IF NOT COMPLETE
;
;
OVRANG  LDX     #01     ;SET DIGIT COUNTER SO THAT DIGITS
        STX     XSTOR   ; WILL NOT OVERFLOW ZERO PAGE MEM
        NOP             ;IF REQUIRED, USER PROGRAM FOR
        NOP             ; SERVICING OVERRANGE GOES HERE
        RTI             ;AND RETURN
;
;
        .END
```

Figure 3

Once the 6522's interrupt has been recognized and vectored to location "INTVEC", a read of Port A loads the TSC7135 data into the 6502 accumulator. Reading Port A also sets the μP's status flags and resets the 6522's interrupt flag.

The μP now tests whether the accumulator contains the TSC7135's most significant digit by testing for DS5 being high. Connecting DS5 to PA7 (MSB) of the I/O port allows testing DS5 with a single branch on plus instruction.

If DS5 is high, this data signals the beginning of a new display scan (i.e., an end of conversion has occurred.) The μP zeros its X index register, which will be used both to count the digits and to provide an offset for storing each digit in zero page memory. Register X is also stored in zero page memory at location XSTOR, since its contents will probably be lost upon returning from interrupt.

An early indication of an overrange condition can be obtained at this time. A bit mask, stored in memory, is used to test for the TSC7135's OVERRANGE output. If OR is high, the program branches to an error routine. An alternative for overrange testing is to wait until all digits have been scanned and then test bit 4 of any digit.

TSC7135 to 6502 μP Interface Program Flow Chart

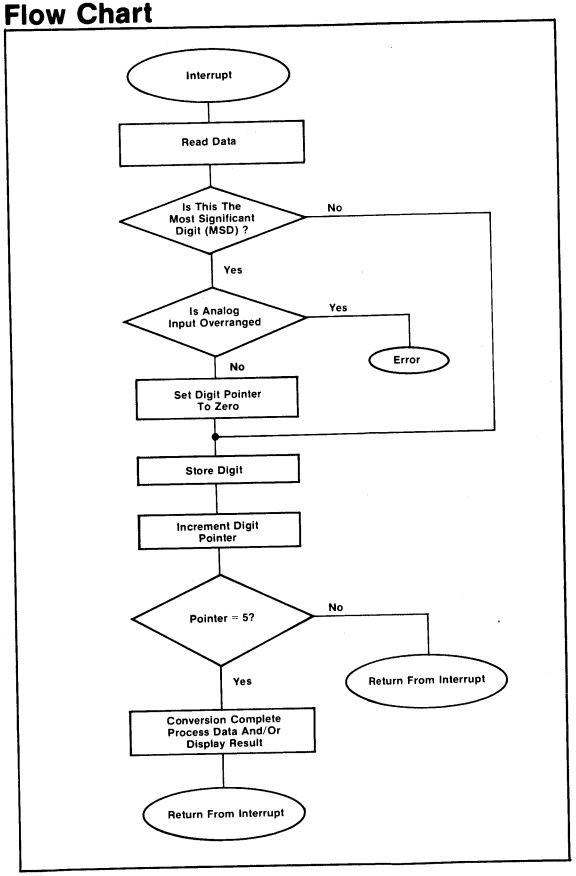


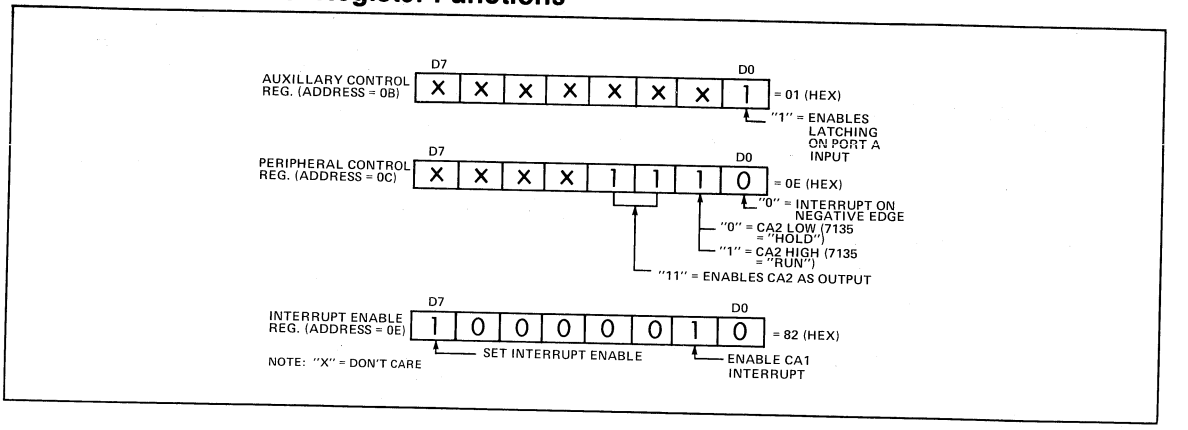
Figure 4

15

If DS5 is not high, or after register X is zeroed, program execution proceeds to location "NXTDIG". The BCD data is stored in zero page memory, beginning at location "DIGSTOR" and indexed by register X. After each digit is stored, register X is incremented and compared to five. If register X equals five, the digit scan is complete and data can be processed or displayed.

Register X less than five indicates the digit scan is not complete, so an RTI instruction returns operation to the main program to await another digit strobe. Other programs can use memory location XSTOR as a "Data Valid" indication: if XSTOR = 5, then 5 consecutive memory locations begining at DIGSTOR contain the results of the latest TSC7135 conversion.

6522 I/O Port Control Register Functions



TELEDYNE SEMICONDUCTOR

Application Note 17
Simplify A/D Converter Interface With Software

By Gary Grandbois & Wes Freeman

Integrating ADCs featuring BCD outputs for display interface offer a number of excellent features as well as high resolution at a very low cost. These advantages which include auto-zeroing, sign-magnitude coding, noise averaging and high impedance inputs are also attractive for microprocessor based systems. Unfortunately many of the display-oriented A/D converters are difficult to interface due to the multiplexed BCD format of the outputs. An exception to this problem is the 4 1/2 digit TSC7135 ADC which provides a "strobe" output.

This output allows the number of I/O port pins required to interface a 4 1/2 digit analog to digital converter chip to a microprocessor to be reduced from 15 lines (see ref.) to only 10 lines by counting the digit strobes in a software register. Besides freeing I/O pins for other applications, this method also results in slightly faster interrupt response because the μP does not have to loop while identifying each digit. Although the hardware and software shown are designed for the 8080, 8085 or Z-80, the same method can be applied to 6502 or 6800 I/O devices.

Interface Hardware

The complete TSC7135 to I8255A hardware interface is shown in Figure 1. The only digit strobe used is DS5 (the MSD), and the BUSY output is ignored. To understand why the other digit strobes are not required refer to the TSC7135 output timing diagram in Figure 2. The $\overline{\text{STROBE}}$ output goes low five times per conversion cycle. The first $\overline{\text{STROBE}}$ pulse occurs in the middle of DS5, when BCD data for the most significant digit is available on outputs B1-B8. $\overline{\text{STROBE}}$ also pulses LOW during the following DS4 through DS1 signals, after which $\overline{\text{STROBE}}$ remains high until the next conversion cycle. Therefore, only one $\overline{\text{STROBE}}$ pulse occurs for each digit select, and each $\overline{\text{STROBE}}$ corresponds to a BCD digit in MSD to LSD order. To read the A/D converter's data the μP simply reads BCD data during each $\overline{\text{STROBE}}$ pulse and stores that data in memory locations that correspond to the number of $\overline{\text{STROBE}}$ pulses received.

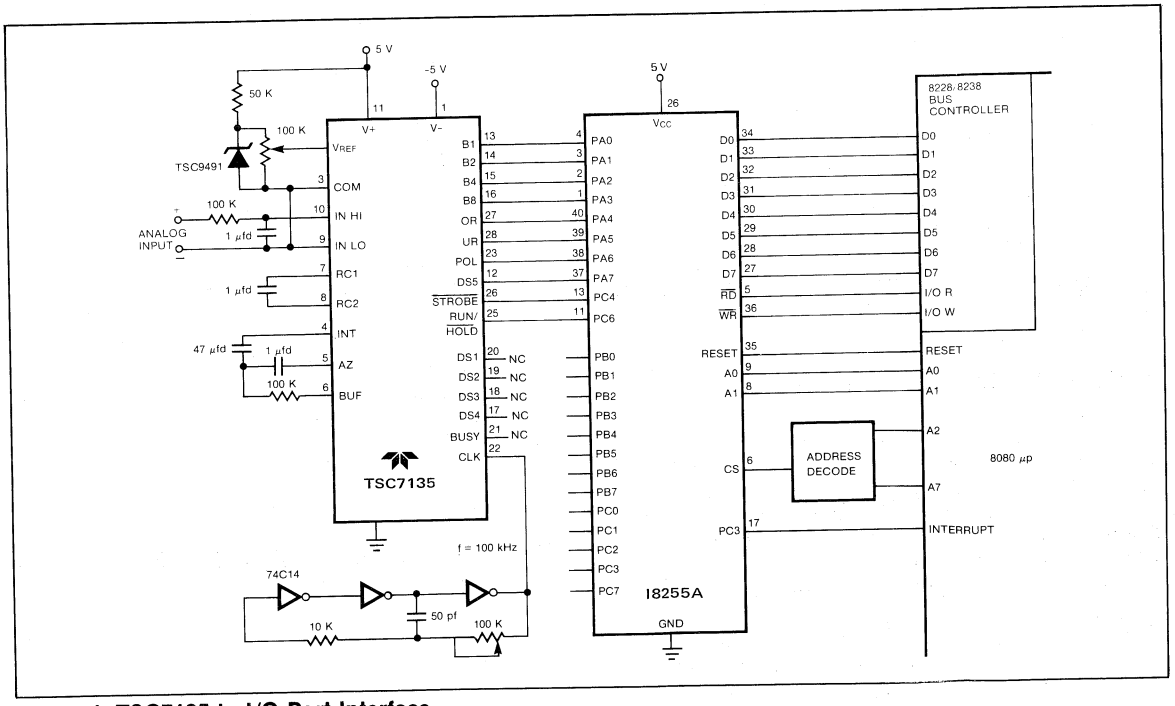


Figure 1: TSC7135 to I/O Port Interface

15

Synchronizing Data Transfer

The microprocessor must be able to identify an end-of-conversion, so that each digit will be stored in its proper location. Since the TSC7135 has a BUSY output, the processor could simply monitor this output for end-of-conversion status. However, this method would require an extra input bit, as well as processor time to test for BUSY status. By using software to identify the end-of-conversion, both software and hardware can be simplified.

In order to synchronize data transfer between μP and A/D converter, the μP tests the most significant bit of I/O port A for the presence of DIGIT STROBE 5(DS5). If DS5 is true then an end-of-conversion has occured. The data pointer is then initialized and assembly of five BCD digits begins. The next four $\overline{\text{STROBE}}$ pulses will find DS5 false, so the BCD digits are simply stored in successive memory locations. The fifth $\overline{\text{STROBE}}$ pulse signals an end of data transfer, so the user can display or manipulate the data as desired.

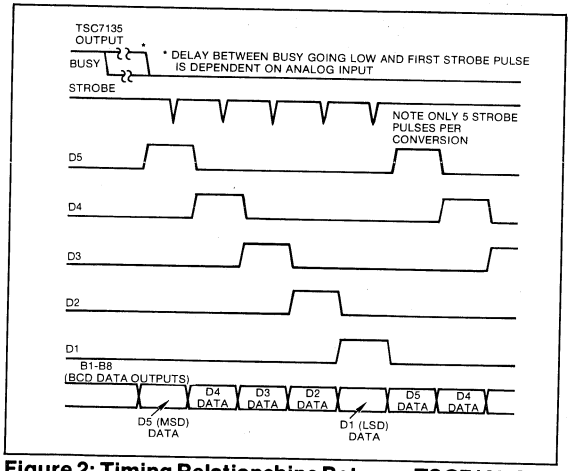


Figure 2: Timing Relationships Between TSC7135 Outputs

Initializing the I8255A I/0 Port

At power up, or after a microprocessor reset, the I8255A is initialized for unlatched (Mode 0) input operation. In order to interface to the TSC7135, the I8255A must be programmed to latch data, and generate an interrupt, from Port A (Mode I operation). In addition, one bit of Port C can be utilized for controlling the TSC7135's RUN/$\overline{\text{HOLD}}$ input, if conversions on command are required.

Programming the I8255A is accomplished by writing data to the control register. Figure 3 outlines the function of each control bit. Writing "0B2H" to the control register, for example, configures Port A as a latched input, Port B as a non-latched input, and remaining Port C bits as outputs.

In the Port A strobed input mode, bit PC3 becomes the interrupt output. In a large system with many interrupting devices, this output would typically go to a priority interrupt controller such as the I8259A. Smaller systems can simply use a single interrupt input, with polling in software to identify the source of the interrupt. To determine whether the TSC7135 has caused the interrupt in a polled system, Port A Input Buffer Full (IBFA) is tested for a HIGH state. If IBFA is high, then data has been latched into Port A by the TSC7135. Reading Port A will clear the interrupt and reset IBFA.

Programming Port A for strobed operation will define bit PC3 as an interrupt output, but a separate operation is required to enable the output. Bit PC4 is the interrupt enable bit for Port A. This bit must be set, using the Port C bit set/reset function, before the I8255A will respond to interrupts.

The circuit of Figure 1 also shows the TSC7135's RUN/$\overline{\text{HOLD}}$ input controlled by bit PC6. Setting PC6 high will result in continuous conversions. When PC6 is low, the TSC7135 will remain in its auto-zero cycle. If PC6 pulses high, the TSC7135 will perform a conversion, output the new data, and return to auto-zero.

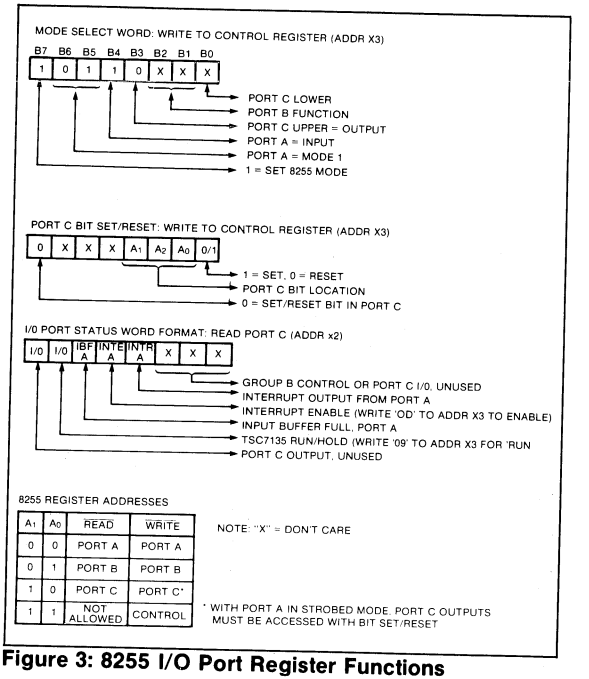


Figure 3: 8255 I/O Port Register Functions

Interface Software

Listing 1 contains software for acquiring data from the A/D converter. Two separate routines are required to program the I/O port and to respond to interrupts. Code at location "SETUP" will configure the I8255A for strobed input and enable Port A's interrupt.

The user must provide software for vectoring interrupts from port A of the 8255A to interrupt service routine "SVC." As mentioned previously, "SVC" will test for digit strobe 5 being high (i.e. beginning of a new digit scan). If DS5 is high then data pointer HL is loaded with the digit storage address.

If DS5 is not high, or after HL has been initialized, the BCD digits are stored in memory. If five digits have not been received, register HL is incremented to point to the next digit storage location. After five $\overline{\text{STROBE}}$ pulses, locations STORAG through STORAG +4 will contain five BCD digits that represent the latest TSC7135 conversion, plus sign, polarity, overrange, and underrange flags.

```
;TSC7135 TO 8255 I/O PORT INTERFACE SOFTWARE, WITH
;SIGN-MAGNITUDE TO 2'S COMPLEMENT CONVERSION
;
;
;CONFIGURE PORT A OF 8255 FOR STROBED INPUT AND
;ENABLE INTERRUPT FROM PORT A
;
;
I8255:  EQU     0               ;8255 I/O PORT ADDRESS
        ORG     2000H           ;CAN BE IN ROM OR RAM
SETUP   DI
        LD      A,0B2H          ;SET 8255A FOR LATCHED
        OUT     (I8255+3),A     ;  INPUT ON PORT A
        LD      A,0DH           ;ENABLE INTERRUPT FROM
        OUT     (I8255+3),A     ;  PORT A
        LD      A,09H           ;TURN ON TSC7135
        OUT     (I8255+3),A     ;  (RUN/HOLD='RUN')
        LD      HL,STOR         ;LOAD DATA POINTER WITH
        LD      (COUNTR),HL     ;  DATA STORE ADDRESS
        EI
        JP      MAINPR            ;JUMP TO USER PROGRAM OR
                                  ;  TO OPERATING SYSTEM
;
;
;
;INTERRUPT SERVICE ROUTINE---USER MUST
;PROVIDE HARDWARE/SOFTWARE TO VECTOR
;INTERRUPTS FROM THE 8255A TO THIS ROUTINE,
;AND PROVIDE FOR SAVING REGISTERS AS REQUIRED
;
;
SVC:    IN      A,(I8255)       ;GET TSC7135 DATA
        OR      A               ;SET FLAGS
        JP      P,NXTDG         ;DS5=0;NOT A NEW SCAN, GO ON
        LD      HL,STOR         ;NEW SCAN, SO SET DATA POINTR
        LD      (COUNTR),HL     ;  TO 1ST DIGIT STOR LOCATION
NXTDG:  LD      HL,(COUNTR)     ;LOAD STOR ADDR OF THIS DIGIT
        LD      (HL),A          ;STORE BCD DATA
        LD      A,L             ;GET LO BYTE OF STORE ADDR
        SUB     ENDSTR.MOD.256;SUBTRACT ENDING STOR ADDR-1
        JP      P,BCD2BI        ;DONE IF RESULT MINUS
        INC     HL              ;POINT TO NEXT ADDR
        LD      (COUNTR),HL     ;SAVE STORE ADDR
        RET                     ;RETURN TO MAIN PROG
;
;
;
;
```

Listing 1: TSC7135 to TSC8250 Interface Software

Converting Multiplexed BCD Numbers to 2's Complement Format

BCD data is very convenient for driving LED or LCD displays, but 2's complement format is usually preferred for computer arithmetic operations. Listing 2 is a program which will convert five BCD digits to 2's complement. This program multiplies the MSD by 10, adds the next digit, multiplies the sum again, etc., until all 5 digits have been converted. The sign bit is then tested and, if negative, a 2's complement adjustment (complement all data bits and add one) is performed. Finally, the 2's complement data is stored at location AD2SCM.

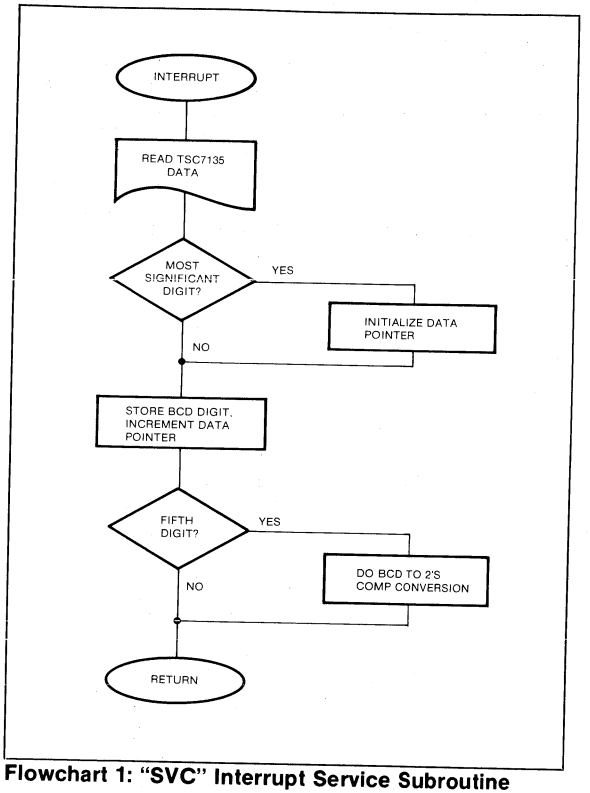
```
;
;BCD TO 2'S COMPLEMENT CONVERSION SOFTWARE
;THIS ROUTINE CONVERTS 5 BCD DIGITS LOCATED AT
;'STOR'    TO 2'S COMP AND STORES RESULT AT 'AD2SCM'
;
        ORG     2040H
BCD2BI: LD      HL,0000         ;ZERO HL REG
        LD      BC,STOR         ;POINT TO 1ST (MSD) BCD DIGIT
DIGIT:  LD      A,(BC)          ;GET DIGIT
        AND     0FH             ;MASK DS5,POL,OR,AND UR FLAGS
        LD      D,0             ;ZERO D
        LD      E,A             ;DIGIT TO E
        ADD     HL,DE           ;16 BIT ADD
        LD      A,C             ;LO BYTE OF DIGIT POINTER
        SUB     ENDSTR.MOD.256;COMPARE TO END; IF DONE,
        JP      P,DONE          ;  BC POINTS TO LAST DIGIT
        INC     BC              ;NOT DONE
        ADD     HL,HL           ;MULTIPLY HL BY 10;START
        PUSH    HL              ;  WITH HL*2; SAVE ON STACK
        ADD     HL,HL           ;    (HL*2)*2=HL*4
        ADD     HL,HL           ;      TIMES 2 AGAIN=HL*8
        POP     DE              ;       GET BACK HL*2
        ADD     HL,DE           ;         HL*8+HL*2=HL*10
        JP      DIGIT           ;NEXT BCD DIGIT
DONE:   LD      A,(BC)          ;BC STILL POINTS TO BCD DIGIT
        AND     40H             ;TEST 7135 POL -IF POSITIVE,
        JP      NZ,AD2CPL       ;  NO 2'S COMP CORRECTION REQ
        LD      A,H             ;RESULT NEG, SO DO A 2'S COMP
        CPL                     ;  CORRECTION BY COMPLEMENTING
        LD      H,A             ;    THE 15 BIT RESULT IN HL,
        LD      A,L             ;      AND COMPLEMENTING THE
        CPL                     ;        SIGN BIT
        LD      L,A             ;RESULT NOW IS 1'S COMP IN HL
        INC     HL              ;ADD ONE FOR 2'S COMPLEMENT
AD2CPL: LD      (AD2SCM),HL     ;STORE RESULT AND DONE
        RET
;
;
;RESERVE STORAGE FOR POINTER AND RESULTS
;
        ORG     0BFFCH          ;MUST BE LOCATED IN RAM
COUNTR: DEFS    2               ;STORAGE FOR DATA POINTER
STOR:   DEFS    5               ;STORAGE FOR 5 BCD DIGITS
ENDSTR: EQU     STOR+4
AD2SCM: DEFS    2               ;2'S COMPLEMENT DATA STOR
;
;
```

Listing 2: BCD to 2's Complement Conversion Software

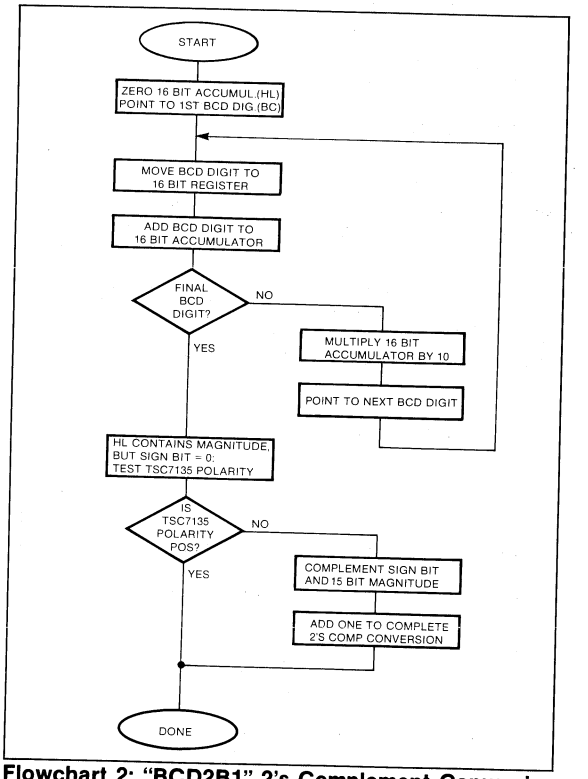
Reference:

Smith, M.F. Interface program links A/D chip with microprocessor *Electronics* Nov. 3, 1982 p. 124, 125

15



Flowchart 1: "SVC" Interrupt Service Subroutine



Flowchart 2: "BCD2B1" 2's Complement Conversion Subroutine

TELEDYNE SEMICONDUCTOR

Application Note 18
TSC7211AM/TSC7212AM Display Driver Microprocessor Interface

By Wes Freeman

TSC7211AM/TSC7212AM Microprocessor Interface

The TSC7211AM and TSC7212AM are complete CMOS four-digit display drivers which greatly simplify microprocessor display interfaces. The devices contain data latches, BCD to seven-segment decoders, and either back plane and segment drivers for liquid crystal displays (TSC7211AM) or current controlled outputs for LEDs (TSC7212AM). This application note describes interfacing these display drivers to popular microprocessors.

TSC7211AM/TSC7212AM μP Interface Inputs

The TSC7211AM and TSC7212AM need only eight inputs to transfer data from a μP to the display. Inputs are divided into four data inputs, two address inputs, and two chip selects. Input timing relationships are shown in Figure 1.

BCD data for display is entered on inputs B0(LSB) through B3(MSB). Data inputs from 0000B through 1001B are decoded to correct seven-segment representation, while data inputs from 1010B to 1110B are decoded to "—," "E," "L," "P," and "H" respectively. An input of 1111B results in a blank display, which permits either individual digits or the entire display to be blanked under software control without external hardware.

The digit select inputs (DS1 and DS2) select the digit written to when the chip select inputs become active. Normally DS1 and DS2 are connected to the low-order bits (A0 and A1, respectively) of the microprocessor address bus. The DS1 and DS2 inputs must meet the same setup-and-hold-time limits as the data inputs.

Chip select inputs $\overline{CS1}$ and $\overline{CS2}$ control data entry into the TSC7211AM/TSC7212AM. The two chip selects are interchangeable, since they are logically "ORed" internally. In a typical application one chip select input connects to the READ/WRITE control line and the other chip select will connect to an address decoder. If only one chip select is required the remaining input should be tied to GND.

Microprocessor Bus Interfaces

Microprocessor bus structures can roughly be divided into two groups: the 6800-type, where data is guaranteed valid on a clock edge, and the 8080-type, where data is stable for the duration of a WRITE pulse. Since the TSC7211AM and TSC7212AM are specified in terms of data setup-and-hold-times, either processor type is easily accommodated.

The 6800-type edge activated I/O is used on several popular microprocessors, such as the 8048, 8085, 6809 and 6502. A timing diagram for the 6502 is shown in Figure 2, and a typical 6502 to TSC7211AM interface is shown in Figure 3. To transfer data to the display simply write data to the appropriate memory location.

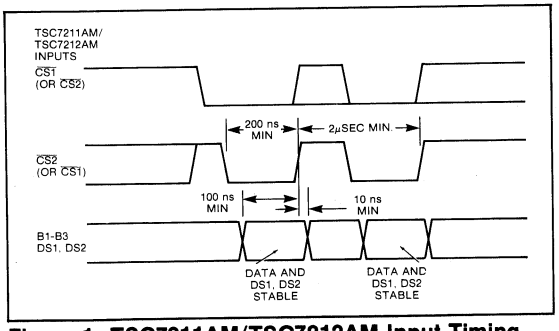


Figure 1. TSC7211AM/TSC7212AM Input Timing Diagram

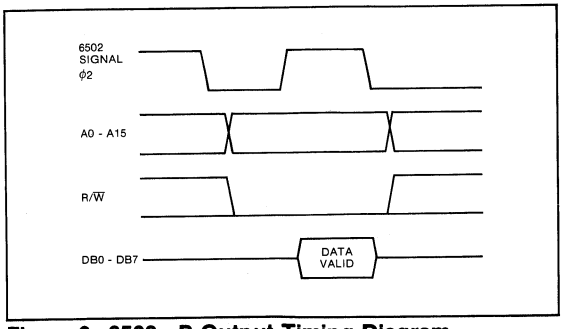


Figure 2. 6502 μP Output Timing Diagram

15

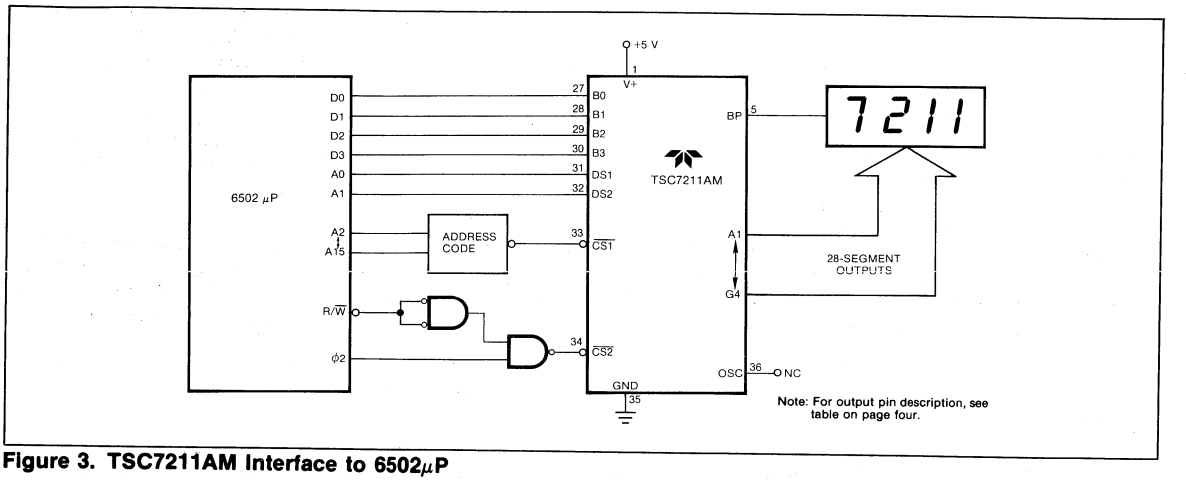


Figure 3. TSC7211AM Interface to 6502μP

The 8080 bus characteristics, shown in Figure 4, are shared by the Z-80, NSC800 and 8086, among others. A typical 8080 to TSC7212AM interface is shown in Figure 5, where the TSC7212AM is accessed as four I/O port locations. The 8080 can also treat the TSC7212AM as memory, in which case the full range of memory reference instructions can be used to transfer data to the display.

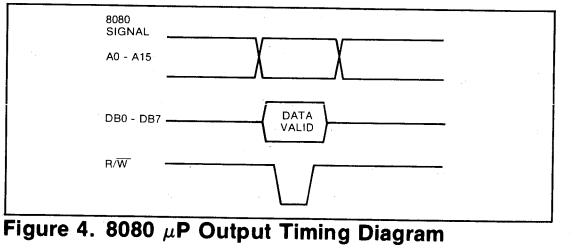


Figure 4. 8080 μP Output Timing Diagram

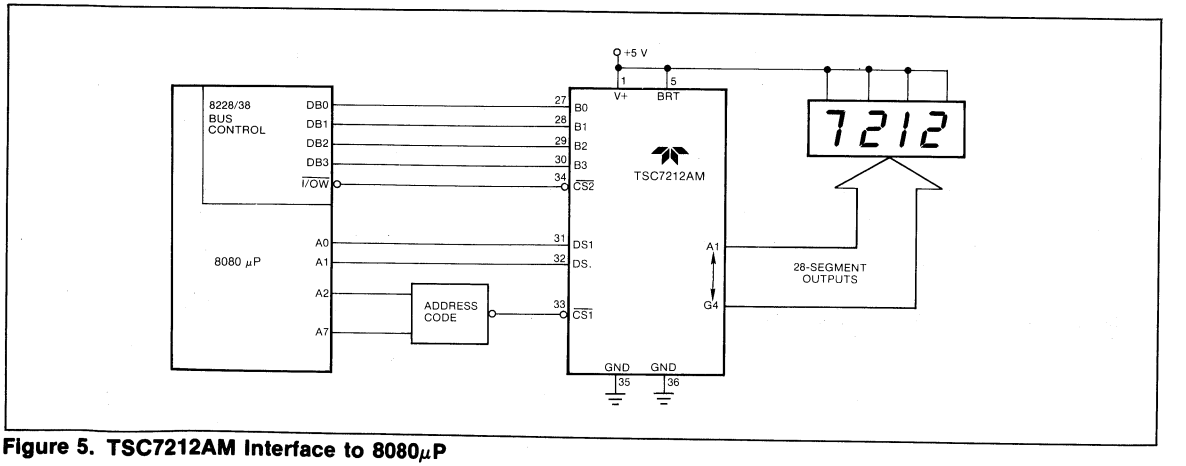


Figure 5. TSC7212AM Interface to 8080μP

Interfacing to Multiple LCD Displays

LCD displays will be damaged if the display driver causes a DC voltage between the backplane and segment inputs. Therefore, display driver outputs must be synchronized if more than one driver is used with a display. The TSC7211AM backplane outputs can be slaved together, permitting large LCD displays to be driven.

Figure 6, for example, shows three TSC7211AMs driving two six-digit LCD displays to produce a date/time display in MM:DD:YY, HH:MM:SS format. Since the backplane outputs are synchronized, each display can be driven by two separate TSC7211AMs without any display degradation. The processor shown is a Z-80, and the displays are accessed as twelve I/O port locations beginning at address 80H.

The Z-80 indirect output instruction (OUTI) efficiently transfers data from a twelve-byte buffer in memory to three TSC7211AMs. The OUTI instruction transfers the byte data addressed by registers H & L to the output port addressed by reg C, then increments register HL and decrements the buffer count register B. A typical output routine is:

```
Transfer   LD   C,7FH          ; 1st I/O address - 1
           LD   HL,
                Buffer Address ; 1st byte of data
           LD   B, 12          ; Transfer 12 bytes
Loop1      INC  C              ; Point to next I/O address
           OUTI                ; Output byte; inc HL; dec B
           JR   NZ, Loop1      ; Next byte unless B = 0
```

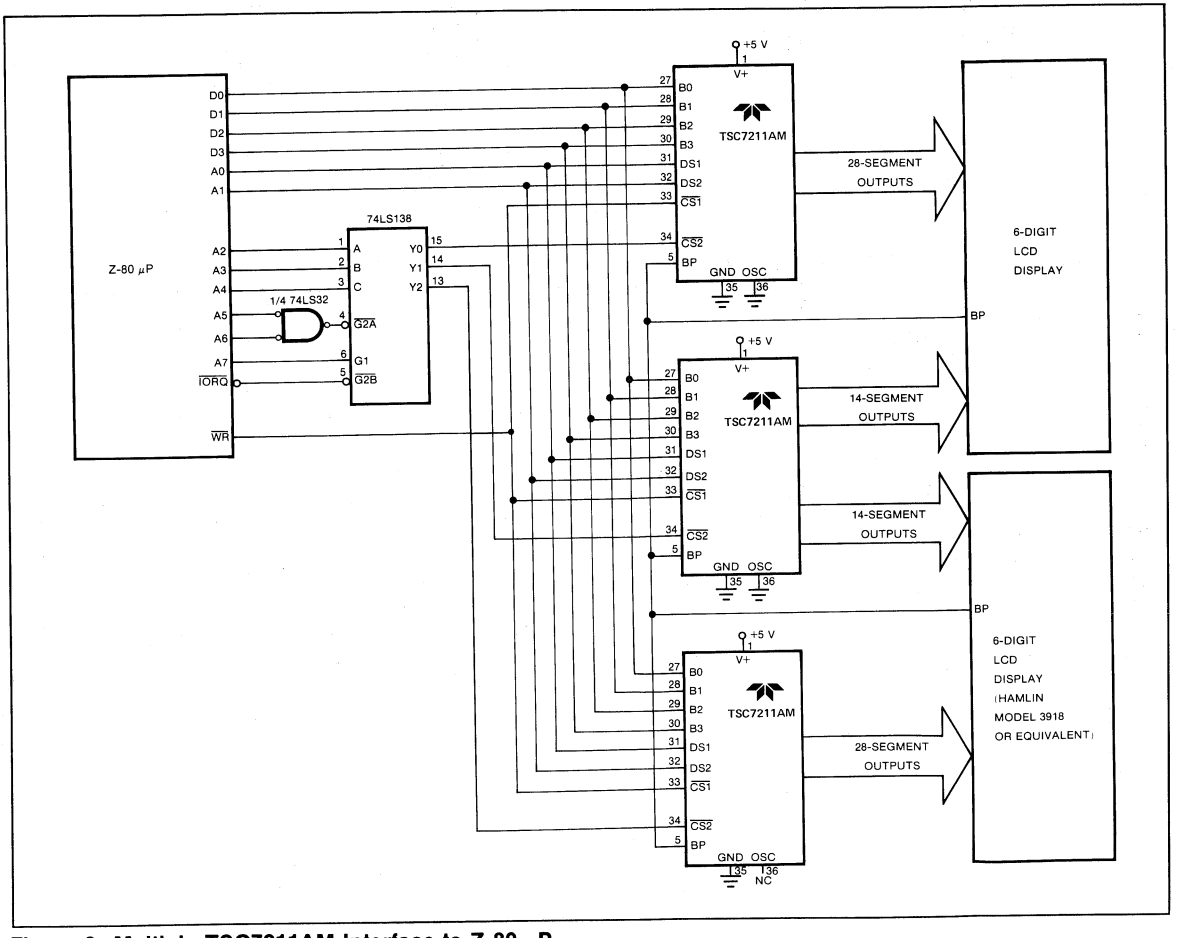
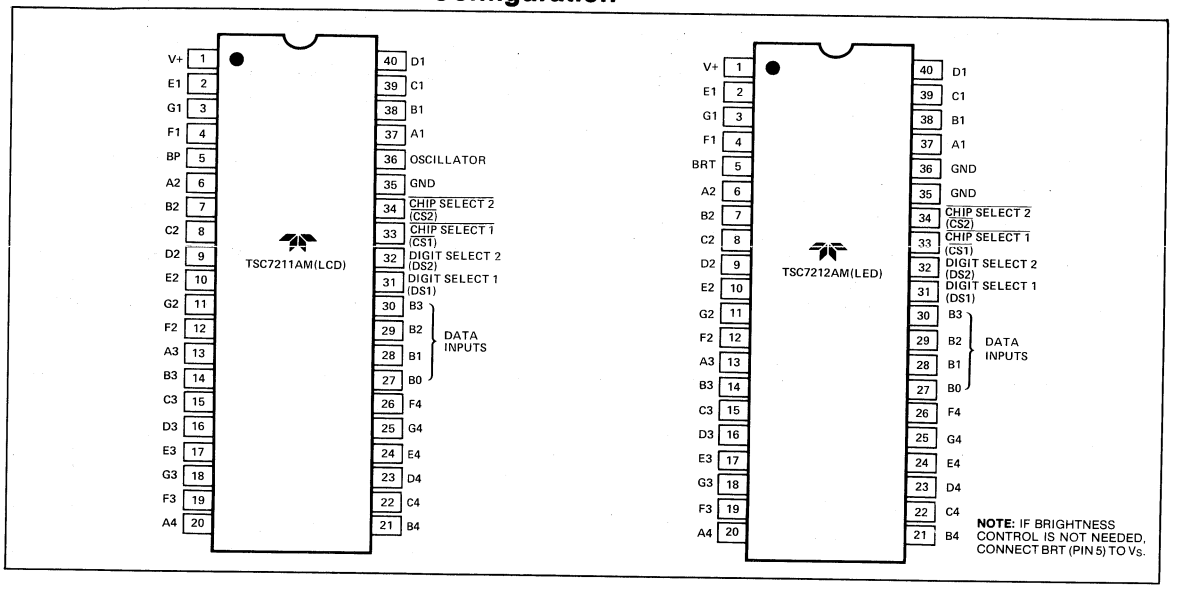


Figure 6. Multiple TSC7211AM Interface to Z-80 μP

TSC7211AM/TSC7212AM Pin Configuration



Output Pin Description and Function

OUTPUT	TERMINAL		FUNCTION	OUTPUT	TERMINAL		FUNCTION
A1	37	A	Segment Dr. Digit 1 (LSD)	A3	13	A	Segment Dr. Digit 3
B1	38	B		B3	14	B	
C1	39	C		C3	15	C	
D1	40	D		D3	16	D	
E1	2	E		E3	17	E	
F1	4	F		F3	19	F	
G1	3	G		G3	18	G	
A2	6	A	Segment Dr. Digit 2	A4	20	A	Segment Dr. Digit 4 (MSD)
B2	7	B		B4	21	B	
C2	8	C		C4	22	C	
D2	9	D		D4	23	D	
E2	10	E		E4	24	E	
F2	12	F		F4	26	F	
G2	11	G		G4	25	G	

Application Note 19
BCD Analog-to-Digital Converter Interface to Dot Matrix LEDs
By David Gillooly

Traditionally 3 1/2 digit analog-to-digital converters have interfaced to seven segment LED or LCD displays. Converters like the TSC7106A, TSC7126A and TSC7107A contain decoder/driver circuits to directly drive seven segment displays. Devices like the TSC14433A and 4 1/2 digit TSC7135 offer users greater flexibility since decoder/drivers are not contained on-chip. Output data is in a multiplexed BCD format. Information can be displayed on LED, LCD, vacuum fluorescent or incandescent displays as the application and environment require. Information can simultaneously be transferred to a microprocessor.

The output data latching, decoding, and drive functions for BCD output converters,however, require external MSI devices such as the TSC700A, TSC7211A or MC14543/1413. The devices are inexpensive but do require additional board space.

In measurement applications where high reliability, small size and excellent readability are needed, the Hewlett Packard #5082-7356 dot matrix LEDs may be used. Within the LCD case is an integrated circuit display latch, decoder and driver. The numeric display font matches the style used in alphanumeric dot matrix indicators. Instrument front panels can be designed without resorting to mixed font styles. The LEDs have operating ranges from -20° C to +85° C. The family contains parts with -55° C to +100° C operating temperature range. When matched with similarly specified converters a very reliable, compact measurement and display module can be constructed for industrial and military applications.

A typical dot matrix LED interface is shown in Figure 1. The three LSD LEDs each contain a decoder, latch and driver. The one-half Digit MSD has only LEDs; two 4013 latches hold positive polarity information and the "1" MSD data. The TSC14433A encodes polarity information in the MSD BCD output as shown in Table 1.

In an overrange condition the data to the three LSDs is forced to all 1's through the 7432 OR gates. The HP#5082-7356 LED display blanks when an all 1's input is decoded. This added feature is at no additional cost since the gates are required as buffers to provide logic input drive to the LEDs. The MSD and sign bits are active in an overrange condition.

A slight modification (Figure 2) causes the three LSD displays to "blink" ON and OFF for overrange analog inputs. The overrange bit (OR) remains low until an in range conversion completes. With OR = O the Blink FF set is removed. The end-of-conversion (EOC) clock causes the display to blink at one-half the conversion rate. This visual blinking indicates more forcefully a measurement channel has overranged. Each display also contains a decimal point for range formatting.

Table 1: Half Digit And Polarity Coding

Coded MSD	Data			
	Q3	Q2	Q1	Q0
+0	1	1	1	0
-0	1	0	1	0
+0 UR	1	1	1	1
-0 UR	1	0	1	1
+1	0	1	0	0
-1	0	0	0	0
+1 OR	0	1	1	1
-1 OR	0	0	1	1

Notes
1. Q3- 1/2 digit, low for "1", high for "0"
2. Q2- Polarity: "1" = positive, "0" = negative
3. Q0- Out of range condition exists if Q0 = 1. When used in conjunction with Q3 the type of out of range condition is indicated, i.e. Q3=0➤OR or Q3=1➤UR.

15

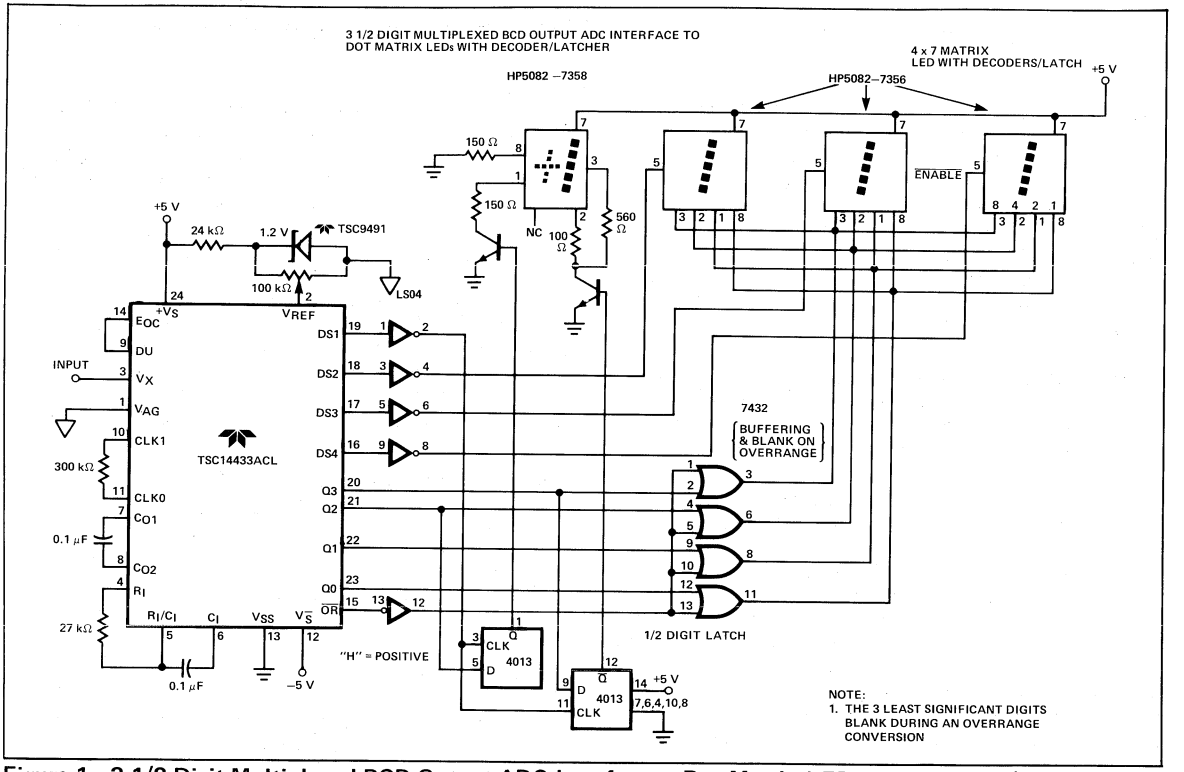


Figure 1: 3 1/2 Digit Multiplexed BCD Output ADC Interface to Dot Matrix LEDs with Decoder/Latches

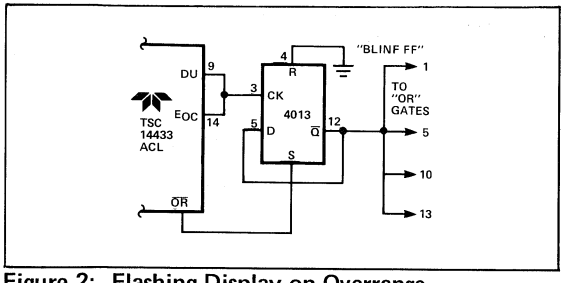


Figure 2: Flashing Display on Overrange

TELEDYNE SEMICONDUCTOR

Application Note 20
Two-Digit Serial Input LED Display Driver Using TSC9404

By David Gillooly

Many system applications require microprocessors to display data on seven segment light emitting diode (LED) displays. To minimize the number of input/output lines needed, a serial to parallel data bit conversion scheme can be used. The TSC9404 will perform a serial to 16-bit parallel output conversion. The TSC9404 outputs will each sink 60 mA @ $V_{SAT} \leq 0.5$ V for directly driving the LED displays.

The sixteen outputs will drive two seven segment displays plus two decimal points or annunciators. A serial output allows devices to be cascaded for more digits. Two digits, however, are adequate for many event, switch position, percentage and temperature display applications.

A basic two digit display circuit is shown in Figure 1. The TSC9404 interfaces with a standard 6522 Versatile Interface Adapter (VIA) I/O chip. The 6522 communicates with a 6502 microprocessor. The VIA chip is widely used since it contains two configurable I/O ports, and timers. It also contains an 8-bit serial input/output shift register. The VIA shift register is configured as an output with the shift rate set by the phase 2 system clock. Data latches are not needed on the TSC9404 as the high speed data transfer is transparent to the eye. Two output shift operations will fill the TSC9404 with data for display.

Program operation is straight forward. (See program listing) The eight least significant data bits are loaded first from memory into the VIA shift register. The appropriate binary to seven segment display code is obtained through a table look-up (Table 1) procedure. The number stored in memory is the table offset. Hex or special symbol display characters are possible by expanding the table. The VIA automatically shifts eight data bits to the TSC9404. The program waits for a complete 8-bit transfer before obtaining the most significant digit data from memory. The wait state is implemented by testing the interrupt register shift complete flag bit with the shift register interrupt disabled. A memory map for the 6522 is shown in Table 2. The program/system was developed on a SYM-01 microcomputer board.

If decimal point drive is desirable the program is easily modified:

```
LDA    Table, X
ORA    LSBDP; Add #01 for decimal point
STA    SR
LDA    Table, X
ORA    MSBDP; Add #01 for decimal point
STA    SR
```

Similar programming techniques can be developed for alpha-numeric display using 14 or 16 segment LEDs. Bar graph displays are also possible.

Table 1: Decimal to Seven Segment Conversion Table

Displayed Character	LED Segment a b c d e f g DP	HEX Equivalent *
0	1 1 1 1 1 1 1 0	FC
1	0 1 1 0 0 0 0 0	60
2	1 1 0 1 1 0 1 0	DA
3	1 1 1 1 0 0 1 0	F2
4	0 1 1 0 0 1 1 0	66
5	1 0 1 1 0 1 1 0	B6
6	1 0 1 1 1 1 1 0	BE
7	1 1 1 0 0 0 0 0	E0
8	1 1 1 1 1 1 1 0	FE
9	1 1 1 0 0 1 1 0	E6
"BLANK"	0 0 0 0 0 0 0 0	00

* For decimal point add 01 to HEX code

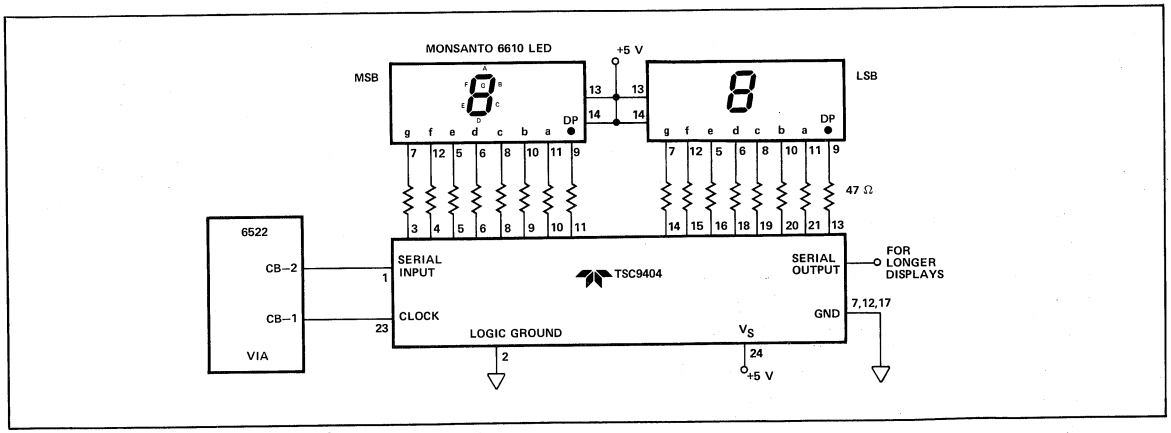


Figure 1: High Current Serial I/O Port Expander

15

Serial I/O Port Expander; Two Digit, Seven Segment LED Drive Program Listing

	Instructions						
Address	Byte 1	Byte 2	Byte 3	Label	Mnemonic	Operand	Comments
200	A9	18		Display	LDA	#18	
202	8D	OB	A8		STA	ACR	; Shift out under 2 Control
205	A9	80			LDA	#80	
207	8D	OE	A8		STA	IER	; Disable shift register Interrupt
20A	AE	50	03		LDX	LSB	
20D	BD	00	03		LDA	Table,X	; Convert LSB decimal digit to seven segment code
210	8D	OA	A8		STA	SR	; Send LSB to shift register
213	AD	OD	A8	LSBTST	LDA	IFR	; Load shift register flag
216	29	04			AND	MASK	
218	FO	F8			BEQ	LSBTST	; Test for LSB shift completion
21A	AE	51	03		LDX	MSB	
21D	BD	00	03		LDA	Table,X	; Convert MSB decimal digit to seven segment code
220	8D	OA	A8		STA	SR	; Send MSB to shift register
223	AD	OD	A8	MSBTST	LDA	IFR	; Load shift register flag
226	29	04			AND	MASK	
228	FO	F8			BEQ	MSBTST	; Test for MSB shift completion
22A	60				RTS		; Return from subroutine
300	FC			Table		FC	; Seven segment code 0
301	60					60	; 1
302	DA					DA	; 2
303	F2					F2	; 3
304	66					66	; 4
305	B6					B6	; 5
306	BE					BE	; 6
307	EO					EO	; 7
308	FE					FE	; 8
309	E6					E6	; 9
30A	00					00	; Blank

Table 2: 6522 (VIA) Memory Map

Address(Hex) *	Register
A80E	IER - Interrupt Enable Register
A80D	IFR - Interrupt Flag Register
A80B	ACR - Auxiliary Control Register
A80A	SR - 8-Bit Shift Register

U28 On SYM-01 Single Board Computer

Application Brief 1 Combining HiNIL and CMOS — an Optimum Design Technique

The growing interest in CMOS logic and its increasing popularity have brought about a new awareness of power dissipation and noise immunity among designers of electronic systems. The popularity of the 4000 series and the 74C series of CMOS Logic offers the system designer several important advantages—standardized input/output characteristics and TTL pin and function equivalence. Of particular interest to designers of industrial controls systems and other circuitry where electrical noise presents a major problem is the ability of CMOS to interface with bipolar high noise immunity logic elements (HiNIL).

The 4000 series and 74C series can easily interface with Teledyne's HiNIL family as shown in Figure 1. The result is a system which has greater noise immunity and has drive capability to interface with lamps, relays and displays, yet the system retains the advantages of CMOS—low power dissipation, moderate speed and complexity, and operation over wide operating supply voltages.

HiNIL devices are designed to operate from 10.5 volts to 16.5 volts, which is well within the 3-18 volt operating range for CMOS. In addition, this voltage is compatible with popular linear IC's and other analog circuits, eliminating the need for extra power supply voltages. Thus, a single inexpensive supply with little regulation can be used to power the system.

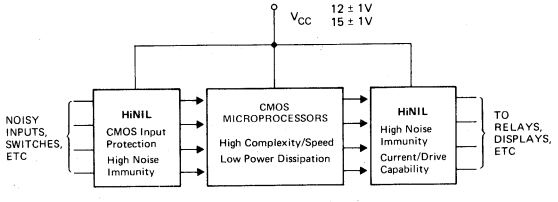


Fig. 1. Optimum System Design Approach

A review of dc noise margin characteristics bears out the increased noise immunity advantages obtained when using HiNIL as an input port (Figure 2).

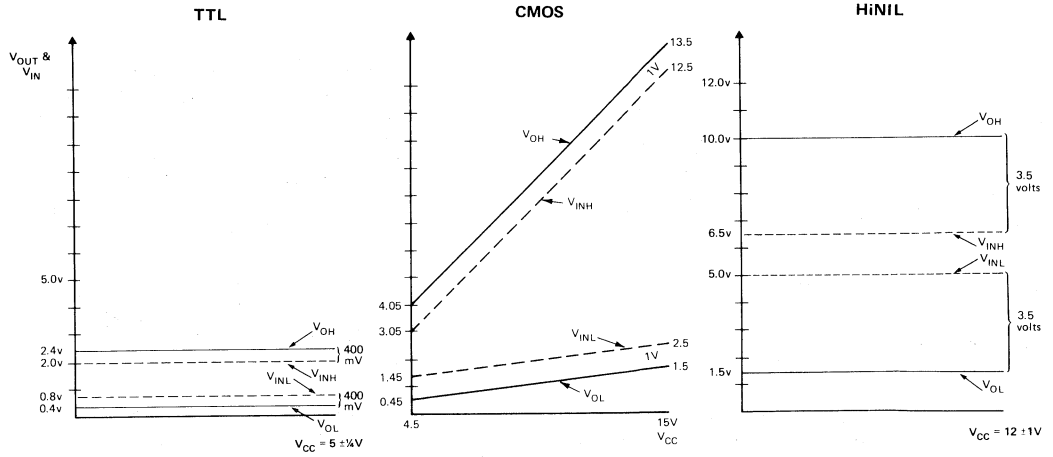


Fig. 2. DC Noise Margins

15

In addition to dc noise margin, there is an AC noise immunity factor to be considered, related to device propagation delay, output impedance and dc noise margin. AC noise immunity reflects susceptibility to errors caused by noise transients or spikes.

The electrical model for a gate driving a gate (or any logic device) in a noisy environment (where noise is capacitively coupled on a line) is shown in Figure 3 with its equivalent RC circuit.

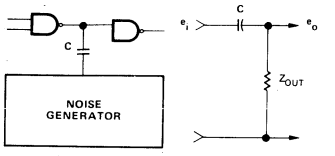


Fig. 3. Electrical Noise Model

The output impedance (Z_{OUT}) of the device determines how quickly any noise charge coupled onto the line can be discharged through the output resistor—the lower the output impedance, the faster the noise charge is leaked off.

The propagation delay of the logic gate determines what magnitude spike will be recognized by the output as a logic transition. The results of ac noise immunity tests conducted on CMOS, TTL and HiNIL logic devices are presented in Figure 4.

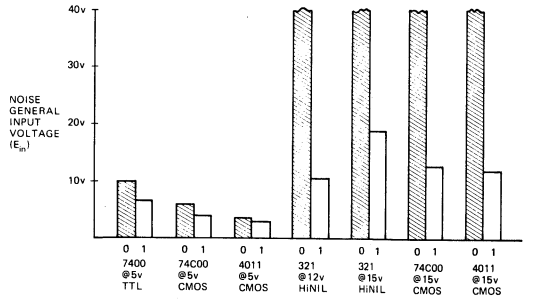


Fig. 4. Noise Immunity Test Results C = 500pf

Test results shown were run with a frequency generator of 100 Khz and a coupling capacitor of 500 pf. The noise generator voltage was increased slowly until a logic error was generated. HiNIL with its 3.5 volts of guaranteed dc noise immunity clearly offers the highest noise immunity available in a standard logic device.

Combining HiNIL with CMOS in a system design significantly reduces power dissipation in comparison to a system utilizing only bipolar technologies. Consider the following power reduction factors for conversion (quiescent state):

Conversion	Power Reduction Factor
LPTTL to CMOS	1000
TTL to CMOS	10,000
HiNIL to CMOS	50,000–100,000

For design flexibility, ease of interface to peripheral devices, low cost and optimum system performance, the HiNIL/CMOS design approach makes sense for particularly noisy environments.

The major considerations in interfacing logic families are to maintain proper voltage levels and to have compatible current sinking characteristics. The various HiNIL/CMOS interfacing schemes are shown in Figures 5, 6 and 7.

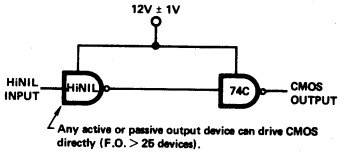


Fig. 5. HiNIL/CMOS Interface

HiNIL devices have the proper voltage characteristics to operate with CMOS directly, and HiNIL's current sinking and drive capability enable a fan-out of more than 25 devices (Fig. 5).

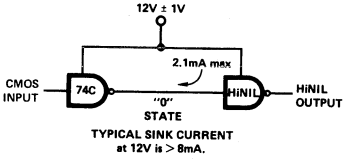


Fig. 6. CMOS/HiNIL Interface

A CMOS gate (74C) has no problem sourcing the 10μA max. leakage of the HiNIL input diode in the "1" state. (Fig. 6.) The only real concern in driving HiNIL is the ability of CMOS to sink the 2.1mA max. current in the "0" state. 74C can sink this current directly without resorting to a parallel gate combination. Other CMOS types may require an auxilliary transistor to boost the input level (Fig. 7).

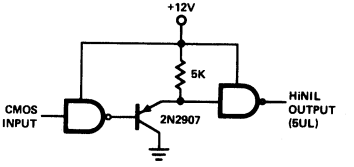


Fig. 7. CMOS Output Booster

Following are some specific situations where CMOS and HiNIL can be utilized to optimize a system design.

Parasitic SCR latch-up is a common CMOS malfunction. Large noise transients and DC input levels below ground or above V_{CC} force CMOS input diodes into forward conduction, causing SCR action in the four-layer diodes formed by the diode and parasitic p-n substrate junctions. This condition leads to device latch-up, increased I_{CC} current and, when

current is not limited, to gate destruction (Figure 8). Maximum protection can be obtained by using a HiNIL Schmitt trigger.

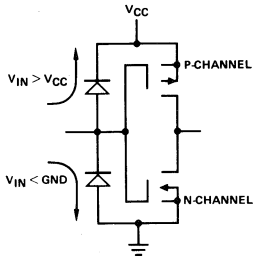


Fig. 8. CMOS Latch-Up Causes

This device has been designed as a universal input port for a receiver or for a contact bounce eliminator (see HiNIL 367/368 data sheet for details). The basic feature of the Schmitt trigger—2.5 volts hysteresis and latching output (no open circuit recognized)—provide the system designer with a unique opportunity to fight noise at its worst point—the system inputs. The 367/368 also features slow-down capacitor capability to ignore voltage spikes of up to 100 volts for up to 1 μsec, making it attractive for applications where high voltage input protection is required or in applications where static charge pulses cause logic errors, such as in CRT display electronic games, slot machines, xerographic copies, machine controls—any place where switches are decoded (Figure 9).

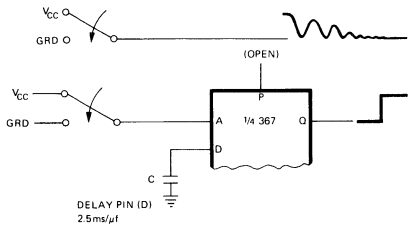


Fig. 9. 367 Schmitt Trigger Switch Contact Bounce Eliminator

One of the shortcomings of the CMOS technology is in its current handling characteristics for driving relays, lamps and displays. The HiNIL family provides devices capable of driving these peripherals, and it complements the low power and moderate speed of the CMOS subsystem. An example of a CMOS/HiNIL interface to drive a small relay or lamp is shown in Figure 10.

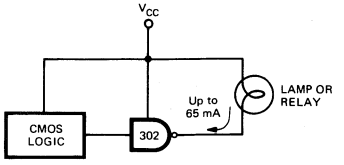


Fig. 10. Lamp/Relay Interface

Another example is an industrial controller using LED displays. The HiNIL 383 decoder/driver can sink 20 mA dc (40 mA @ 50% duty cycle) and is compatible with Monsanto Man-1, Man-7 type displays. The 383 is a pin and function replacement for the 7447 TTL decoder/driver, eliminating the need for a 5 volt supply requiring ±¼V regulation (Figure 11).

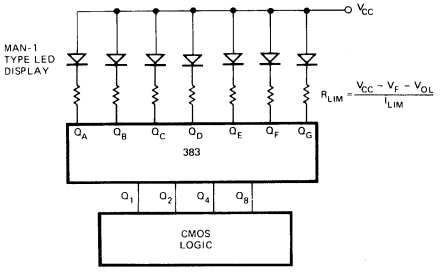


Fig. 11. LED Display Circuit

The creative system designer no doubt can discover many other applications using the complementary aspects of HiNIL and CMOS to optimize system performance and gain advantages from both logic families—increased noise immunity, reduced power dissipation, and elimination of expensive regulated power supplies.

15

Application Brief 2
Protecting Logic Inputs
By David Guzeman

Industrial logic applications, by their very nature, tend to be rough on the integrated circuits used in the system. While the circuits buried in the system several logic levels deep are adequately protected from high voltage transients, those that have inputs leading to the "outside world" may be exposed to extremely high voltage spikes. The input diodes of HiNIL circuits have typical breakdown voltages in the 30-40 V region. Unfortunately, spikes on long lines can exceed 100 V for very short times. These spikes are of sufficient energy to blow the input diodes on integrated circuits, even those in HiNIL inputs.

Logic inputs tied to lines leaving the logic system are particularly susceptible to high voltage spikes. See Figure 1. This situation commonly occurs when logic inputs are tied to microswitches through long lines, sometimes longer than 10 feet. No systems designer would ever consider tying logic systems ten feet apart together without the use of line drivers and line receivers. The assumption is made that since the logic input is tied to a switch, no line driver or line receiver is needed. While this assumption is correct, too frequently is that same input left unprotected from transients even though that long line acts as a perfect antenna.

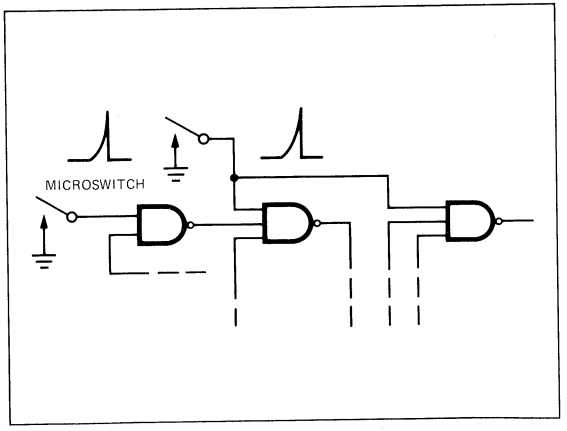


Fig. 1. Spikes on logic inputs can cause permanent damage.

One form of protection is to place a high breakdown diode in series with the input. See Figure 2. In this configuration the breakdown voltage of the diode (which may be chosen as high as 200-300 V) offers ample protection against positive going spikes.

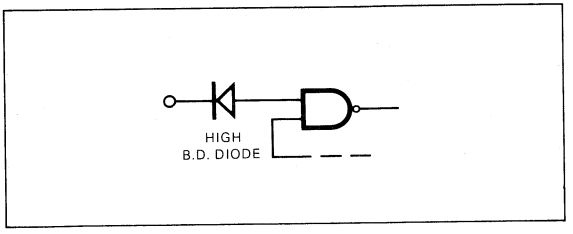


Fig. 2. (Using a series diode for protection)

A better technique is to clamp the input to V_{CC} with a diode. See Figure 3. This approach allows the use of inexpensive low breakdown voltage diodes. As a positive going spike reaches an amplitude of V_{CC} +0.7 V the diode forward biases and clamps the input. This diode should be reasonably fast, like a 1N914 or a 1N4148, and should be as close as possible to the IC.

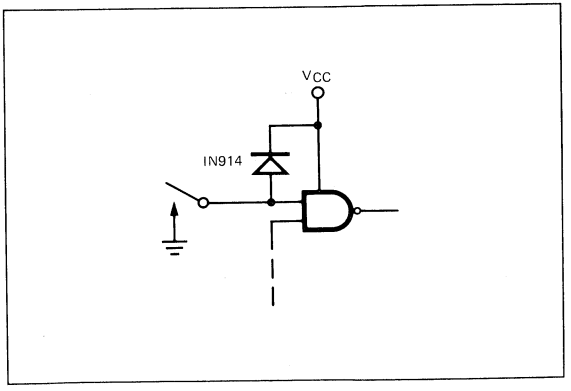


Fig. 3. (Using a clamp diode for protection)

15

Further protection is achieved by putting a 1 kΩ resistor in series with the protected lead. See Figure 4. This serves to limit the surge current (100 mA for a 100 V spike). In the event that further protection is desired, a capacitor tied from the input to ground serves as an ac voltage divider that will shunt fast spikes to ground. With the values given in Figure 5, the input will be protected against 1 μs pulses of 1000 V amplitude.

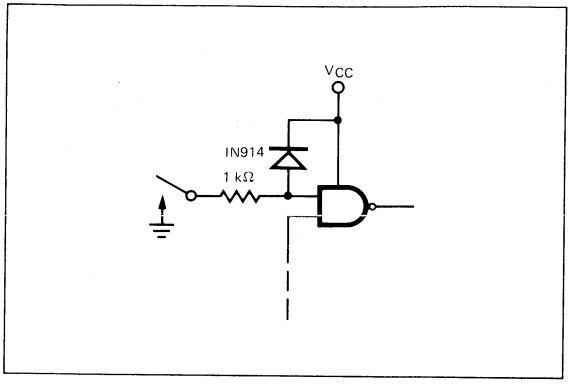


Fig. 4.

In this entire discussion, no mention has been made of negative going spikes. Actually the circuit shown in Figure 5 functions as well for negative going spikes as for positive going spikes. This is because there is already a diode from each input to ground that is "built in" to the device at the time of fabrication. These diodes, normally reverse-biased, play no part in the normal operation of the device and are seldom shown on the data sheet schematic. Any negative spike on the input forward biases the internal diodes which shunt the spike to ground and hence protect the input diodes. Thus the configuration of Figure 5 actually protects the inputs against both positive and negative 1000 V spikes.

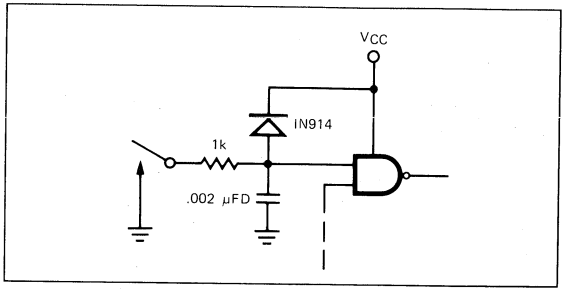


Fig. 5.

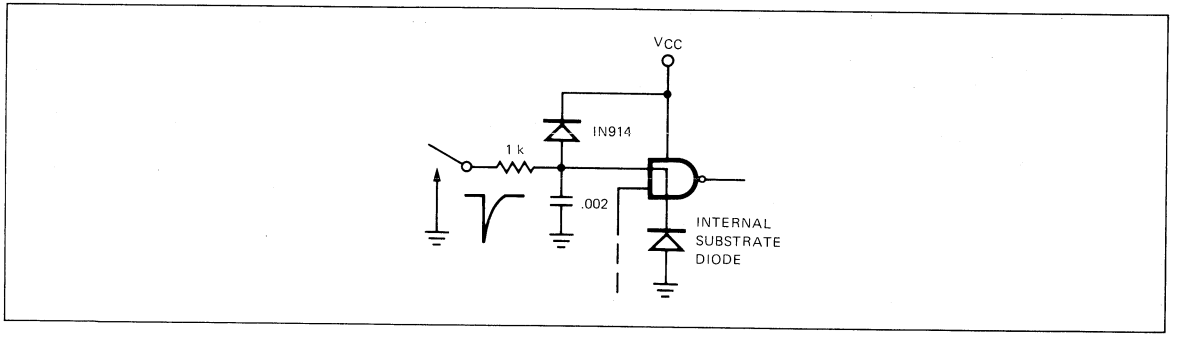


Fig. 6

TELEDYNE SEMICONDUCTOR

Application Brief 3
The 355 Timer Solves Noise Problem
By Robert MacIntyre

Since the advent of the IC Timer, semiconductor applications Engineer's have been swamped by complaints of malfunctions. Generally, the accused culprit is a counter or other array of flip-flops. Most complaints come from users building industrial or commercial controls — particularly those using CMOS or HiNIL for noise immunity.

After a bit of detective work, it is discovered that the real culprit is the Timer being used as a clock generator. Every time the output of a 555 type of circuit switches high, a large current spike is generated. This is not surprising to TTL users who are concerned with high speed operation and are accustomed to looking for problems that show up only briefly. It is fairly well known among computer logic and computer power supply designers that the totem pole output virtually shorts out the supply during the switching transient. It is therefore standard practice to utilize a well regulated and well filtered 5V power supply for these applications.

But CMOS and HiNIL are not supposed to require tight regulation and heavy filtering. Part of the rationale is a cost savings in the power supply; besides industrial systems run at slow speeds and the logic used is not the fastest in the world and does not have the current generating output stage of TTL. The designer of such a system is genuinely surprised when he finds out that his "faulty" counter is only faulty because of a 300 milliamp current spike on the supply line which is only there for 200 nanoseconds. See Figure 1 (upper waveform). The spike at the trailing edge of the output pulse is lower, but still is about 50 mA.

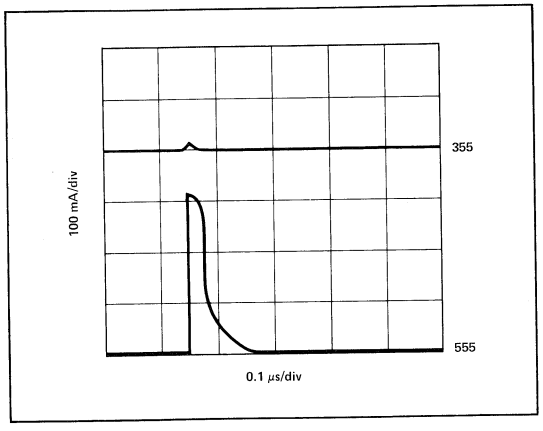


Fig. 1.

This is the most common applications problem encountered by the Timer user. The current spike drags down the supply and the flip flops no longer have a decent amount of feedback to maintain their stability, so some of them change state — sometimes! The designer trying to figure out what's happening may not think of looking for 200 nanosecond spikes in his "slow" system.

There are also a couple of other potential problems with the popular Timer. One of them is the reset function. The threshold on the reset is specified at 400 mV minimum and most run pretty close to that limit. This just happens to be the maximum zero guaranteed noise immunity since the old RTL micrologic™ specs were published in the early sixties. The problem, in this case, is that it is possible that the timer will not reset on command.

A third problem arises when the user tries to load the Timer running at 15V the same as he does at 5V. The Data Sheets don't inform the user that the power dissipation ratings may be exceeded. Of course, the answer to this problem is a good conservative design approach (by the user) which considers all of the specs collectively instead of each parameter individually.

What can the Engineer who needs a Timer do? Teledyne has introduced a new device which has tackled these three problems head on. The new 355 Timer is designed as part of the company's 300 series HiNIL (High Noise Immunity Logic) family specifically for industrial and commercial applications. It is also designed to be compatible with CMOS, operating with supply voltages ranging from 11V to 16V and specified for full load over the entire supply range, it is a pin-for-pin substitute for the 555 in these applications.

Figure 1 (lower waveform) shows the current waveform generated by the 355. The transient spikes are on the order of only 1 mA. The 2 mA decay is the current change in the timing resistor as the timing capacitor charges to threshold level. Obviously, this will be proportional to the value of the resistor, which in this case is 5K. The half mA step at the beginning of the timeout is the difference in the supply current demanded by the two operating states of the Timer output.

The reset threshold has also been increased to be compatible with HiNIL. Like the trigger and the threshold inputs, the reset threshold level is picked off the voltage divider, so it is proportional to the supply voltage. At 40% of the supply level, the value runs between 4.4 and 6.4 volts for operation over the whole supply variation. This guarantees plenty of noise immunity and no potential danger of non-reset.

Certain compromises were necessary to achieve this performance. First, the device operates only at voltages above 10 volts. Because of this, it is also necessary to reduce the current loading allowed in the high and low states to stay within dissipation limits.

In order to eliminate the current spike, which was the prime objective, the output stage has to be made slower than that of the 555. In most applications, this will go unnoticed.

Another, more subtle, compromise had to be reached when the thresholds were setup. It is obviously desirable that the trigger and reset thresholds are at least close to standard HiNIL levels. It is also desirable for certain applications that the reset threshold is always below the trigger threshold. These two considerations put the trigger level at 45% of V_{CC} instead of at 1/3 V_{CC}. The major effect is that the timing equation changes for astable operation. The period of the astable waveform for the 355 is approximately given by

$$T = 0.5\ C_T\ (R_A + 1.8\ R_B) + 1\ \text{sec.}$$

This compares to $T = 0.7\ C_T\ (R_A + 2\ R_B)$ for the 555, so for given external component values, the 355 will run faster. The 1 sec represents the delays through the 355 and becomes significant at frequencies in the neighborhood of 20 KHz. There is also a similar delay in the 555, though it may be shorter, but there are no published numbers.

As long as attention is paid to the differences that exist, the 355 Timer may be used in place of the 555 in virtually all applications at the higher supply voltages. In these sockets, the 355 will solve many system noise problems.

TELEDYNE SEMICONDUCTOR

Application Brief 4
Keeping the Bugs Out of Microprocessor Systems with High Noise Immunity Logic

An MOS microprocessor system can be troubled by disastrous bugs unless it is protected against noise transients generated by switches, electromechanical peripherals and other nearby noise sources, such as lamps, and machinery. But filters and shielding, the traditional cures, are often difficult to add to a microprocessor because of size and cost constraints.

These problems can be avoided by substituting HiNIL interface devices for conventional I/O logic. HiNIL—Teledyne's bipolar High Noise Immunity Logic—has a guaranteed DC noise immunity about 10 times that of TTL, for example (3.5 vs. 0.4V). Also, HiNIL blocks AC transients large enough to cause TTL malfunctions. Two additional advantages are superior output drive and, in low power systems, protection of CMOS memory and random logic inputs.

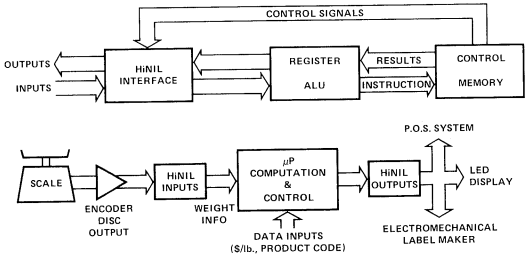
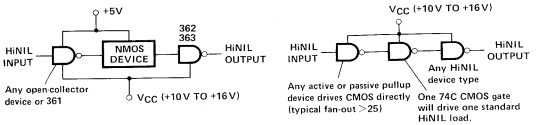


Figure 1. Use of HiNIL interfaces in POS systems with electronic scale. Top diagram shows basic microprocessor configuration.

One manufacturer of microprocessor-controlled electronic scales decided to use the configuration in Figure 1 because he was concerned about the consequences of incorrect weights and prices. The probability of errors resulting from noise transients was high because the scale would be used in a supermarket POS system, where the environment includes refrigerators, fluorescent lamps, meat grinders and electromechanical label makers.

In the system, the microprocessor receives weight codes from an encoder disc in the scale and operates a cash register interface, LED display, and relays of a receipt printer or label maker. The system designers put HiNIL interface logic on the microprocessor board to handle the I/O functions, suppress noise transients picked up along the transmission lines, and drive the peripheral devices. HiNIL output interfaces can drive long lines, relays, displays and lamps without additional components since they sink up to 65 mA and source up to 12 mA. (The new 390 buffer series will sink up to 250 mA.)

Manufacturers of systems requiring random logic are finding that HiNIL and CMOS are an ideal combination. They maximize system noise immunity and assure an excellent system function/power product. HiNIL and 54C/74C CMOS interface directly at V_{CC} voltages from 10 to 16 volts, the power supply range of HiNIL. Moreover, HiNIL protects CMOS inputs from destruction by static electricity and from harmful DC input levels that can exist before CMOS circuits are powered up.



N-channel MOS Complementary MOS

Figure 2. Typical HiNIL/MOS and HiNIL/CMOS interfaces

The rules for using HiNIL with MOS or with CMOS operating at lower voltages are simple. The pullup resistor of an open collector HiNIL device is connected to the desired high logic level voltage (see Figure 2). To use HiNIL with other bipolar logic, just plug in a Teledyne dual or quad interface circuit (see table). HiNIL is also compatible with most analog devices.

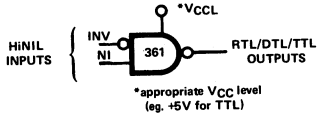
Examples of HiNIL Interface Devices

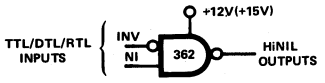
301 Dual 5-Input Power Gate 302 Quad Power NAND Gate (OC)	65mA relay or lamp driver
323 Quad NAND Gate (OC) 332 Hex Inverter (OC) 334 Strobed Hex Inverter (OC)	Input noise protection plus open-collector pullup to other logic levels
350 8-Bit Multiplexer 351 Dual 4-Bit Multiplexer	Drive longer lines than TTL with 10X noise immunity (I_{OH}=12mA)
361 Dual Input Interface 362 Dual Output Interface 363 Quad Output Interface	361 directly connects HiNIL to DTL/RTL/TTL 362 and 363 connect DTL/RTL/TTL to HiNIL
367 Quad Schmitt Trigger 368 Quad Schmitt Trigger (OC)	Suppress 100V/1μs spikes, protect CMOS, decode switches, etc.
380 BCD to Decade Decoder 381 BCD to Decade Decoder (OC) 382 BCD to Decade Decoder 383 BCD to 7-Segment Decoder	Provide decode/drive for lamps, LEDs, gas discharge displays, etc.
390 Interface Buffer Series	250mA HiNIL driver series will be available soon.

If you need a simple, inexpensive solution to a difficult noise problem, write or call Teledyne Semiconductor for a copy of application notes and specifications on Teledyne's High Noise Immunity Logic family.

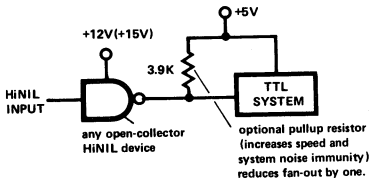
15

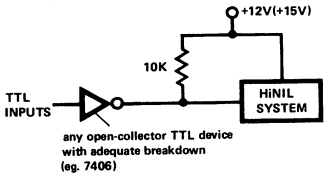
TTL/DTL/RTL



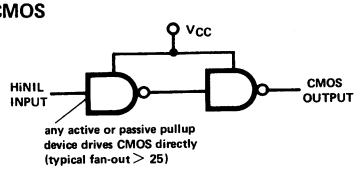


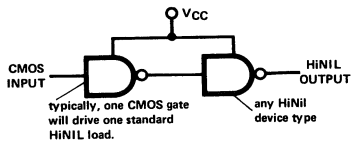
TTL

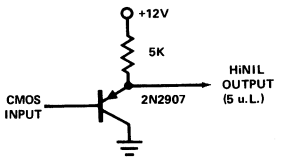




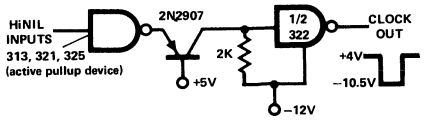
CMOS



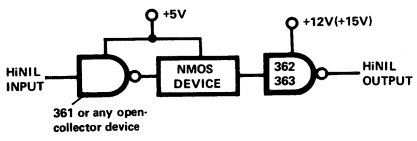




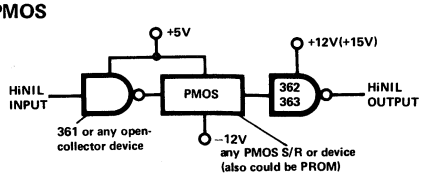
MOS CLOCK DRIVER



NMOS



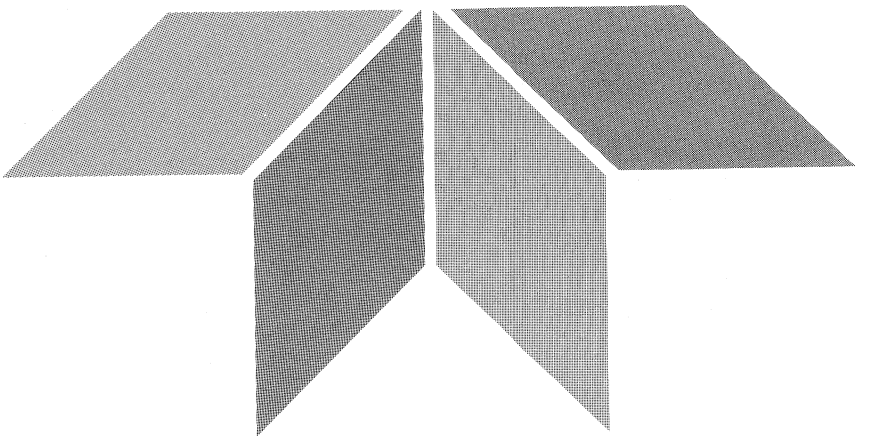
PMOS



15

Application Brief 6
Typical Applications for Bipolar Interface Logic

Telephone Dictation Machine
IC Handling Equipment
Paper Copy Machines
Ion Implanters
Antenna Motor Speed Controllers
High Power Radio Transmitter Protection
Timing and Control Logic for Industrial Laser Systems
Control Module for Mega-Watt Power Supplies
Food Processing Instrumentation
Milling Machine Controllers
Traffic Controllers
Welding Equipment
Ticket Dispensers
Engine Control Alarms
Conveyor Belt Controller
Telephone Answering Equipment
Gasoline Pumps
Logic for Tape Recorders
Collator Machines
Ski Lift Motor Controllers
Frequency Counters
Machine Tool Controllers
Power Plants Instrumentation
Drink Dispensers
Nuclear Power Plants Instrumentation
Car Wash Timers
Engine Analyzers
Vending Machines
Exhaust Emission Testers
Marking Machines
Coin Changers
Slot Machines
Phototypesetting Equipment
Aircraft Navigational Systems
Troop Carriers
Missile Fire Controllers
Shipboard Radar



SECTION 16

Glossary of Terms and Abbreviations

Section 16
Glossary of Terms and Abbreviations 16-1

Brief Glossary For TSC Products

Analog-to-Digital Converter
Electronic device that converts Analog (continuous) information into a Digital word (number). Analog quantities can be temperature, pressure, weight, chemical concentration, noise level, and fluid level.

The Digital result can be a number in binary, decimal, or binary-coded-decimal (BCD).

Auto-Zero
A self-correcting system that insures a Zero output of the ADC for a Zero input.

Binary
Number system with only two values — 0 or 1 — in each numeric position. This is the number system used in computer systems.

Binary-Coded-Decimal (BCD)
A number system whereby binary numbers are grouped in sets of four to represent decimal (Ten system) numbers. This system is shown below.

BCD #	Decimal #
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9

This number system is useful for some A/D converters intended to be used in displaying the output as decimal numbers.

Bit
A single binary number unit, 0 or 1. An 8-bit number could appear as:

10011110 (158 in decimal)
or
01000011 (67 in decimal)

or any other combination from 00000000 to 11111111

Code
Output format of A/D converter. Usually binary, BCD, or sign-magnitude binary.

Digit
A single decimal number unit that can range in value from 0 to 9.

Thus, a 3 1/2 digit A/D converter goes from 0000 to 1999;

a 4 1/2 digit A/C converter can provide outputs from 00000 to 19999;

and a 3 digit converter can provide outputs from 000 to 999.

Note that the "1/2 digit" merely doubles the output range by adding a Most Significant Bit to the output.

Display ADC
An A/D converter normally designed to convert and display the numeric value representing the analog signal. Display ADC's may have the Display Driver built in (as the TSC7106, 7107, 7116, 7117 have), or may provide multiplexed BCD for use by external drivers (the TSC14433, TSC7135, and TSC8750 do this).

Least-Significant-Bit (or Digit)
The lowest number position

for Decimal 1287
↑
Least Significant Digit (LSD)

for Binary 10010011
↑
Least Significant Bit (LSB)

Multiplexed
Signals sharing a common connection but separated in time are said to be multiplexed. Multiplexed BCD is characterized by the 4 BCD signal paths in which the appropriate digits are separated in time.

Resolution
Number of output states offered by the A/D converter. For a binary ADC, the resolution is 2^n; where n equals the number of bits,

thus:
$2^8 = 256$
$2^{10} = 1024$
$2^{12} = 4096$
$2^{14} = 16384$
$2^{16} = 65536$

For decimal and BCD ADCs, the resolution equals 10^n; where n is the number of digits (see "Digit" definition).

Sign
An additional output in some ADCs that are capable of measuring both + and - voltage. The sign bit identifies this polarity (typically, "1" for + and "0" for -). The coding format resulting is called Sign-Magnitude Code.

Glossary of Data Conversion Terms

Absolute Accuracy
The worst-case input to output error of a data converter referred to the NBS standard volt.

Accuracy
The conformance of a measured value with its true value; the maximum error of a device such as a data converter from the true value. See *relative accuracy* and *absolute accuracy.*

A/D Converter
Analog-to-digital converter. A circuit which converts an analog (continuous) voltage or current into an output digital code.

Auto-Zero
A stabilization circuit which serves an amplifier or A/D converter input offset to zero during a portion of its operating cycle.

Bandgap Reference
A voltage reference circuit which is based on the principle of the predictable base-to-emitter voltage of a transistor to generate a constant voltage equal to the extrapolated bandgap voltage of silicon (≈1.22 V).

Binary Code
A positive weighted code in which a number is represented by

$$N = a_0 2^0 + a_1 2^1 + a_2 2^2 + a_3 2^3 + \ldots + a_n 2^n$$

where each coefficient "a" has a value of zero or one. Data converters use this code in its fractional form where:

$$N = a_1 2^{-1} + a_2 2^{-2} + a_3 2^{-3} + \ldots a_n 2^{-n}$$

and N has a fractional value between zero and one.

Binary Coded Decimal (BCD)
A binary code used to represent decimal numbers in which each digit from 0 to 9 is represented by four bits weighted 8-4-2-1. Only 10 of the 16 possible states are used.

Bipolar Mode
For a data converter, when the analog signal range includes both positive and negative values.

Busy Output
See Status Output

Charge Balancing A/D Converter
An analog-to-digital conversion technique which employs an operational integrator circuit within a pulse generating feedback loop. Current pulses from the feedback loop are precisely balanced against the analog input by the integrator, and the resulting pulses are counted for a fixed period of time to produce an output digital word. This technique is also called *quantized-feedback.*

Clock
A circuit in an A/D converter that generates timing pulses which synchronize the operation of the converter.

Common-Mode Rejection Ratio
For an amplifier, the ratio of differential voltage gain to common-mode voltage gain, generally expressed in dB.

$$CMRR = 20 \log_{10} \frac{A_D}{A_{CM}}$$

where A_D is differential voltage gain and A_{CM} is common mode voltage gain.

Conversion Time
The time required for an A/D converter to complete a single conversion to specified resolution and linearity for a full-scale analog input change.

Differential Linearity Error
The maximum deviation of any quantum (LSB change) in the transfer function of a data converter from its ideal size of $FSR/2^n$.

Dual Slope A/D Converter
An indirect method of A/D conversion whereby an analog voltage is converted into a time period by an integrator and reference and then measured by a clock and counter. The method is relatively slow but capable of high accuracy.

End of Conversion
See Status Output

Frequency-To-Voltage (F/V) Converter
A device which converts an input pulse rate into an output analog voltage.

Full-Scale Range (FSR)
The difference between maximum and minimum analog values for an A/D converter input or D/A converter output.

Integral Linearity Error
The maximum deviation of a data converter transfer function from the ideal straight line with offset and gain errors zeroed. It is generally expressed in LSB's or in percent of FSR.

Integrating A/D Converter
One of several types of A/D conversion techniques whereby the analog input is integrated with time. This includes dual slope, triple slope, and charge balancing type A/D converters.

Least Significant Bit (LSB)
The rightmost bit in a data converter code. The analog size of the LSB can be found from the converter resolution:

$$\text{LSB Size} = \frac{FSR}{2^{nk}}$$

where FSR is full-scale range and n is the resolution in bits.

Linearity Error
See Integral Linearity Error and *Differential Linearity Error.*

Missing code
In an A/D converter, the characteristic whereby not all output codes are present in the transfer function of the converter. This is caused by a non monotonic D/A converter inside the A/D.

Monotonicity
For a D/A converter, the characteristic of the transfer function whereby an increasing input code produces a continuously increasing analog output. *Nonmonotonicity* may occur if the converter differential linearity error exceeds ±1 LSB.

Most Significant Bit (MSB)
The leftmost bit in a data converter code. It has the largest weight, equal to one half of full-scale range.

Multiplying D/A Converter
A type of digital-to-analog converter in which the reference voltage can be varied over a wide range to produce an analog output which is the product of the input code and input reference voltage. Multiplication can be accomplished in one, two, or four algebraic quadrants.

Noise Rejection
The amount of suppression of normal mode analog input noise of an A/D converter or other circuit, generally expressed in dB. Good noise rejection is a characteristic of integrating type A/D converters.

Offset Drift
The change with temperature of analog zero for a data converter operating in the bipolar mode. It is generally expressed in ppm/°C of FSR.

Parallel Type A/D Converter
An ultra-fast method of A/D conversion which uses an array of $2^n - 1$ comparators to directly implement a quantizer, where n is the resolution in bits. The quantizer is followed by a decoder circuit which converts the comparator outputs into binary code.

Power Supply Sensitivity
The output change in a data converter caused by a change in power supply voltage. Power supply sensitivity is generally specified in %/V or in %/% supply change.

Ratiometric A/D Converter
An analog-to-digital converter which uses a variable reference to measure the ratio of the input voltage to the difference.

Relative Accuracy
The worst case input to output error of a data converter, as a percent of full-scale, referred to the converter reference. The error consists of offset, gain, and linearity components.

Resolution
The smallest change that can be distinguished by an A/D converter or produced by a D/A converter. Resolution may be stated in percent of full-scale, but is commonly expressed as the number of bits n where the converter has 2^n possible states.

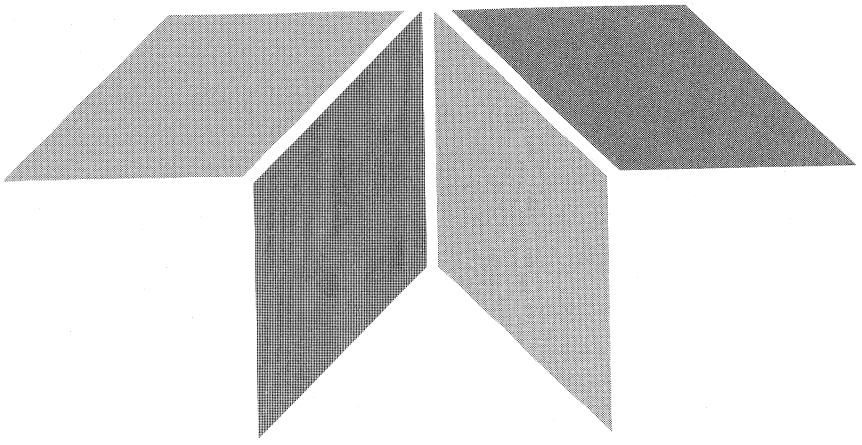
Status Output
The logic output of an A/D converter which indicates whether the device is in the process of making a conversion or the conversion has been completed and output data is ready. Also called *busy output* or *end of conversion* output.

Temperature Coefficient
The change in analog magnitude with temperature, expressed in ppm/°C.

Three-State Output
A type of a/D converter output used to connect to a data bus. The three output states are logic 1, logic 0, and off. An *enable* control turns the output on or off.

Voltage-To-Frequency (V/F) Converter
A device which converts an analog voltage into a train of digital pulses with frequency proportional to the input voltage.

Zero Drift
The change with temperature of analog zero for a data converter operating in the unipolar mode. It is generally expressed in μV/°C.



SECTION 17

Distributors and Representatives

Section 17
Distributors and Representatives 17-1

Main Sales Offices

Domestic Sales Offices

Teledyne Semiconductor
1300 Terra Bella Avenue
Mountain View, CA 94943
415/968-9241
TWX: 910-379-6494

Teledyne Semiconductor
Western Regional Sales Office
1300 Terra Bella Avenue
Mountain View, CA 94043
415/968-3868 or
415/968-6140
TWX: 910-379-6494

Teledyne Semiconductor
Central Regional Sales Office
5105 Tollview Drive
Suite 107
Rolling Meadows, IL 60008
312/394-5599
TWX: 910-687-0272

Teledyne Semiconductor
Eastern Regional Sales Office
284 North Roadway
Salem, NH 03079
603/893-9551
TWX: 710-366-1110

Foreign Sales Office

Teledyne Semiconductor
Abraham Lincoln Street 38-42
6200 Wiesbaden
West Germany
Telephone 49-7741-5066
TWX: 841-792-1462

Teledyne Semiconductor
Heathrow House, Bath Road
Cranford, Hounslow
Middlesex, TW5 9QQ
England
Telephone 44-01-897-2503
TWX: 851-935008

Teledyne Semiconductor
10 Sam Chuk Street
San Po Kong Kowloon
Hong Kong
Telephone 3-240122
TLX: 780-73549

United States Representatives

Arizona

Luscombe Engineering Company
4424 N. Scottsdale Road
Suite 600
Scottsdale, AZ 85251
602/949-9333
TWX: 910-950-1333

California

Bestronics, Inc.
5150 Overland Avenue
Suite E1
Culver City, CA 90230
213/870-9191
TWX: 910-340-6369

Pacific Electronics, Inc.
21060 Homestead Road
Suite 207
Cupertino, CA 95014
408/733-9920
TLX: 17-2760

Bestronics, Inc.
18011 Sky Park Circle
Suite L
Irvine, CA 92714
714/979 9910
TWX: 910-595-2781

Bestronics, Inc.
10150 Sorranto Valley Road
Suite 300
San Diego, CA 92121
619/452-5500
TWX: 910-335-1267

Bestronics, Inc.
6351 Owensmouth Avenue
Suite 102
Woodland Hills, CA 91367
213/704-5616
TWX: 910-494-4600

Florida

Electrocraft, Inc.
1500 North University Drive
Suite 225
Coral Springs, Fl 33065
305/753-8666

Electrocraft, Inc.
8691 Somerset Drive
Largo, FL 33543
813/530-4749

Electrocraft, Inc.
1950 Lee Road
Suite 112F
Winter Park, FL 32790
305/628-4705

Georgia

Dixie Technical Marketing
925 Main Street
Suite 203
Stone Mountain, GA 30086
404/962-2530

Illinois

Kennaugh & Associates
701 E. Irving Park Road
Roselle, Il 60172
312/980-7570

Indiana

The Given Corporation
3301 Portage Boulevard
Suite 8
Fort Wayne, IN 46804
219/432-5585
TWX: 810-332-1412

Kansas

Midtec Associates, Inc.
7702 Mize
Desoto, KS 66018
913/331-6565
TWX: 910-743-4129

Maryland

Walker-Houck Associates
1205 Oak Croft Drive
Lutherville, MD 21903
301/296-6021
TWX: 710-232-0012

Massachusetts

Dynasel Associates
22 Green Road
Waltham, MA 02154
617/890-6777
TWX: 710-324-0202

Michigan

KRW Sales
13570 Silver Lake
Brighton, MI 48116
313/437-7255

KRW Sales
1843 Nelson S.E.
Grand Rapids, MI 49507
616/363-2953

Minnesota

Quantum Sales
10800 Mormandale Boulevard
Suite 100
Bloomington, MN 55437
612/884-4700
TWX: 910-576-2758

Missouri

Midtec Associates, Inc.
8360 Lindberg North
Suite 11
Florissant, MO 63031
314/837-5200

New Jersey

TAM
389 Pasaic Avenue
Fairfield, NJ 07006
201/575-4390
TWX: 710-734-4308

Sunday O'Brien
15 Potter Street
Haddenfield, NJ 08033
609/429-4013

New York

Quality Components
3343 Harlem Road
Buffalo, NY 14225
716/837-5430

Quality Components
116 E. Fayette St.
Manlius, Ny 13104
315/682-8885
TWX: 710-545-0663

TAM
1727 Veterans Memory Highway
Suite 408
South Hauppauge, NY 11722
516/348-0800

United States Representatives (Cont.)

North Carolina

Dixie Technical Marketing
667 Knollwood Drive
P.O. Box 1333
Mt. Airy, NC 27030
919/789-9759

Ohio

KRW Sales
P.O. Box 45008
Westlake, OH 44145
216/871-7521

Oklahoma

Cunningham Components
7917 S. 72nd E. Avenue
Tulsa, OK 74113
918/492-0390

Pennsylvania

KRW Sales
227 Allegheny Avenue
Oakmont, PA 15139
412/261-1323

Texas

Cunningham Components
8330 Burnet Road
Suite 135
Austin, TX 78758
512/459-9100

Cunningham Components
4332 Spring Valley Road
Dallas, TX 75234
214/233-4303

Cunning Components
9440 Old Katy Road
Suite 100
Houston, TX 77055
713/461-4197

Virginia

Walker-Houck Associates
Rt. 1 Box 110-41
Moneta, VA 24121
703/297-4496

Washington

SDR²
14230 N.E. 8th Street
Bellevue, WA 98007
206/747-9424 or
216/624-2621
TWX: 910-443-2483

Canadian Representatives

Canada

Vitel Electronics, Inc.
4019 Carling Ave.
Suite 3301
Kawata, Ontario KWK 2A3
613/592-0090

Vitel Electronics
5945 Airport Road
Suite 180
Mississauga, Ontario L4V 1R9
416/676-9720
TWX: 610-492-2528

Vitel Electronics
3300 Cote Vertu
Suite 203
St. Laurent, Quebec
514/331-7393

United States Distributors

Alabama

Powell Electronics
704 Arcadia Circle
Huntsville, AL 35801
205/539-2731
TWX: 710-826-2231

Arkansas

Marshall Industries
835 W. 22nd Street
Tempe, AR 85282
602/968-6181

California

Marshall Industries
8015 Deering Avenue
Canoga Park, CA 91304
213/999-5001

Marshall Industries
9674 Telstar Avenue
El Monte, CA 91731
213/442-7204

Marshall Industries
17321 Murphy Avenue
Irvine, CA 92714
714/556-6400

Marshall Industries
10105 Carroll Canyon Road
San Diego, CA 92131
619/578-9600

R.V. Weatherford
1310 Kifer Road
Sunnyvale, CA 94086
408/738-8694

Marshall Industries
788 Palomar Avenue
Sunnyvale, CA 94086
408/732-1100

Colorado

Marshall Industries
7000 North Broadway
Building 1, Suite 108
Denver, CO 80221
303/427-1818

A.C.T.
4016 Young Field
Wheat Ridge, CO 80033
303/422-9229

Connecticut

Marshall Industries
Village Lane, Box 200
Barnes Industrial Park
Wallingford, CT 06792
203/265-3822

Florida

Marshall Industries
4205 34th Street
Orlando, FL 32805
305/841-1878

Georgia

Marshall Industries
4364B Shackelford Road
Norcross, GA 30093
404/923-5750

Illinois

Marshall Industries
1261 Wiley
Schaumburg, IL 60195
312/490-0155

Semiconductor Specialists
195 Spangler
Elmhurst, IL 60126
312/279-1005

Advent Electronics
7110-16 N. Lyndon Street
Rosemont, IL 60018
312/298-4210
TWX: 910-233-2477

Indiana

Advent Electronics
8446 Moller Road
Indianapolis, IN 46268
317/872-4910
TWX: 810-341-3228

Iowa

Deeco, Inc.
2500 16th Avenue S.W.
Cedar Rapids, IA 52406
319/365-7551

Advent Electronics
682 58th Avenue Ct S.W.
Cedar Rapids, IA 52404
319/363-0221
TWX: 910-525-1337

Massachusetts

Marshall Industries
One Wilshire Road
Burlington, MA 01803
617/272-8200

Now Electronics
85 Speen Street
Framingham, MA 01701
617/872-5876

Future Electronics
133 Flanders Rd.
Westborough, MA 01580
617/366-3400
TWX: 710-390-0374

Maryland

Marshall Industries
16760 Oakmont Ave.
Gaithersburg, MD 20877
301/840-9450

Pyttronic Industries
8220 Wellmore Street
Savage, MD 20863
301/792-0780

Michigan

Advent Electronics
24713 Crestview Court
Farmington Hills, MI 48018
313/477-1650

Calder Electronics
6731 28th Street S.E.
Grand Rapids, MI 49506
616/949-2900

United States Distributors (Cont.)

Minnesota

Semiconductor Specialist
1701 E. 79th Street
Suite 6
Bloomington, MN 55420
612/854-8841

The Joel Company
8836 7th Avenue North
Minneapolis, MN 55427
612/545-5669
TWX: 916-576-317

Missouri

Semiconductor Specialists
3805 North Oak Trafficway
Kansas City, MO 64116
816/452-3900

New Jersey

Marshall Industries
101 Fairfield Road
Fairfield, NJ 07006
201/882-0320

Marshall Industries
102 Gaither Drive
Mt. Laurel, NJ 09054
609/234-9100

Vantage Electronics
257 Park
Nutley, NJ 07110
201/667-1840

New York

Future Electronics
7 Adler Drive
E. Syracruse, NY 13057
315/463-6633
TWX: 710-541-0402

SAI
564 Smith Street
Farmingdale, NY 11735
516/293-2710
TWX: 510-224/2710

Marshall Industries
275 Oser Avenue
Hauppauge, LI NY 11788
516/273-2424

Marshall Industries
1260 Scottsville Road
Rochester, NY 14624
716/235-7620

Ohio

Hughes-Peters, Inc.
4865 Duck Creek Road
P.O. Box 237119
Cincinnati, OH 45227-0119
513/351-2000
TWX: 810-461-2885

Reptron Electronics, Inc.
830 Busch Court
Columbus, OH 43229
614/436-6675

Hughes-Peters, Inc.
481 E. 11th Ave.
Columbus, OH 43212
614/294-5351
TWX: 810-482-1760

Marshall Industries
6212 Executive Boulevard
Dayton, OH 45424
513/236-8088

Oklahoma

Quality Components
9934 E. 21st Street South
Tulsa, OK 74129
918/664-8812

Pennsylvania

Pyttronic Industries
P.O. Box 433, Stump Road
Montgomeryville, PA 18936
215/643-2850
TWX: 510-224-6067

Texas

Quality Components
4257 Kellway Circle
P.O. Box 819
Addison, TX 75001
214/387-4949
TWX: 910-860-5459

Active Components Technology
P.O. Box 1164
15800 Addison Road
Addison, TX 75001
214/980-1888

Active Components Technology
6448 Highway 290 East
Building A, 108
Austin, TX 78723
512/452-5254

Texas (Cont.)

Quality Components
2427 Rutland Drive
Austin, TX 78758
512/835-0220
TWX: 910-874-1377

Marshall Industries
14205 Proton Road
Dallas, TX 75234
214/233-5200

Solid State Electronics
P.O. Box 20299
Dallas, TX 75220
214/438-5700
TWX: 910-860-5069

Marshall Industries
3698 Westchase Drive
Houston, TX 77042
713/789-6600

Solid State Electronics
9515 Town Park
Houston, TX 77036
713/772-8483
TWX: 910-881-7251

Quality Components, Inc.
1005 Industrial Boulevard
Sugarland, TX 77478
713/491-2255

Washington

Shannon Ltd.
7030 South 188th Street
Kent, WA 98031
206/763-0545

Marshall Industries
14102 N.E. 21st Street
Bellevue, WA 98007
206/747-9100

Wisconsin

Taylor Electric Company
100 West Donges Bay Road
Mequon, WI 53092
414/241-4321
TWX: 910-262-3414

Canadian Distributors

Canada

Intek Electronics
10-8385 St. George Street
Vancouver, British Columbia
V5X AP3
604/324-6831

Future Electronics
3070 Kingsway
Vancouver, British Columbia
V5R 5J7
604/438-5545

Future Electronics
5809 McLeod
Trail South Unit 109
Calgary, Alberta T2H OJ9
403/259-6408

Future Electronics
1050 Baxter Road
Ottawa, Ontario K2C 3P2
613/820-831

Future Electronics
4800 Dufferin Street
Downsview, Ontario M3H 5S8
416/663-5563

Future Electronics
237 Hymus Blvd.
Pointe Claire, Quebec H9R 5C7
514/694-7710
TWX: 610-421-3500 or
610-421-3251

International Representatives and Distributors

Australia

Promark Electronics
Pty. Ltd.
Suite 102, 6-8 Clarke Street,
Crows Nest, NSW 2065,
Australia
Telephone: 439-6571 or 439-6965
TLX: 20474

England

Semiconductor Supplies Int. Ltd.
Dawson House
128/130 Carshalton Road
Sutton, Surrey
Telephone: 01 643 1126
TWX: 946650

Macro Marketing Ltd.
Burnham Lane
Slough
Berkshire SL1 6LN
Telephone: 06286 4422
TWX: 847945

Norsem Electronics Ltd.
Norsem House
Unit 4 - Heron Ind Estate
Spencers Wood
Reading, Berks
Telephone: 0734 884588
TWX: 849727

Norsem Electronics Ltd.
Level One, Civic Center
Hartlepool
Cleveland
Telephone: 0429-33501
TWX: 587785

England (Cont.)

Semicomps Ltd.
Halifax Road
Keighley
West Yorks
Telephone: 0535-65191
TWX: 517343

Semicomps Ltd.
East Bowmont Street
Kelso
Roxburghshire
Telephone: 05732 2366
TWX: 72692

Phoenix Electronics Ltd.
Western Buildings
Vere Road
Kirkmuirhill
Lanarkshire
Telephone: 0555 892393
TWX: 77404

Phoenix Electronics Ltd.
99 Windsor Road
Oldham
Lancashire
Telephone: 061-633-2463
TWX: 77404

France

Tekelec Airtronic
Cite Des Bruyeres
Rue Carle Vernet
Telephone: 0033 1-5347535
TWX: 042 204552

Germany

Adelco Elektronik GMBH
Boxholmstr. 5
2085 Quickborn
Telephone: 04106 2024
TWX: 2180619

Emtron Elektronik
Electronic Vertriets GMBH
Waldstrasse 55
6085 Nauheim
Telephone: 06152 6003
TWX: 4191175

ING. T. Henskes GMBH
Radenstedter Str. 9
3000 Hannover 91
Telephone: 0511 456082
TWX: 923509

Hot Elektronik
Wendelsteinweg 11
8028 Taufkirchen
Telephone: 089 6121092
TWX: 529528

Hot Elektronik
Schulstr. 22
7060 Schorndorf
Telephone: 07181 3093-95
TWX: 7246622

Metronik GMBH
Kapellenstr. 9
8025 Unterhaching
Telephone: 089 6114063
TWX: 529524

Metronik GMBH
Sifmensstr. 4-6
6805 Heddesheim
Telephone: 06203 4701
TWX: 465035

International Representatives & Distributors (Cont.)

Germany (Cont.)

Metronik GMBH
Vogelsgarten 1
8500 Nuernberg
Telephone: 0911 468066-67
TWX: 626205

Metronik GMBH
Semerteichst. 92
4600 Dortmund 30
Telephone: 0231 423037 - 38
TWX: 8227082

Rein Elektronik GMBH
Loftscher Weg 66
4054 Nettetal 1
Telephone: 02153 71971
TWX: 854251

Semitron W. Roeck GMBH
Im Gut 1
7891 Kuessarerg 6
Telephone: 07742 7011
TWX: 7921472

Semitron
Heidelberger Str. 71
6140 Rensheim/Bergstrasse
Telephone: 06251 6085
TWX: 468212

Italy

Eledra Spa
Viale Elvezia 18
1-20154 Milano
Telephone: 0039 2-349751
TWX: 043 332332

Japan

Teijin Advanced Products Corp.
1-1, Uchisaiwai-Cho 2-Chome
Chiyoda-Ku, Tokyo 100
Telephone: (03) 506-4670
TLX: J-23548

Sil-Walker Inc.
1-1, Shinjuku 5-Chome
Shinjuku-Ku, Tokyo 160
Telephone: (03) 341-3651
TLX: 0232-3398

Korea

Vine-Overseas Trading Corp.
Rm. 308, Korea Electric
Association Bldg.,
11-4, Supyo-Dong, Jung-Ku
Seoul
Telephone:
266-1663/265-9875/269-0832
TLX: K24154

Netherlands

Alcom Electronics
Hollandsch Diep 57
NL-2904 EP Capella A.D. IJSSEL
Telephone: 031 10-519533 or
0031 10-519533
TWX: 044 26160

New Zealand

Professional Electronics Ltd.
22A, Milford Road
Milford, Auckland
Telephone: 493-048/029
TLX: NZ21084

Spain

Amitron S.A.
C/Loeches 6, Bajo D
Madrid - 8
Telephone: 0034 1-2479313
TWX: 052 45550

Switzerland

Ena A.G.
Hermetschloostr. 75
CH-8048 Zuerich
Telephone: 0041 1-645757
TWX: 045 822303

Omni Ray A.G.
Dufourstr. 56
CH-8008 Zuerich
Telephone: 0041 1-2520766
TWX: 045 57198

Taiwan

Timkuo Taiwan Ltd.
8F-2, 157 Fu Hsing S. Road
Sec. 2, Taipei
Telephone: (02) 709-2246
TLX: 26206

TELEDYNE SEMICONDUCTOR
1300 Terra Bella Avenue • Mountain View, CA 94043 • Telephone: (415) 968-9241